



SANYO Semiconductors

DATA SHEET

Monolithic Linear IC

LA6324NJM — High-Performance Quad Operational Amplifier

Overview

The LA6324NJM is a high-performance quad operational amplifier that can operate from a single voltage power supply. It features a built-in phase correction circuit. It can also operate from a dual power supply with both positive and negative levels and features low power consumption. The LA6324NJM is a wide operating temperature range ($T_{opr} = -40$ to 85°C) allows the device to be used for a wide variety of applications in consumer products as well as industrial equipment, including automotive applications (excluding critical safety components).

Functions

- High-performance quad operational amplifier

Specifications

Maximum Ratings at $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		32	V
Differential input voltage	V_{ID}		32	V
Maximum input voltage	V_{IN} max		-0.3 to +32	V
Output short time *1	VO_{shT}		Infinity	sec
Allowable power dissipation	P_d max	$T_a \leq 25^{\circ}\text{C}$ *2	330	mW
Operating temperature	T_{opr}		-40 to +85	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

*1: 15V or less, only by one arbitrary channel. Moreover, the LA6324NJM must be used under the conditions that its maximum power dissipation (P_d max) is not exceeded and the following derating factor is observed.

*2: At $T_a > 25^{\circ}\text{C}$, a derating factor of $-2.64\text{mW}/^{\circ}\text{C}$.

Recommended Operating Conditions at $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		3		24	V

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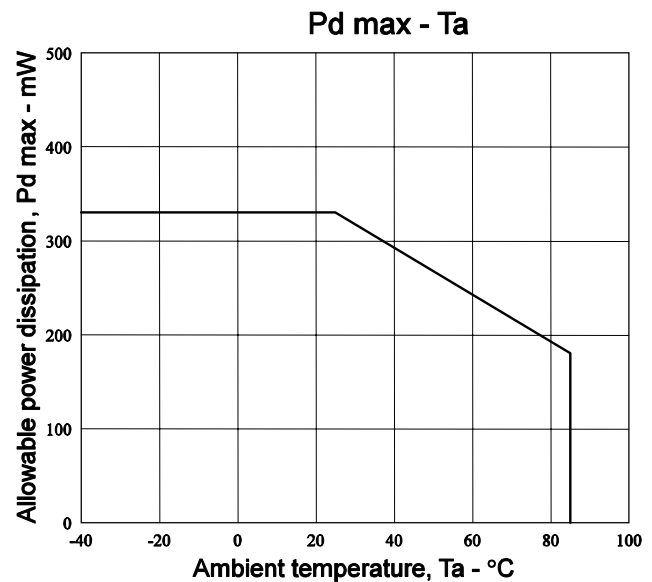
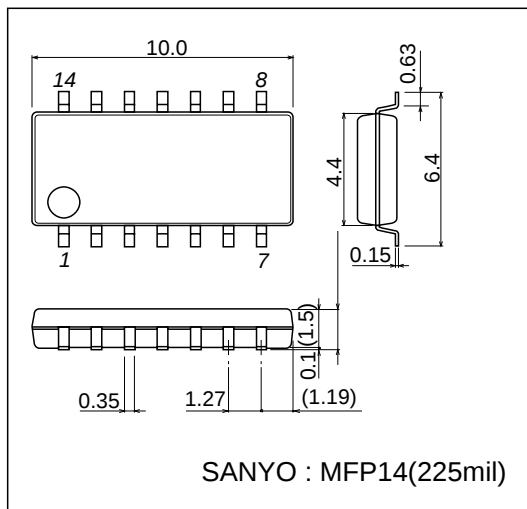
LA6324NJM

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

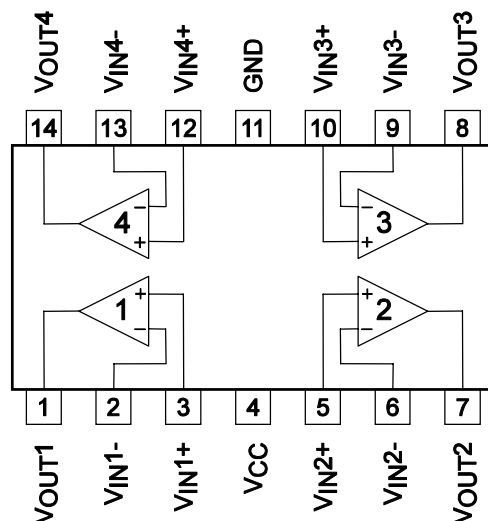
Parameter	Symbol	Conditions	Test Circuit	Ratings			Unit
				min	typ	max	
Input offset voltage	V_{IO}		1		± 2	± 7	mV
Input offset current	I_{IO}	$I_{IN(+)} / I_{IN(-)}$	2		± 5	± 50	nA
Input bias current	I_B	$I_{IN(+)} / I_{IN(-)}$	3,4		45	250	nA
Common-mode input voltage range	V_{ICM}		5	0		$V_{CC}-1.5$	V
Common-mode rejection ratio	CMR	$V_{CC} = 30\text{V}$	5	65	80		dB
Large-amplitude voltage gain	VG	$V_{CC} = 15\text{V}$, $R_L \geq 2\text{k}\Omega$	6	25	100		V/mV
Output voltage range	V_{OUT}			0		$V_{CC}-1.5$	V
Supply voltage rejection ratio	SVR		11	65	100		dB
Channel separation	CS	$f = 1\text{kHz}$ to 20kHz	7		120		dB
Current drain	I_{CC}		8		0.6	2	mA
		$V_{CC} = 30\text{V}$			1.5	3	mA
Output current (source)	$I_{O \text{ source}}$	$V_{IN+} = 1\text{V}$, $V_{IN-} = 0\text{V}$	9	20	40		mA
Output current (sink)	$I_{O \text{ sink}}$	$V_{IN+} = 0\text{V}$, $V_{IN-} = 1\text{V}$	10	10	20		mA

Package Dimensions

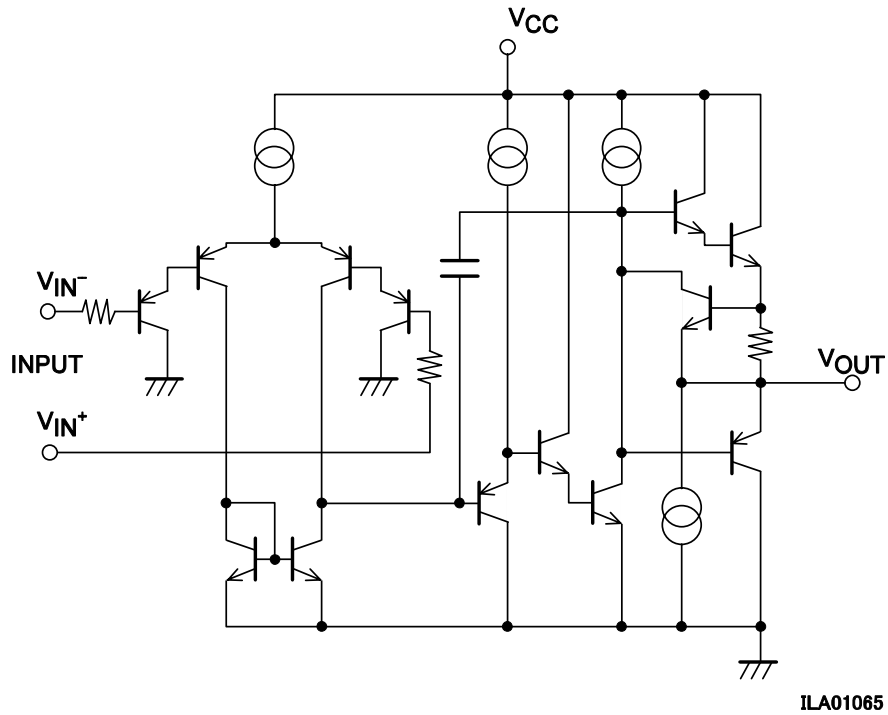
unit : mm
3034B



Pin Assignment



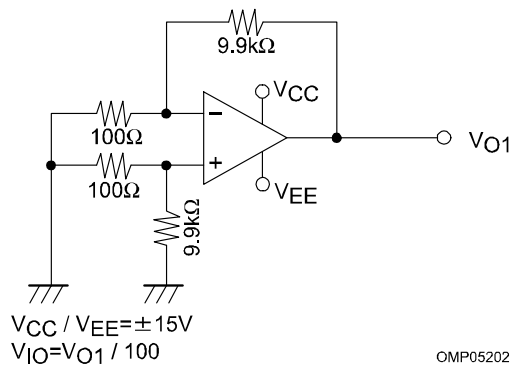
Equivalent Circuit



1LA01065

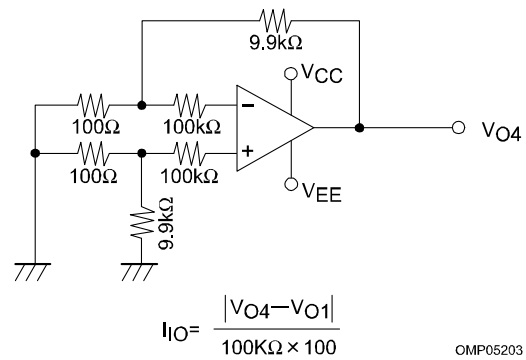
Test Circuits

1. Input offset voltage V_{IO}



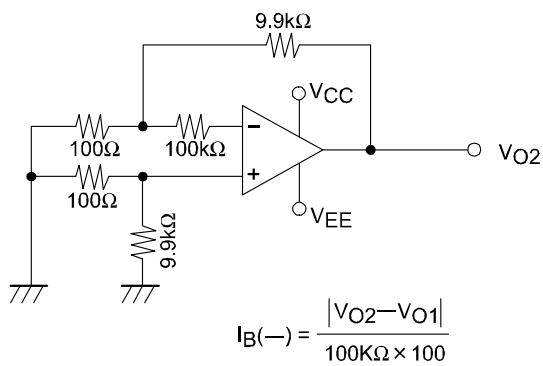
OMP05202

2. Input offset current I_{IO}



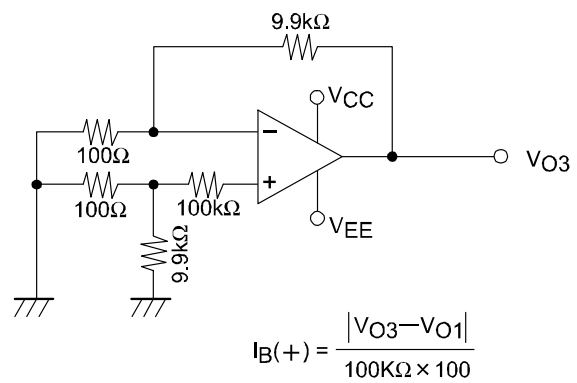
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3. Input bias current $I_B (-)$



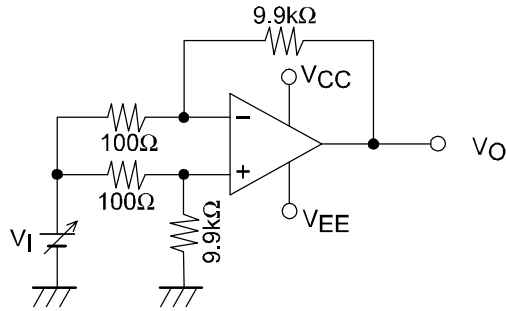
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4. Input bias current $I_B (+)$



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5. Common-mode rejection ratio CMR
Common-mode input voltage range VICN

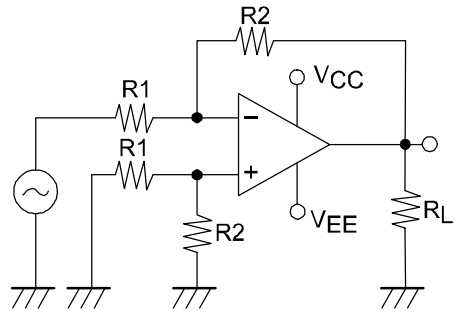


CMR $V_I = \pm 7.5V$

$$CMR = 20 \log \frac{15 \times 100}{|\Delta V_O|}$$

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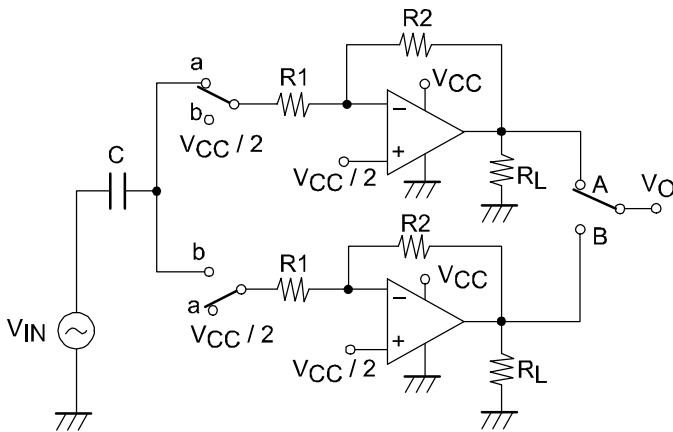
6. Voltage gain V_G



$$V_G = \frac{R_2}{R_1}$$

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7. Channel separation CH sep



When the switch is in the "a" position

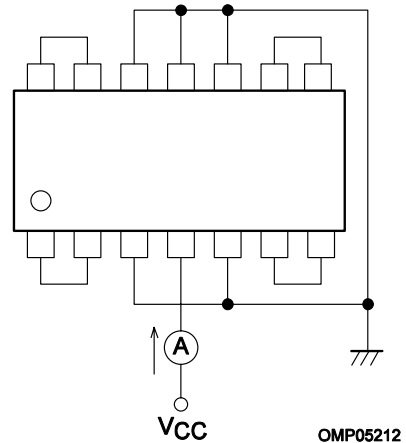
$$CS(A \rightarrow B) = 20 \log \frac{R_2 V_{OA}}{R_1 V_{OB}}$$

When the switch is in the "b" position

$$CS(B \rightarrow A) = 20 \log \frac{R_2 V_{OB}}{R_1 V_{OA}}$$

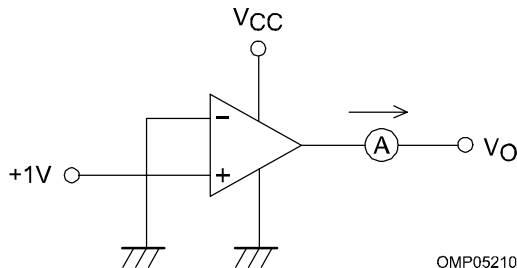
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8. Current drain I_{CC}



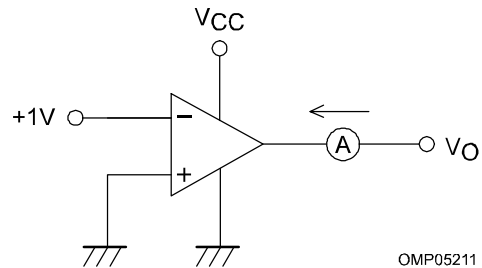
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9. Output current I_O source



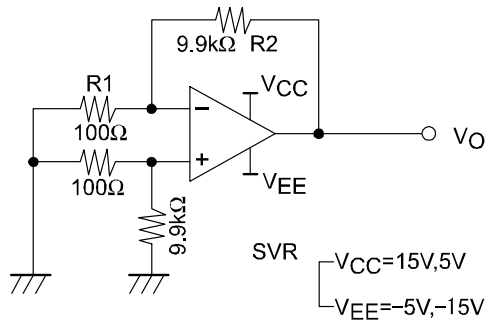
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10. Output current I_O sink



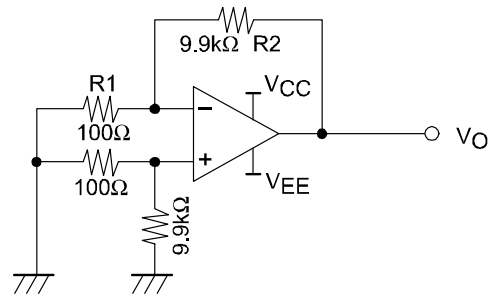
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11. Supply voltage rejection ratio SVR (+)



$$SVR(+)=20\log \left| \frac{\Delta V_{CC} \times 100}{\Delta V_O} \right|$$

12. Supply voltage rejection ratio SVR (-)



$$SVR(-)=20\log \left| \frac{\Delta V_{EE} \times 100}{\Delta V_O} \right|$$

OMP05213

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