MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44001

Chroma 4
VIDEO PROCESSOR

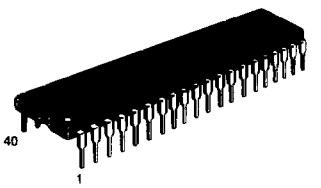
SILICON MONOLITHIC
INTEGRATED CIRCUIT

Product Preview

Chroma 4 Multistandard Video Processor

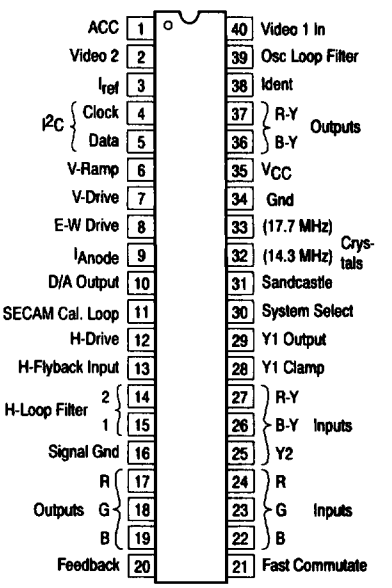
The MC44001 is a highly advanced circuit which performs most of the basic functions required for a color TV. All of its advanced features are under processor control via an I^2C bus, enabling potentiometer controls to be removed completely. In this way the component count may be reduced dramatically, allowing significant cost savings together with the possibility of implementing sophisticated automatic test routines. Using the MC44001, TV manufacturers will be able to build a standard chassis for anywhere in the world.

- Operation from a Single + 5.0 V Supply; Typical Current Consumption Only 120 mA
- Full PAL/SECAM/NTSC capability
- Dual Composite Video or S-VHS Inputs
- All Chroma/Luma Channel Filtering, and Luma Delay Line Are Integrated Using Sampled Data Filters Requiring No External Components
- Filters Automatically Commutate with Change of Standard
- Chroma Delay Line is Realized with a 16 Pin Companion Device, the MC44140
- RGB Drives Incorporate Contrast and Brightness Controls and Auto Gray Scale
- Switched RGB Inputs with Separate Saturation Control
- Auxiliary Y, R-Y, B-Y Inputs
- Line Timebase Featuring H-Phase Control, Time Constant and Switchable Phase Detector Gain
- Vertical Timebase Incorporating Vertical Geometry Corrections
- E-W Parabola Drive Incorporating Horizontal Geometry Corrections
- Beam Current Monitor with Breathing Compensation



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)*

Ratings	Pin	Symbol	Value	Unit
Supply Voltage	35	V_{CC}	6.0	Vdc
Operating Ambient Temperature	35	T_A	0 to + 70	°C
Storage Temperature	—	T_{stg}	− 65 to +150	°C
Junction Temperature	—	T_J	+150	°C
Drive Output Sink Current	12	I_{12}	2.0	mA
Applied Voltage Range:				Vdc
E-W Drive	8	V_8	0 to + 7.0	
Feedback	20	V_{20}	0 to + 7.0	
Anode Current	9	V_9	− 2.0 to V_{CC}	
All Other Pins	—	V_i	0 to V_{CC}	

* (Based on C26K, C32K, C63K and C88K geometries characterizations)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44001P	0° to + 70°C	Plastic DIP

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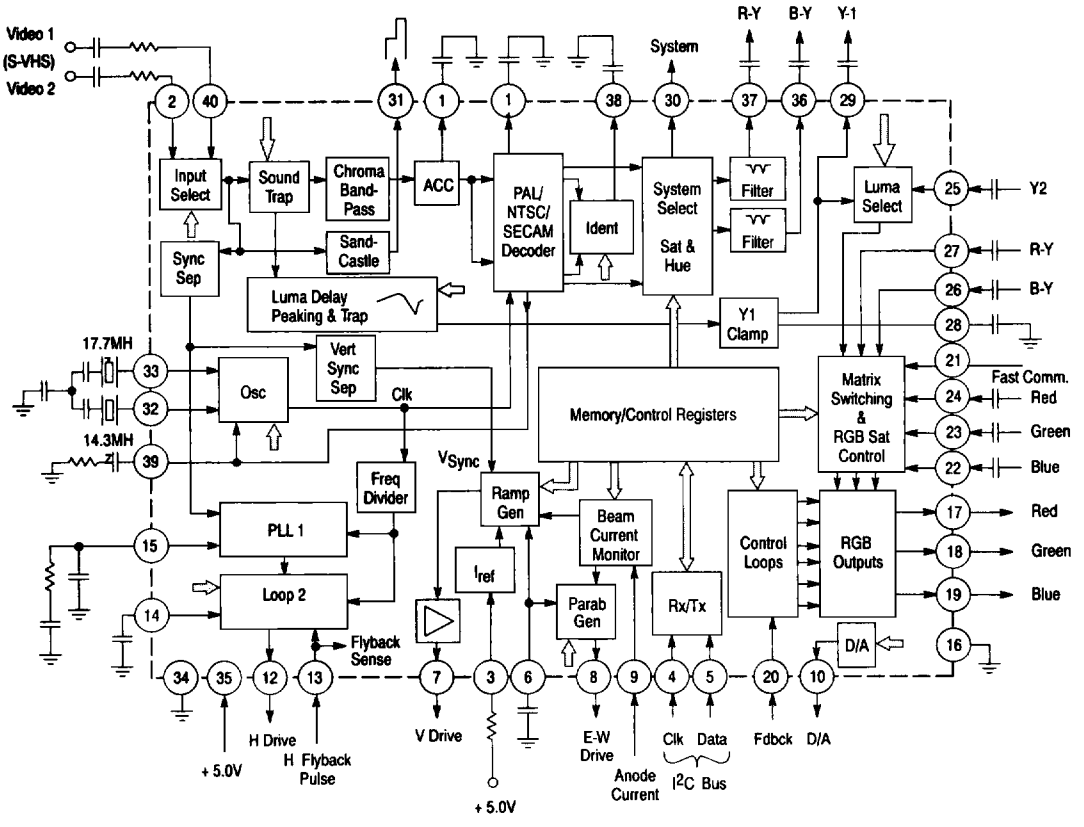
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, I_3 = 70 µA, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	35	4.75	5.0	5.12	V
Operating Current	35	90	120	180	mA
Reference Current, Input Voltage	3	1.0	1.30	1.60	V
D/A Output Offset D/A Output Register Set to 00	10	– 5.0	0	+ 5.0	µA
D/A Output Range D/A Output Register Varying from 00 to 63	10	100	300	500	µA

NOTES: Composite Video Input Signal Level = 1.0 Vpp
Black-to-White = 0.7 Vpp, Syn-to-Black = 0.3 Vpp
PAL/NTSC = 75% color bars; Burst = 300 mVpp
SECAM = 75% color bars
Horizontal Timebase started (subaddress 00)
Vertical Breathing control set to 00; V9 = 0 V
All other analog controls set to midrange 32
Video Peaking "P1, P2, P3" bits high

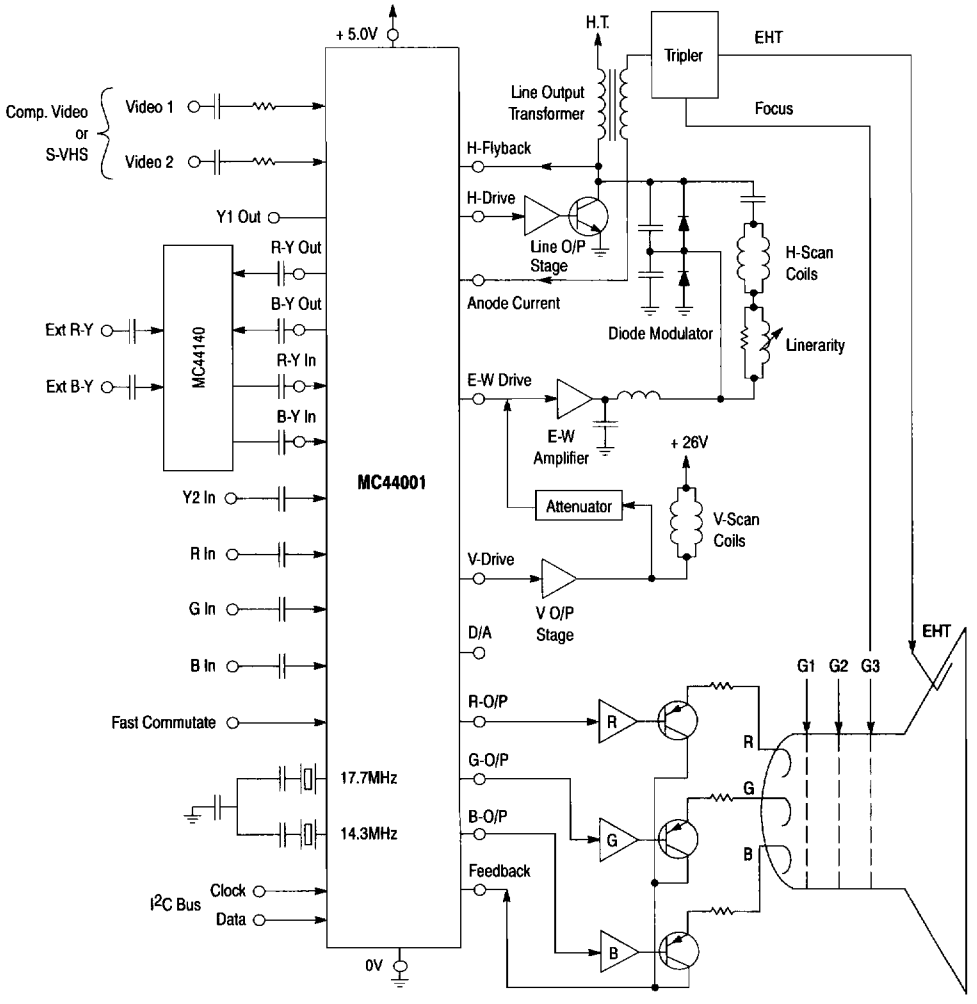
Simplified Block Diagram



GENERAL DESCRIPTION OF THE CHROMA 4 SYSTEM

Figure 1 shows a simplified block diagram representation of the basic system using the MC44001 and its companion device the MC44140 chroma delay line. The Chroma 4 has been designed to carry out all the processing of video signals, display controls and timebase functions. There are two video inputs which can be used for normal composite video or separate Y and C inputs. In either case, the inputs are interchangeable and selection is made via the I²C bus. The video is decoded within the MC44001 which involves separation, filtering and delay of the luminance part of the signal, and demodulation of the chroma into color difference signals. The luminance (called Y1) together with the demodulated R-Y and B-Y are all then brought out from the IC. The color difference signals then enter the MC44140 which performs color correction in PAL and the delay line function in SECAM. Corrected color difference signals then re-enter the MC44001.

Figure 1. Connection to TV Chassis



The next stage is called the color difference stage where a number of control functions are carried out together with matrixing of the components to derive RGB signals. At this point a number of auxiliary signals may also be switched in, again all under MCU control. External RGB (text) and Fast Commutate enter here; also an external luminance (Y2) may be used instead of Y1. External R-Y and B-Y are switched in via the delay line circuit to save pins on the main device. The Y2 and External R-Y, B-Y will obviously be of considerable benefit from the system point of view for use with either feature boxes MAC or CTI.

The final stage of video processing is the RGB outputs which drive the high voltage amplifiers connected to the tube cathodes. These outputs are controlled by a sophisticated digital servo-loop which is maintained and stabilized by a sequentially sampled beam current feedback system. Automatic gray scale control is featured as a part of this system.

Both horizontal and vertical timebases are incorporated into the MC44001 and control is via the I^2C bus. The horizontal timebase employs a dual loop system of a PLL and variable phase shifter, and the vertical uses a countdown system. For the vertical, a field rate sawtooth is available which is used to drive an external power amplifier with flyback generator (usually a single IC). The line output consists of a pulse which drives a conventional line output stage in the normal way. The line flyback pulse is sensed and used by the second loop for horizontal phase shift.

Where E-W correction is required, a parabola waveform is available for this which, with the addition of a power amplifier, can be used with a diode modulator type line output stage for dynamic width and E-W control. The bottom of the EHT overwinding is returned to the MC44001 and is used for anode current monitoring and anti-breathing correction.

A much more detailed description of each stage of the MC44001 will be found in the next section. Information on the delay line is to be found in this data sheet.

Introduction

The following information describes the basic operation of the MC44001 IC together with the MC44140 chroma delay line. The MC44001 is a highly advanced circuit which performs all the video processing, timebase and display functions needed for a modern color TV. The device employs analog circuitry but with the difference that all its advanced features are under processor control, enabling external filtering and potentiometer adjustments to be removed completely. Sophisticated feedback control techniques have been used throughout the design to ensure stable operating conditions and the absence of drift with age.

The IC described herein is one of a new generation of TV circuits, which make use of a serial data bus to carry out control functions. Its revolutionary design concept permits a level of integration and degree of flexibility never achieved before. The Chroma 4 consists of a single bipolar VLSI chip which uses a high density, high frequency, low voltage process called MOSAIC 1.5. Contained within this single 40 pin package is all the circuitry needed for the video signal processing, horizontal and vertical timebases and CRT display control for today's color TV. Furthermore, all the user controls and manufacturer's set-up adjustments are under the control of the processor I^2C bus, eliminating the need for potentiometer controls. Chroma 4 offers an enormous variety of different options configurable in software, to cater to virtually any video standard or circumstance commonly met. The decoder section offers full multistandard capability, able to handle PAL, SECAM and NTSC standards. Practically all the filtering is carried out onboard the IC by means of sampled data filters, and requires no external components or adjustment.

Digital Interface

One of the most important features of Chroma 4 is the use of processor control to replace external potentiometer and filter adjustments. Great flexibility is possible using processor control, as each user can configure the software to suit their individual application. The circuit operates on a bidirectional serial data bus, based on the well known I^2C bus. This system is rapidly becoming a world standard for the control of consumer equipment.

I²C Bus

It is not within the scope of this data sheet to describe in detail the functioning of the I²C bus. Basically, the I²C bus is a two-wire bidirectional system consisting of a clock and a serial data stream. The write cycle consists of 3 bytes of data and 3 acknowledge bits. The first byte is the Chip Address, the second the Sub-address to identify the location in the memory, and the third byte is the data. When the address' Read/Write bit is high, the second and third bytes are used to transmit status flags back to the MCU.

Figure 2 shows a block diagram of the MC44001 Bus Interface/Decoder. To begin with, the start bit is recognized by means of the data going low during CLK high. This causes the Counter and all the latches to be reset. For a write operation, the Write address ($88) is read into the Shift Register. If the correct address is identified, the Chip Address Latch is set and at CLK 9 an acknowledge is sent.

The second byte is now read into the Shift Register and is used to select the Sub-address. At CLK 18 a Sub-address Enable is sent to the memory to allow the Data in the register to be changed. Also at CLK 18 another acknowledge is sent.

The third byte is now read into the Shift Register and the Data bussed into the memory. The Data in the Sub-address location already selected is then altered. A third acknowledge is sent at CLK 27 to complete the cycle.

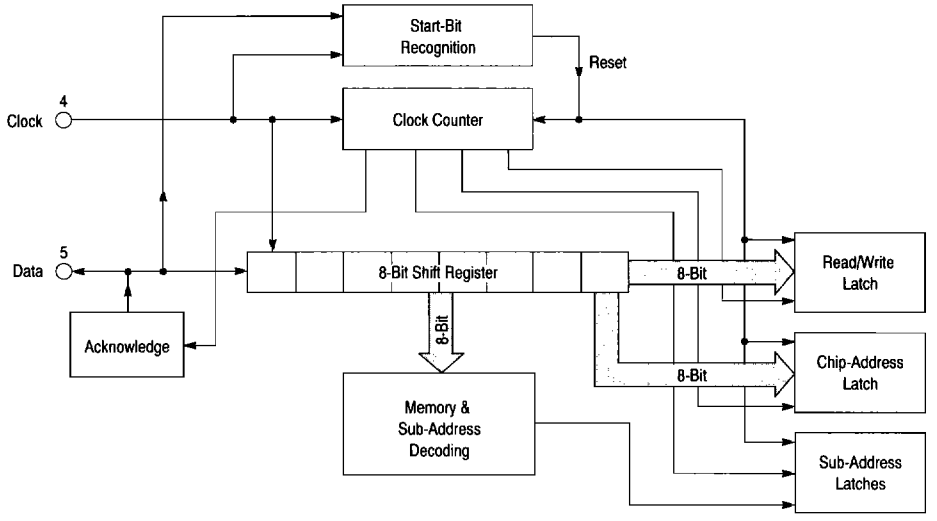
A Read address ($89) indicates that the MCU wants to read the Chroma 4 status flags. In this instance, the Read/Write Latch is set, causing the Memory Enable and Subaddress Enable to be inhibited, and the flags to be written onto the data line. Two of the status flags are permanently wired one-high and one-low (O.K. and Fault), to provide a check on the communication medium between the MC44001 and the MCU.

At start-up the Counter is automatically reset and the Data for each Sub-address is read in. Only after the entire memory contents has been transmitted, is Data 00 sent to start the Horizontal Drive.

It must be noted that Chroma 4 does not fully conform to the I²C bus specification. The protocol of the Chroma 4 bus differs from that of the I²C bus in the following respect:

When the device is in the Read mode, it starts with the Chip Address as always, but detects the Read bit high and sends an acknowledge (SDA pulled low). The first byte of data is transmitted to the MCU and an acknowledge is also given. The second byte is transmitted, again followed by an acknowledge. These two acknowledges are always transmitted, both in the Read and Write mode. In the I²C bus specification, it is normally the receiver device which provides the acknowledge, in order to indicate the validity of the transmission.

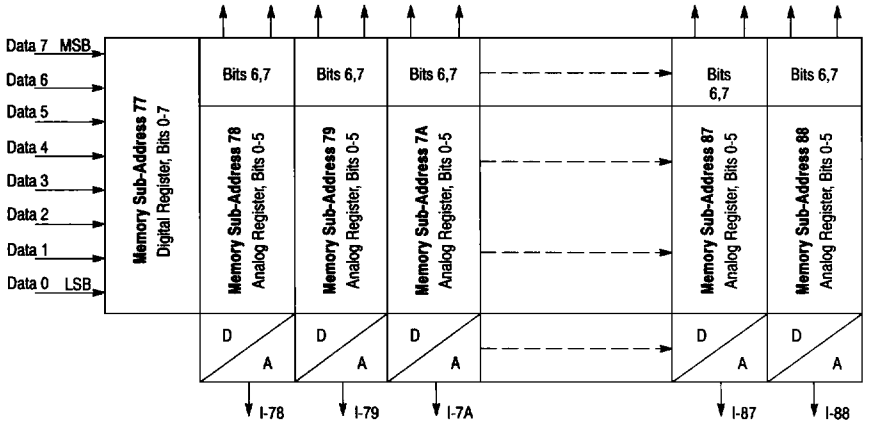
Figure 2. I²C Bus Interface and Decoder



Memory

Figure 3 shows a diagram of the MC44001 Memory Map. It has 18 bytes of memory which are located at hex sub-addresses 77 to 88. Sub-address 77 is used to set up the vertical timebase mode of the IC and for S-VHS switching, and consists of 8 separate data bits. The remaining 17 bytes use the least significant 6-bits as an analog control register. The contents of each are D/A converted, providing an analog control current which is distributed to the appropriate part of the circuit. Bits 6 and 7 are used singularly for switching control functions.

Figure 3. MC44001 Memory Map



Chroma Decoder

The main function of this section is to decode the incoming composite video, which may be in any of the PAL, NTSC or SECAM Standards, and to retrieve the luminance and color difference signals. In addition the signal filtering and luma delay line functions are carried out in this section by means of sampled data filters.

The entire decoder section operates in sampled data mode using clocks generated by external crystals. The oscillator, which is phase-locked in the usual way for PAL/NTSC modes, provides the clock function for the whole circuit. The crystals are selected by the MCU by means of a control bit. Only crystals appropriate to the standards which are going to be received need to be fitted. A 17.7 MHz crystal (4x PAL subcarrier) is used for PAL and SECAM systems (50 Hz, 625 lines); and 14.3 MHz (4x NTSC subcarrier) for the NTSC system (60 Hz, 525 lines). Nearly all the filters, together with the luma delay line and peaking, have been integrated, requiring no external components or any adjustment. The filter characteristics are entirely determined by the clocks and by capacitor ratios, and are thus completely independent of variations in the manufacturing process. The PAL/NTSC subcarrier PLL and ACC loop filters have not been integrated in order to facilitate testing. These filters consist of fixed external components.

Figure 4 is a block diagram of the main features of the chroma decoder. Selection is first made between the V1 and V2 inputs. These may be either normal composite video or separate luma and chroma which may enter the IC at either pin. Commands from the MCU are used to route the signals through the appropriate delay and filter sections. A composite video signal first passes through the sound trap filter which is of recursive design. With the 17.7 MHz crystal selected the following trap frequencies may be set by an MCU control word: 5.5 MHz, 6.0 MHz, 6.5 MHz. Next, the video enters the luma delay line and SECAM cloche filter. The PAL or NTSC chroma signal is separated out by a transversal filter receiving inputs from taps along the luma delay line, arranged in such a way that group delays in PAL and SECAM are nominally equalized. A second set of taps feeds another transversal filter whose function is to provide a chroma trap combined with luma channel peaking. In SECAM mode the trap frequency is dynamically steered to follow the instantaneous frequency of the chroma.

The high frequency luma may be peaked in 1 dB steps, up to a maximum of + 6 dB, by a control word from the MCU. Another control word is used to trim the delay in the luma channel. Five steps of 56 ns are possible, giving a total programmable delay of 280 ns. The resulting processed luma signal then proceeds to the color difference section. The luma output (Y1) is also made available at Pin 29, for use with frame store or other auxiliary function.

As all the delay and filter responses are determined by the clock, they automatically commute to the new standard when the crystal is changed over. Thus, when the 14.3 MHz clock is being used the chroma trap moves to 3.58 MHz, and the sound traps move to 4.5 MHz.

The filtered PAL/NTSC and SECAM chroma signals are decoded by their respective circuits. The PAL/NTSC decoder employs a conventional design, using ACC action for gain control and the common double balanced multipliers to retrieve the color difference signals. The SECAM decoder is discussed in a separate subsection.

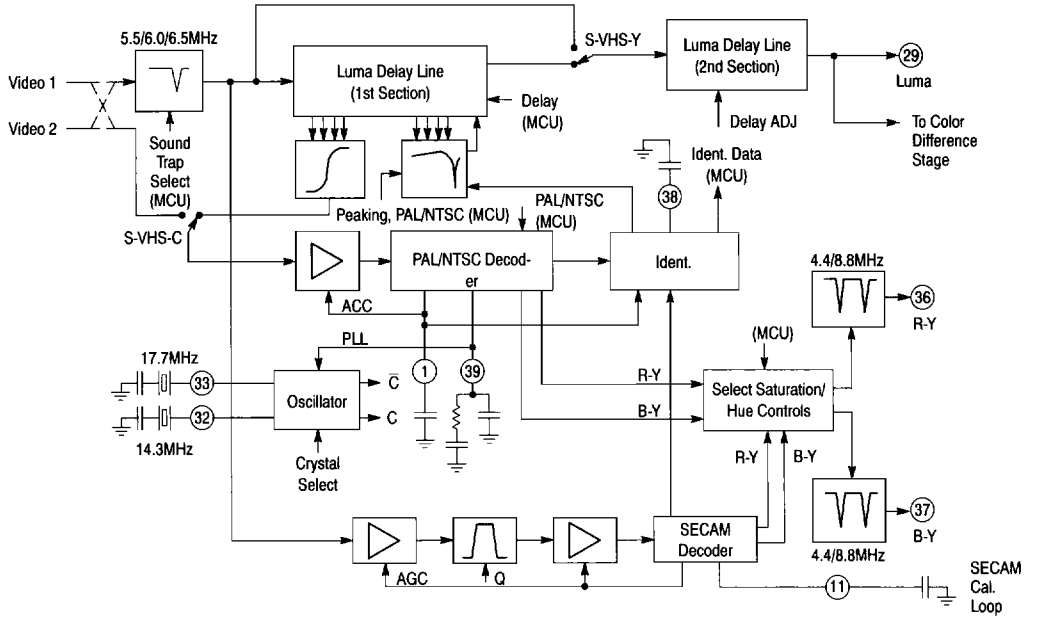
The identification signals from the PAL and SECAM decoders are set in opposition to each other, this being done as the best way to prevent misidentification between the two. The actual decision as to a signal's identity is made by the MCU based on data provided by 3 flags returned to it, namely: ACC Active, PAL Identified, and SECAM Identified.

This allows a maximum of flexibility, since the software may be written to accomodate many different sets of circumstances. For example, channel information could be taken into account if certain channels always carry signals in the same standard. Alternatively, if one standard is never going to be received, the software can be adapted to this circumstance. If none of the flags are on, color killing will be implemented by the MCU. This occurs if the net Ident Signal is too low, or if the ACC circuit is inactive due to too low a signal level.

The demodulated color difference signals now enter the Saturation/Hue control section, where selection is made between PAL/NTSC and SECAM outputs. The Saturation and Hue control is simply realized by altering the amplitudes of both color difference signals together. Hue control is only a requirement in NTSC mode and would not normally be used for other standards. The function is usually carried out prior to demodulation of the chroma by shifting the phase of the subcarrier reference, causing decoding to take place along different axes. In Chroma 4, Hue control is performed on the already demodulated color difference signals. A proportion of the R-Y signal is added or subtracted to the B-Y signal and vice-versa. This has the same effect as altering the reference phase. If desired, Chroma 4 can apply the Hue control to simple PAL signals.

After manipulation by the Saturation and Hue controls the color difference signals are finally filtered to reduce any remaining subcarrier and multiplier products. Before leaving the chip at Pins 36 and 37, the signals are blanked during line and frame intervals. The 64 µs chroma delay line is carried out by a companion device, the MC44140.

Figure 4. Chroma Decoder



SECAM Decoder

The SECAM signal from the high-pass filter enters tightly controlled AGC amplifiers wrapped around a cloche filter which is a sampled recursive type, with the AGC derived from a signal squarer. Next, the signal is blanked during the calibration gate period and a reference 4.43 MHz is inserted during this time. The SECAM signal is then passed through a limiter.

The frequency demodulator function is carried out by a frequency-locked-loop (F.L.L.). This consists of three components: a tracking filter, a phase detector and a loop filter. The center frequency of the tracking filter depends on three factors: internal R-C product, ADJUST voltage, TUNING voltage. The tracking filter is dynamically tuned by the TUNING feedback from the loop-filter forming the F.L.L. The ADJUST control calibrates the F.L.L. and compensates for variations in the R-C product. After the F.L.L. the color difference signals are passed to another block where several functions are carried out. The signals are de-emphasized and outputs are provided to the IDENT section. Another function of this section is to generate the I_{COMP} signal used for calibrating the F.L.L. This signal is blanked during the H-IG period to ensure that (R-Y) and (B-Y) output signals have a clean DC level for clamping purposes.

In addition, components are added to compensate for the R-C product, and tuning offsets are introduced during the active lines for FOR/FOB.

Calibration of the F.L.L. takes place during every field blanking interval, starting from field retrace and ending just before the SECAM vertical ident. sequence (bottles). The calibration current I_{CAL} is derived from I_{COMP} during the calibration gate (CAL) and integrated by an external capacitor on Pin 11. The resulting voltage V_{EXT} is then transformed to generate the ADJUST control voltage removing from the loop range most of the variations due to internal RC products and temperature.

Color Difference Stages

This stage accepts luminance and color difference signals, together with external R,G,B and Fast Commutation inputs and carries out various functions on them, including clamping, blanking, switching and matrixing. The outputs, consisting of processed R,G,B signals, are then passed to the Auto Gray Scale section.

A block diagram of this stage is shown in Figure 6. The Y2, R-Y, B-Y together with R, G and B are all external inputs to the chip. The Y1 signal comes from the decoder section. Each of the signals is back-porch clamped and then blanked. The Y2 and R,G,B inputs have their own simple sync separators, the output from which may be used as the primary synchronization for the chip by means of commands from the MCU.

The Fast Commutation is an active high input used to drive a high speed switch; for switching between the Y and color difference inputs and the R,G,B (text) inputs.

After blanking, the Y1 and Y2 channels go to the Luma Selector which is controlled by means of 2-bits from the MCU. From here the selected luma signal goes to the RGB matrix. The two color difference signals pass through a second saturation control, whose main function is described later. From here they go to a matrix in which G-Y is generated from the R-Y and B-Y, and lastly, to another matrix where Y is added to the three color difference signals to derive R,G,B.

The R,G,B inputs may take one of two different paths. They may either go straight to the output without further processing, or via a separate matrix and the second saturation control. The path taken is controlled in software. When the latter route is selected, the R,G,B signals undergo a matrix operation to derive Y. From this R-Y and B-Y are easily derived by subtraction from R and B; the derived color difference signals are then subjected to saturation control. The second saturation control may be disabled by the MCU if desired. This extra circuitry allows another feature to be added to the TV set, namely the ability to adjust the color saturation of the RGB inputs. This is not possible on present day receivers. After the saturation control the derived signals are processed as before.

Figure 5. SECAM Decoder

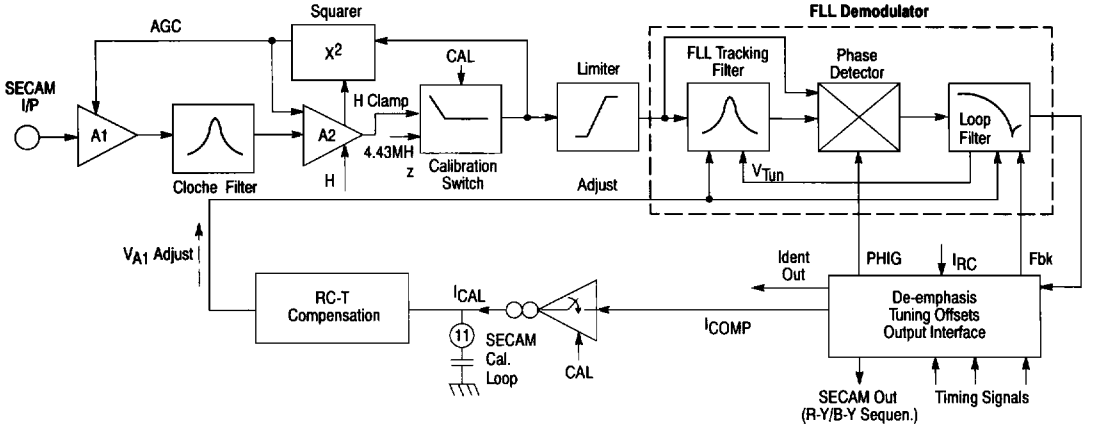
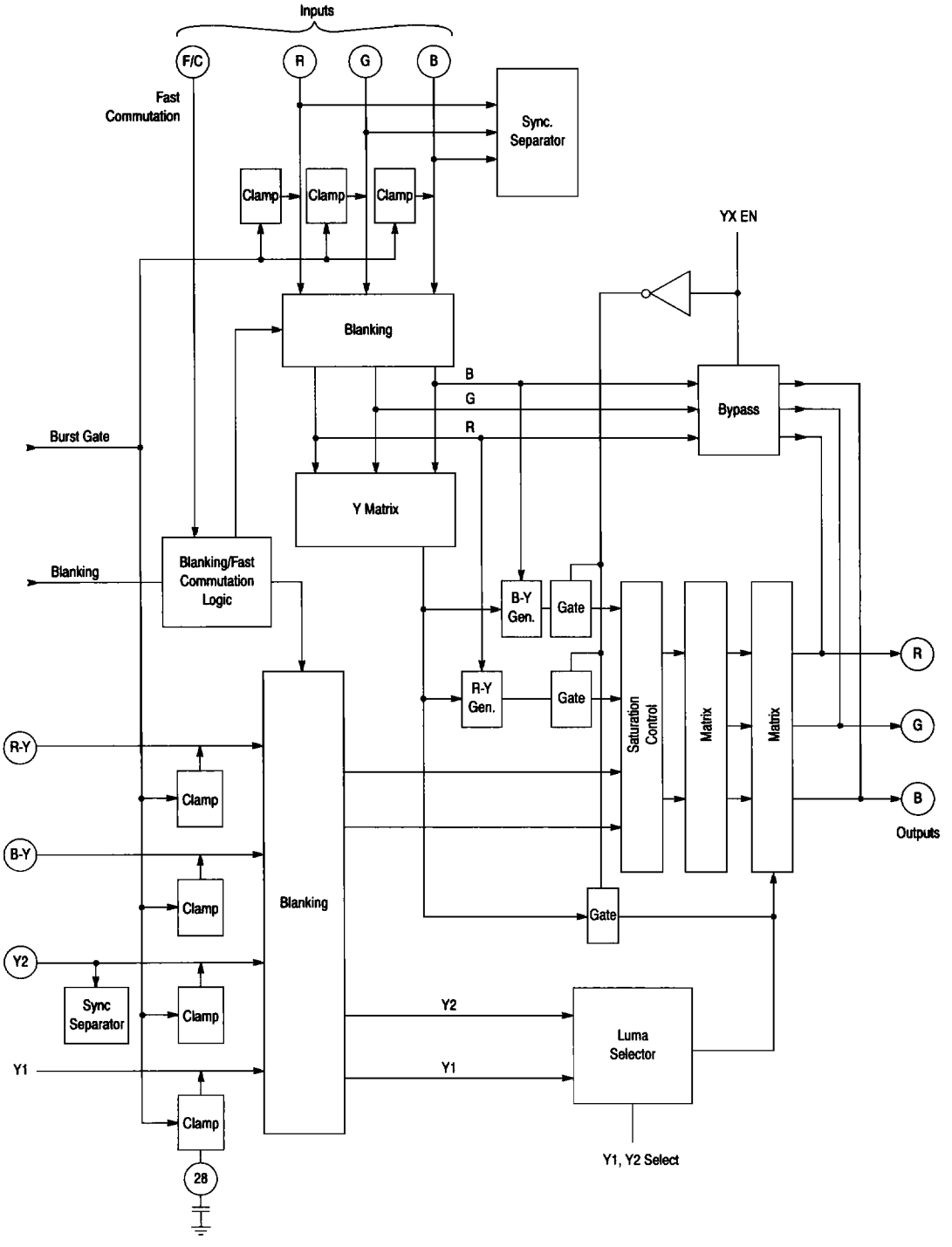


Figure 6. Color Difference Stages



Auto Gray Scale Control Loops

This section supplies current drives to the RGB cathode amplifiers and receives a signal feedback from them, proportional to the combined cathode currents. The current feedback is used to establish a set of feedback loops to control the DC and gain of the RGB drives. There are three loops to control the dark currents and another three to control the gains. During the field blanking period the video outputs are switched off and a set of references are inserted on three consecutive lines to control the R, G, and B outputs respectively. The white current reference pulses are sent first, followed by the black current reference pulses. Drives whose outputs are not being monitored are rendered nonconducting during this time.

A block diagram of the complete system is illustrated in Figure 7. Data words from the MCU which represent the RGB color temperatures selected at the factory, are stored in Latches 1,2,3 and D/A converted by DAC1,2,3 to reference currents. During, e.g., the red dark current set-up period, the reference current from DAC1 is selected and compared with the feedback current. The currents must match each other. If not, a current will flow in resistor R producing an error voltage. This is then buffered into comparators Comp1, 2 and is compared with voltage references Vref1 and Vref2. If the error voltage is greater than Vref1, Comp1 causes the counter to count up. If the error voltage is less than Vref2, Comp2 sends a count-down command. In this way a "deadband" is set up to prevent the outputs from continuously changing.

During Load the contents of the counter are loaded into Latch 6 (for red DC) and then D/A converted by DAC6. The resulting DC current is then applied as an offset to the red output amplifier, completing the loop. For white current set-up the same color temperature data is used but multiplied by a common factor. A common pulse representing a white level is applied to the RGB cathode amplifiers. The feedback loop adjusts the gains to establish a set of cathode currents scaled by a common factor to a set of black currents. Therefore, the image color will always be adjusted to match the black level color; i.e. gray scale tracking is ensured.

The Load/Backload sequencer is used to control which latch is being addressed at any given time by means of the timing signals input to it. The backload command sends the data from the appropriate latch to the Up/Down Counter, ready to be modified if necessary.

The Brightness control is affected by simply changing the DC pedestal of all three drives by the same amount, and does not form part of the feedback loop. The Contrast is adjusted to a set of values dependent on the level of the input pulse applied during the calibration time. This level is set by a control word from the MCU. Once the loops have stabilized under normal working conditions, they may be deactivated by means of a control bit from the MCU. When, however, any change is made to either contrast or brightness, the loops must be reactivated.

An extra loop has been included via Latch 4 and DAC 4, which operates during the field flyback time to compensate for offsets within the loop. This has the effect of counteracting any input offset from the Buffer/Amp and will also compensate for cathode leakage should this be needed.

A second output of the reference currents from DAC6, 8 and 10 are used to compare with preset limits, to ensure that the loops are working within their range of control. Should the limits be exceeded in either direction, flags are returned to the MCU to request that the G2 control be adjusted up or down as appropriate.

Horizontal Timebase

The horizontal timebase consists of a PLL which locks up to the incoming horizontal sync, and a phase detector and shifter whose purpose is to maintain the H-Drive in phase with the line flyback pulse.

Because of on-chip component tolerances, the free-running oscillator frequency cannot be set more accurately than ± 40%; whereas ± 5% would be a more appropriate figure for the sake of the line output stage. For this reason the free-running frequency is calibrated periodically by other means. Continuously during start-up and thence during two lines every field, the phase detector is disconnected from the VCO. A block diagram of the line timebase is given in Figure 8. The calibration loop consists of a frequency comparator driving an Up/Down Counter. The count is D/A converted to give a DC bias which is used to correct a 1.0 MHz VCO. The 1.0 MHz is divided by 64 to give line frequency and this is returned to the frequency comparator. This compares Fh from the VCO with a reference derived from dividing down the subcarrier frequency. Any difference in frequency will result in an output from the comparator, causing the counter to count up or down; and thus closing the loop.

A Coincidence Detector looks at the PLL Fh and compares it with the incoming H-sync. If they are not in lock, a flag is returned to the MCU. To allow for use with VCRs, the gain of the phase detector and the loop time constant may be switched by means of commands from the MCU.

Twice line frequency is output from the PLL which may be divided by either 1 or 2 depending on the command of the MCU. The x2 Fh will be used with Frame Store TV in the future. The phase of the Fh and flyback pulses are compared in a phase detector, whose output drives a phase shifter. A 6-bit control word and D/A converter are used to apply an offset to the phase detector giving a horizontal phase shift control. Also the phase of the horizontal drive may be shifted by 180 degrees with a control bit set by the MCU.

The presence of the horizontal flyback pulse is detected; if it is missing a warning flag is sent back to the MCU which can take appropriate action.

Vertical Timebase

The vertical timebase consists of two sections; a digital section which includes a vertical sync separator and standard recognition; and an analog section which generates a vertical ramp which may be modified under MCU control to allow for geometrical adjustments. A parabola is also generated and may be used for pin-cushion (E-W) correction and width control (see Figure 9).

The MC44001 uses a video sync separator which works using feedback, such that the threshold level of a comparator (slice level) is always maintained at the center of the sync pulse. Sync from any of the auxiliary inputs may also be used. The composite sync is fed to a vertical sync separator, where vertical sync is derived. This consists of a comparator,

up/down counter and decoder.The counter counts up when sync is high, and down when sync is low. The output of the decoder is compared with a threshold level, the threshold only being reached with a high count during the broad pulses in the field interval.

Initially the vertical timebase operates in Injection Lock mode, until a standard signal is recognized (525, 625), then it is switched to a Countdown mode. A standard recognition circuit is employed, which looks for a count of more or less than 576; the standard recognized is then indicated to the MCU. Commands from the processor may be used to force the timebase to operate only in Countdown mode at 525 or 625 lines, or stay in Injection Locked mode.

An adjustable current source is used to charge an external capacitor at Pin 6 to generate a vertical ramp. The amplitude of the ramp is varied according to the current source (Height), and is automatically adapted when the 525 standard is recognized by multiplying by 1.2. The Linearity control is achieved by squaring the ramp and either adding or subtracting a portion of it to the main linear current.

The final ramp with corrections added is then passed to a driver/amplifier and is output at Pin 7. The vertical ramp can be used to drive a separate vertical deflection power circuit with local feedback control. Vertical "S" Correction will then be made using fixed components within the feedback loop of the power op amp.

The reference ramp is squared to provide a pin-cushion correction parabola, developed across an external resistor at Pin 8. The parabola amplitude may be varied from zero to a maximum level set by the external resistor. The parabola itself is squared, giving and independent fourth order term (Corner Correction) whose level can also be varied; this is then added as a further modifying term to the E-W output. This latter correction is used for obtaining good corner geometry with flat-square tubes. A variable DC current is added to the parabola to effect a width control. Using a suitable power amplifier and a diode-modulator in the line output stage, the parabola may be used for E-W correction and dynamic width control. A further control is provided to shift the center point of the parabola up and down the screen (Parabola Tilt), to accommodate different CRTs. As with the vertical ramp output, an EHT correction is applied.

All of the vertical and horizontal signals are adjustable via 6-bit words from the MCU, and stored in latches. The adjustment controls available are:

Vertical Amplitude/Linearity/Breathing Correction
Parabola (E-W) Amplitude/Horizontal Amplitude/
Corner Correction, and Parabola Tilt

The Anode Current Sense at Pin 9 is also used as a beam current monitor. Two thresholds may be set, by the manufacturer, using external components. The first threshold sets a flag to the processor if beam current becomes excessive. The MCU could e.g. reduce brightness and/or contrast to alleviate the condition. The second threshold sets a flag warning of an overload condition where the CRT phosphor could be damaged. If such a condition were to arise, the processor would be programmed to shut down the PSU.

The vertical blanking period may be selected by means of a bit from the MCU to either 22 or 11 lines. The interlace may also be suppressed again under the control of the processor.

Vertical Countdown System

The MC44001 uses a countdown system to implement the vertical timebase function. Initially, the vertical timebase should reset to the Injection mode. This means that the timebase locks immediately to the first signal received, in exactly the same way as an old type injection locked timebase. A Coincidence Detector looks for counts of the right number (e.g., 625) and causes a 4-bit counter to count up. When there are 8 consecutive coincidences the vertical countdown is engaged, and the MSB of the counter is brought out to the set flag. Then the Auto Coundown mode should be set. Similarly, non-coincidences which will occur if synchronizing pulses are missing or in the wrong place, or if there is noise on the signals, cause the counter to count down. When the count goes back to zero, after 8 non-coincidences, the timebase automatically reverts to Injection Lock mode.

If it is known that lock will be lost (e.g., channel change), it is possible to jump straight into Injection Lock mode and not have to wait for the 8 consecutive non-coincidences. In this way the new channel will be captured rapidly. Once locked on to the new channel, "auto countdown" is then reselected by the MCU.

Under some conditions such as some VCRs in Search mode, it is possible to get signals having an incorrect number of lines, meaning that the countdown flag will go off because of successive non-coincidences. In these circumstances, if "auto countdown" is selected, the timebase will automatically lock to the signal in the Injection Lock mode. The fact that the flag is effectively saying that the vertical timebase is out of lock need not be a cause for major concern, since the horizontal timebase will still be locked to the signal, and has its own flag — "Horizontal out of lock". The vertical countdown and horizontal lock flags both perform an independent test for the presence of a valid signal. A logical OR function can be performed on the two flags, such that if either are present then by definition a valid signal is present.

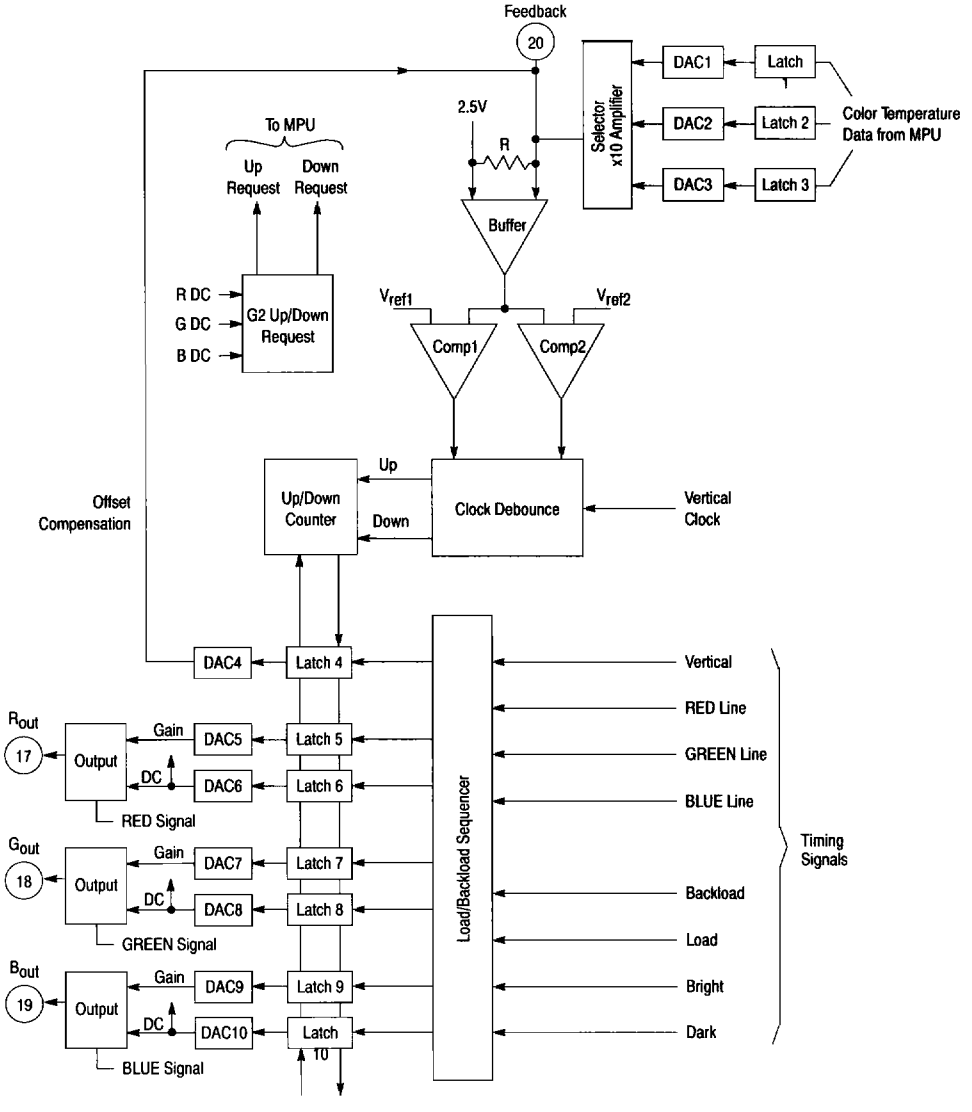
The vertical oscillator has end-stops set at two line-count decodes as given below:

$$50 \times 625 / 672 = 46.5 \text{ Hz (min)}$$
$$50 \times 625 / 512 = 61.0 \text{ Hz (max)}$$

These figures assume that the horizontal timebase is running at 15,625 Hz. When the vertical timebase is in Injection Lock mode the line counter reset is inhibited so that it ignores any sync pulses before a count of 512 is reached. This prevents any possible attempted synchronization in the middle of the picture. If the count reaches 672 lines then there is an automatic reset which effectively sets the lower frequency limit. The choice of these limits is a compromise between a wide window for rapid signal capture and a narrow window for good noise immunity.

It is also possible to run the timebase in 2V mode as there are decodes for 100 Hz (2 x 50 Hz) operation with upper and lower limits in proportion. This is, of course, intended to be used in conjunction with field and frame memory stores. The similar decodes which would be necessary to allow 120 Hz (2 x 60 Hz) operation have not, for the present, been implemented. Finally, the timebase can be forced into a count of either 625 or 525 by commands from the MCU; in this mode the input signal, if present, is ignored completely. If there is no signal present save for noise, then this feature can be used to obtain a stable raster.

Figure 7. Auto Gray Scale Control Loops



PIN FUNCTION AND EXTERNAL CIRCUIT REQUIREMENTS

The following section describes the purpose and function of each of the 40 pins on the MC44001. There is also an explanation of the external circuit component requirements for a practical application; a diagram of the small signal circuit will be found in Figure 10. One of the primary design aims for the MC44001 was to use the minimum number of external components, and where these are necessary to employ low cost and easily obtainable standard types. Thus for example, as all the video signal filtering is carried out on the IC there are no coils required whatsoever. The most common requirement is for AC coupling capacitors which are far too big to be integrated onto the chip. The time constants on certain pins are deliberately left as external components to facilitate testing and for fine tuning the performance.

ACC (Pin 1) – External filter used by ACC section. Normally a single 100 nF capacitor.

Video Inputs 1, 2 (Pin 2, 40) – Video inputs intended for a nominal 1.0 Vp-p input level of composite video. Separate Luma and Chroma components may also be used with these input pins. The external circuit requirement is for a series 100 nF and 1.0 kΩ. The input selection and adaptation for Y and C is carried out in software.

Figure 8. Horizontal Timebase

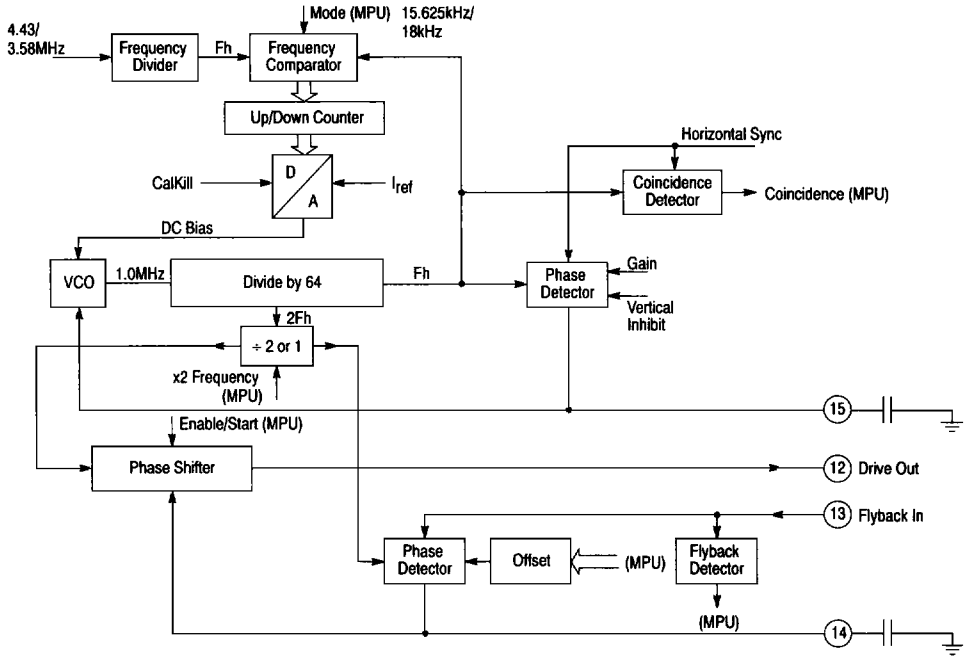
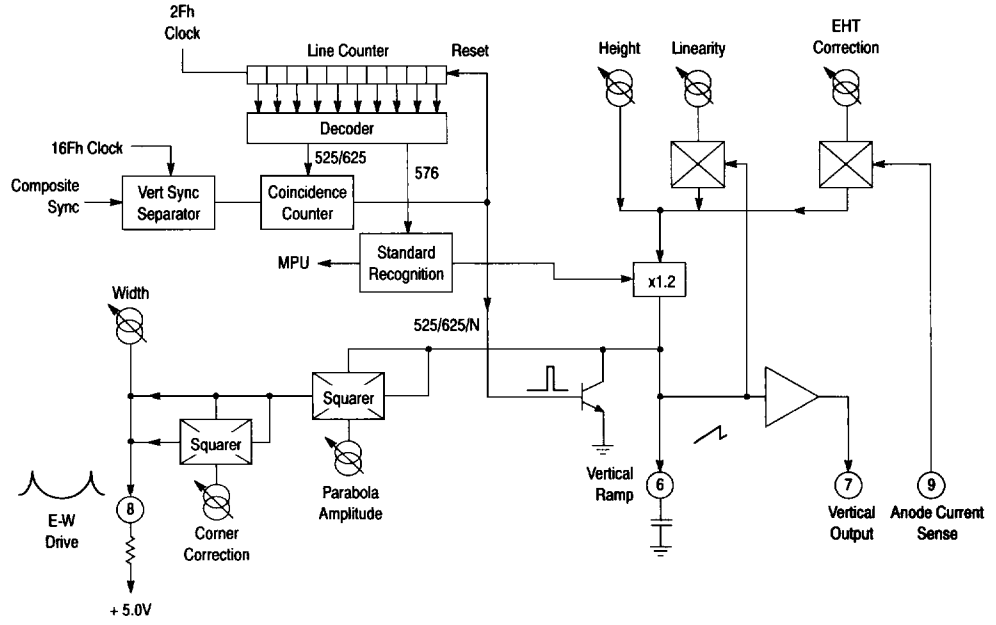


Figure 9. Vertical Timebase



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Reference Current (Pin 3) – Master reference current used throughout the IC. This is programmed by means of an external pull-up resistor, as onboard resistors are not sufficiently accurate. The designated current is 70 μA. This pin should be very well decoupled to ground to avoid picking up interference from the nearby I^2C bus inputs.

I^2C Clock (Pin 4) – I^2C bus clock input. This input can be taken straight into the IC, but in a real TV application it may be prudent to fit a series current limiting resistor nearby the pin in case of flashover.

I^2C Data (Pin 5) – I^2C data input. The comment above for Pin 4 also applies to this pin.

Vertical Ramp (Pin 6) – A current is used to charge an external capacitor connected to this pin, developing a voltage sawtooth with a field period.

Vertical Drive (Pin 7) – The sawtooth derived on Pin 6 is used to drive an external power amplifier vertical output stage. The amplitude and linearity of the output ramp are adjustable via the MCU.

Parabola (E-W) Drive (Pin 8) – A parabolic waveform derived by squaring the vertical ramp is used to drive an external power amplifier. In sets fitted with a diode modulator type line output stage, this provides Width Control and Pin Cushion Correction. The parabola is squared again to give a fourth order correction term required for flat square tubes. The E-W amplitude, DC level, Tilt and Corner Correction are all adjustable by means of the MCU. This is a current output and requires an external pull-up resistor to develop the voltage waveform.

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Anode Current (Pin 9) – Used as an anode current monitor whose purpose it is to: provide EHT compensation (antibreathing); and also warn of excessive and overload beam current conditions.

This pin is connected via 560 k series resistor to the bottom of the EHT overwinding. Thus increasing beam current will pull the voltage on this pin more negative. This change is sensed within the chip and used to apply a correction to the ramp and parabola amplitudes. With large beam currents, thresholds at +1 Vbe and – 2 Vbe set off warning flags to the MCU, which then has to take the appropriate action. The anode current levels at which these thresholds are reached are set up using fixed external resistors.

Grid 2 Control (Pin 10) – This consists of one of the MC44001 control registers which has been D/A converted and brought out from the IC as a current source. The current may be varied from 0 μA to 300 μA, and may be used for a number of auxiliary tasks, such as for Grid 2 control.

SECAM Calibration Loop (Pin 11) – A 100 nF capacitor on this pin is used for the SECAM Calibration Loop.

H-Drive (Pin 12) – Horizontal drive pulses having an approximately even mark-to-space ratio emerge from this pin. This is an open-collector output which can sink up to 10 mA. However, taking this much current is not recommended since there is no separate ground pin available which may be connected near the line O/P stage; noise could be injected into the signal ground on the IC. Therefore, with a transformer driven line output stage, this output has been designed to be used with an extra external transistor inverter between the IC and the line driver.

H-Flyback Input (Pin 13) – Flyback sensing input taken from the line output transformer. These pulses are used by the 2nd horizontal loop for H-phase control. A positive going pulse from 0 V to + 5.0 V amplitude is needed for correct operation. The internal impedance of the pin is about 50 kΩ. An external attenuating series resistor will also be needed.

H-Loop 2 Filter (Pin 14) – A simple external filter consisting of a 100 nF capacitor for the 2nd horizontal loop.

H-Loop 1 Filter (Pin 15) – Horizontal PLL loop time constant. The value of RC time constant is selected with external components to give a smooth recovery after the field interval disturbance.

Signal Ground (Pin 16)

R,G,B Outputs (Pin 17, 18, 19) – The R,G,B drives are current rather than voltage due to the limited headroom available with the 5.0 V supply line. The outputs themselves consist of open-collector transistors and these are used to drive the virtual ground point of the high voltage cathode amplifiers.

Feedback (Pin 20) – Current feedback sense derived from the video output amplifiers. The currents from all three guns are summed together as each is driven sequentially with known current pulses during the field interval. This feedback is then compared with internally set-up references. A low value ceramic capacitor to ground may be fitted close to this pin to help stabilize the control loops.

A secondary function of this pin is for peak beam current limiting. When the feedback voltage during picture time becomes too great (i.e., too high beam current), a threshold at V_{CC} + 2 Vbe is exceeded at which time a flag is sent to the MCU. The MCU then has to carry out the function of peak beam limiter by e.g. reducing contrast until the flag goes off. The threshold current is set externally with a fixed resistor value.

Fast Commutate (Pin 21) – A very fast active high switch (transition time 10 ns). Used with text on the R,G,B inputs, for overlaying text on picture. This hardware switch may be enabled and disabled in software.

R,G,B Inputs (Pins 22, 23, 24) – These external input signals are AC coupled into the IC via 100 nF capacitors and are clamped. The inputs have a 1.0 kΩ impedance and should be driven with 700 mVp-p signal levels.

Y2 Input (Pin 25) – Auxiliary external input to the MC44001. The pin has a 1.0 kΩ impedance and should be driven with 700 mVp-p of luminance signal. The signal must be AC coupled via an external 100 nF coupling capacitor, and is clamped internally.

B-Y and R-Y Inputs (Pin 26, 27) – Corrected color difference inputs from the MC44140. The signals are AC coupled to the MC44001 color difference section and are clamped. The input impedance is of the order of 1.0 kΩ.

Y1 Clamp (Pin 28) – External capacitor used by the circuit which clamps the Y1 signal output on Pin 29.

Y1 Output (Pin 29) – The luminance, after passing through the filter and delay line/peaking sections, is made available on this pin.

System Select (Pin 30) – A DC level output controlled in software. Used by the MC44140 for system selection.

Sandcastle (Pin 31) – A special timing pulse derived in the MC44001 for use by the MC44140.

Crystal (Pin 32, 33) – A 14.3 MHz crystal is required at Pin 32 for NTSC decoding, and a 17.7 MHz crystal is required at Pin 33 for PAL and SECAM decoding. Either crystal may be omitted if the application does not involve the associated signals. The appropriate crystal is selected by the MCU.

The crystals are parallel-driven, and require an external load capacitor of 20 pF to 30 pF. *Only crystals intended for VCO operation should be used.* The selected crystal's frequency is made available to the MC44140 by means of the external capacitor divider.

+ 5.0 V Supply (Pin 35) – Supply line, nominally + 5.0 V requiring about 120 mA. The actual voltage should be in the range of 4.75 V to 5.25 V for usable results. It is recommended to decouple the supply line using a small ceramic capacitor mounted close to the supply and ground pins.

Ground (Pin 34)

B-Y and R-Y Outputs (Pin 36, 37) – Demodulated color difference outputs. These signals are AC coupled to the MC44140 for correction and delay with PAL and SECAM, respectively. Signal levels up to a maximum of 1.0 Vp-p may be expected.

Ident (Pin 38) – External filter used by R-Y indent circuit. The filter normally consists of a single capacitor (47 nF) whose value is a compromise between rapid identification and noise rejection.

OSC Loop Filter (Pin 39) – External time constant for chroma PLL. The crystal reference oscillator is phase-locked to the incoming burst in PAL and NTSC. A low value ceramic capacitor, for good noise immunity, is normally placed in parallel with a much longer RC time constant. The PLL pull-in range is reduced when the time constant on the pin is made bigger; allowing this function to be optimized by the user.

CONTROL FUNCTIONS

General Description

As already related in the circuit description, the MC44001 has a memory of 18 bytes. All, except Sub-address 77 and 7F, use the 6 least significant bits (64 steps) as an analog control register with D/A converters within the memory section. The remaining bits are controlled individually for switching of numerous functions. Table 1 gives a listing of all the memory registers and control bits. An explanation of the function of the 16 analog control registers is given below.

Vertical Amplitude – Changes the amplitude of the vertical ramp available on Pin 7.

Vertical Breathing Correction – A correction is applied to the vertical ramp amplitude in a sense opposite to the picture expansion and contraction produced by changes in beam current. This register alters the sensitivity of the beam current sensing and hence the size of correction applied for a given change in beam current.

Parabola Amplitude – Changes the amplitude of the E-W output parabola developed across an external pull-up resistor at Pin 8.

Parabola Tilt – Shifts the point of inflection of the E-W parabola from side to side along the time axis. Also known as *keystone correction.*

Vertical Linearity – The vertical ramp is multiplied by itself to give a squared term, a part of which is either added or subtracted to the linear ramp as determined by this register.

Corner Correction – An independent 4th order term which is subtracted from the E-W parabola to achieve correct geometry with flat square tubes.

Horizontal Amplitude – A variable DC offset applied to the E-W output parabola on Pin 8.

D/A Output – A variable DC current output which may be used to drive auxiliary external circuitry under I^2C bus control.

Horizontal Phase Control – Applies a variable phase offset to the horizontal drive pulse at Pin 15 providing for a picture centering control.

B, G, R Temperature – These controls set up the current reference pulses used when sampling the beam current during field interval. The data is fixed by the TV manufacturer when setting up the CRT for correct Gray Scale tracking.

(All the above registers are for use during the test and setting up procedures; the remaining 4 registers are also user controls.)

Contrast – During bright sample time during the field interval this control varies the level of the current pulses injected into the R,G,B channels, so altering the picture contrast.

Brightness – A variable current pedestal which is added to the three drives during active picture time.

Saturation – A variable gain control for the two color difference signals (0 to 140%). There are two such controls within the MC44001, and this control acts on them both.

Hue – Achieved by mixing a proportion of one color difference signal into the other.

Individually Adjustable Control Bits – These consist of all Sub-address 77 and bits 6 and 7 of Sub-addresses 78 to 88. Some of these are used individually to control single functions requiring just on/off switching; and some are arranged into 2 or 3-bit words (e.g., luma peaking). A list of control words and truth tables for these may be found in Table 2.

CA1, CB1 – Used to change the mode of operation of the vertical timebase to either injection lock or auto countdown, or to force it into 525 or 625 lines. Just prior to changing channel, the vertical timebase can be switched to injection lock mode and when a new channel is captured, the timebase is switched back to auto mode. In this way there is no delay in locking onto the new channel and hence no picture roll. If there is no valid signal being received the display can be stabilized by forcing the timebase into 525 or 625 lines.

IC1, IF1 – These bits are used to suppress the field interlace, which can be scanned in the nearest even or odd half line.

$\overline{H1}$, $\overline{V1}$ – Selects the type of SECAM ident when operating in this mode. Either vertical ident bursts or back porch ident can be selected individually, or ident can be taken from a combination of the two.

SSA, SSB, SSC – Used to set the DC level of the System Select output from the MC44001, Pin 30. This output is used by the MC44140 delay line in turn for changing between PAL, NTSC, SECAM and external modes of operation. In effect the MC44140 is being controlled by the I^2C bus via the MC44001.

Figure 10. Basic Small Signal Circuit

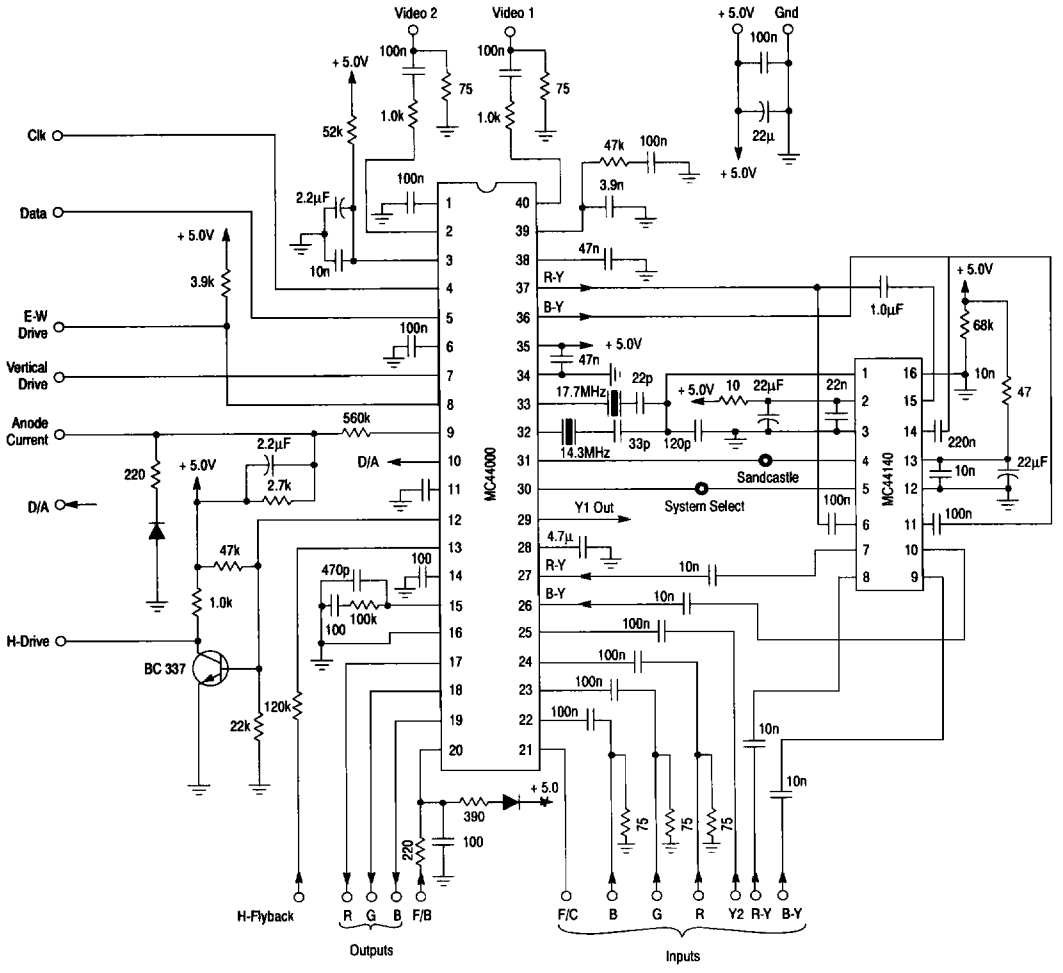

Table 1. Control Data

HEX Sub-address	MSB	Data Byte						LSB
77	S-VHS Y	S-VHS C	FSI	BAI	ICI	IFI	CBI	CAI
78	INTSEL	CALKILL	Vertical Amplitude					
79	HI	VI	Vertical Breathing Correction					
7A	XS	SSD	Parabola Amplitude					
7B	T1	T2	Parabola Tilt					
7C	SSC	SSA	Vertical Linearity					
7D	P1	SSB	Corner Correction					
7E	P3	P2	Horizontal Amplitude					
7F	D3	D1	Reserved					
80	D EN	D2	D/A Output					
81	Y2 EN	Y1 EN	Horizontal Phase Control					
82	TEST	YX EN	Blue Temperature					
83	Not Used	VCR	Green Temperature					
84	FILT	NORM	Red Temperature					
85	BRI EN	2x Fh	Contrast					
86	SSE	H EN	Brightness					
87	SS1	SAT2 EN	Saturation					
88	V1/V2	SS2	Hue					
00		Dummy – If H EN, then starts H timebase						
FF		Dummy – Resets peak beam limit flag						

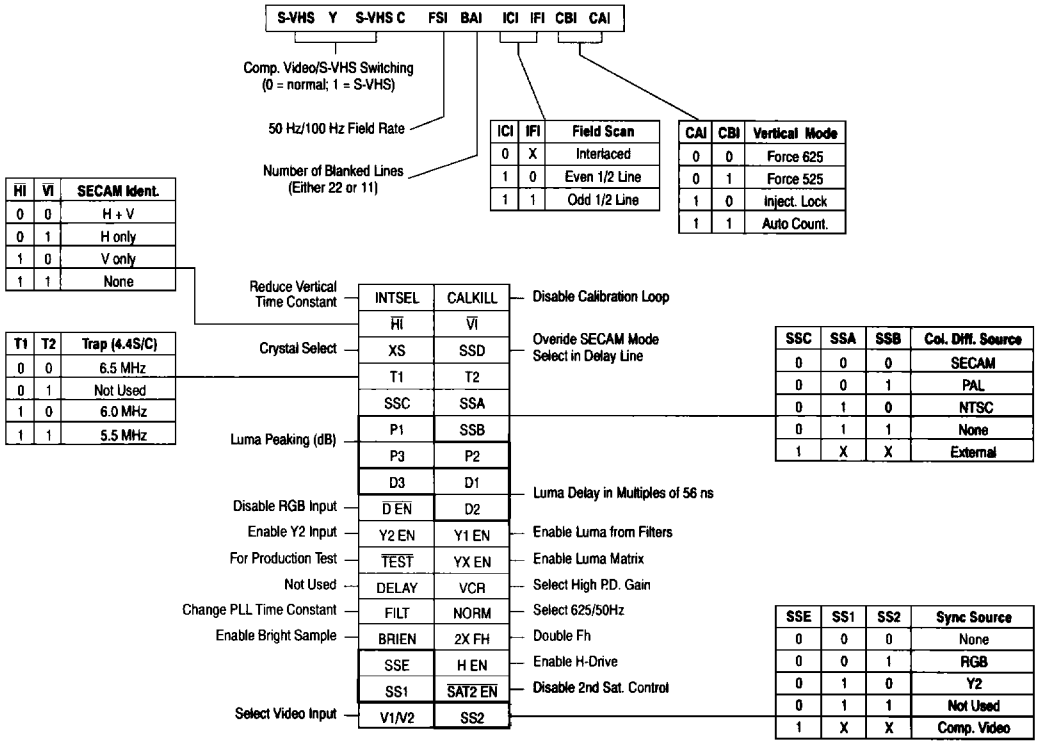

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Table 2. Control Bit Truth Tables

CAI	CBI	Sync Mode
0	0	Force 625
0	1	Force 525
1	0	Injection Lock
1	1	Auto Countdown

ICI	IFI	Field Scan
0	X	Interlaced
1	0	Even Up 1/2 Line
1	1	Odd Up 1/2 Line

$\overline{HI}$	$\overline{VI}$	SECAM Ident.
0	0	H + V
0	1	H only
1	0	V only
1	1	None

T1	T2	Trap*
0	0	6.5 MHz
0	1	Not Used
1	0	6.0 MHz
1	1	5.5 MHz

SSC	SSA	SSB	Col. Diff. Source
0	0	0	SECAM
0	0	1	PAL
0	1	0	NTSC
0	1	1	None
1	X	X	External

SSE	SS1	SS2	Sync Source
0	0	0	None
0	0	1	RGB
0	1	0	Y2
0	1	1	Not Used
1	X	X	Comp. Video

P2	P1	P3	Luma Peak (dB) @ 3.0 MHz *
0	0	0	8.5
0	0	1	8.0
0	1	0	7.2
0	1	1	6.3
1	0	0	5.4
1	0	1	3.8
1	1	0	2.3
1	1	1	0.0

D1	D2	D3	Approx. Luma Delay (ns)*
0	0	0	525
0	0	1	581
0	1	0	637
0	1	1	693
1	0	0	749
1	0	1	805
1	1	0	749
1	1	1	805

*Values given with 17.7 MHz crystal selected. Frequencies and delay step size change proportionately when the 14.3 MHz crystal is selected.

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SSE, SS1, SS2 – These 3 bits select the signal input from which the timebase synchronization is taken. The composite video input has a high quality sync separator which has been designed to cope with noise and interference on the video; the RGB and Y2 inputs have simple single sync separators which may also be used for synchronization.

T1, T2 – To select the center frequency of the sound trap. Either 5.5 MHz, 6.0 MHz, or 6.5 MHz center frequencies are available.

P1, P2, P3 – These 3 bits are used to adjust the luma peaking value.

D1, D2, D3 – These 3 bits are used to adjust the luma delay value.

The remaining control bits are used singularly and are listed as follows:

S-VHS Y – Selects between luminance from chroma trap/peaking section, and separate luminance which bypasses this filter section.

S-VHS C – In one mode selects chrominance from the takeoff filter which forms part of the luma delay line. The other mode accepts separate chrominance directly for the input.

FSI – Selects either 50 Hz or 100 Hz field rate. When bit is low 50 Hz operation is selected. Not usable with NTSC.

BAI – Either 22 or 11 lines may be blanked using this bit.

INTSEL – The vertical sync separator operates by starting a counter counting up at the beginning of each sync pulse, a field pulse being recognized only if the counter counts up to a sufficiently high value. The control bit INTSEL is used in taking the decision as to when a vertical sync pulse has been detected. When low, the pulse is detected after 8.0 µs; when high after 24 µs. This may find application with anti-copy techniques used with some VCRs, which rely on a modified or corrupted field sync to allow a TV with a short time constant to display a stable picture. However, a VCR having a longer time constant will be unable to lock to the vertical.

CALKILL – Enables or disables the horizontal calibration loop. The loop may be disabled so long as the horizontal timebase is locked to an incoming signal.

XS – Is used to change between the two external crystal positions (Pins 32 and 33).

SSD – Can be used to override SECAM mode in the delay line. When low, SECAM mode is enabled.

$\overline{\text{D EN}}$ – Enables or disables the RGB Fast Commutation switch for the RGB inputs. When low, RGB inputs are enabled.

Y1 EN – Switches Y1 through to the color difference stage.

Y2 EN – Switches Y2 through to the color difference stage.

$\overline{\text{Test}}$ – When bit is low, enables continuous sampling by the RGB output control loops throughout the entire field period. Used only for testing the IC.

YX EN – Enables the luma matrix when the 2nd saturation control is selected. Used in conjunction with SAT2 EN.

VCR – Is used to change the gain of the horizontal phase detector, e.g., when locking onto a new channel and operation with VCR.

FILT – Controls the time constant of the horizontal PLL. The long time constant is useful for VCR or other non-broadcast quality signals.

Norm – Alters the division ratio for the reference frequency used by the horizontal calibration loop. Always used when changing between 14.3 MHz and 17.7 MHz crystals.

BRI EN – Used to switch on or off the "bright" sampling pulses used by the RGB output loops. This feature was originally introduced to prevent any backscatter from these three bright lines in the field interval from getting into the picture. Must be enabled when adjusting to any of Contrast or Red, Green and Blue color temperatures.

2x Fh – Line drive output is either standard 15.625 kHz (15.750 kHz) or at double this rate.

H EN – Control bit enables horizontal drive pulse. This is normally done automatically after the values stored in the MCU nonvolatile memory have been read into the MC44001 memory.

SAT2 EN – When low enables operation of 2nd saturation control. Used in conjunction with YX EN.

V1/V2 – To select between Video Inputs 1 and 2.

Table 3. Control Bit Functions

Bits	Bit Low	Bit High
V1/V2	Video I/P 2 Selected	Video I/P 1 Selected
SAT2 EN	Second SAT Control Enabled	Second SAT Control Disabled
H EN	H-Drive Enabled	H-Drive Disabled
2x FH	H-Drive: 1X Fh	H-Drive: 2x Fh
BRI EN	"Bright" Sample Switched Off	"Bright" Sample Switched On
Norm	625/50 Hz	525/60 Hz
FILT	H Phase Detector Short Time Constant	H Phase Detector Long Time Constant
VCR	Low H Phase Detector Gain	High H Phase Detector Gain
YX EN	Disable Luma Matrix (2nd SAT Control)	Enable Luma Matrix (2nd SAT Control)
Test	Video O/Ps Sampled Continuously	Video O/Ps Sampled Once Per Field
Y1 EN	Luma From Filters Switched Off	Luma From Filters Switched On
Y2 EN	EXT Luma Input Switched Off	EXT Luma Input Switched On
D EN	RGB Inputs Enabled	RGB Inputs Disabled
SSD	SECAM Mode Select Enabled	SECAM Mode Select Disabled
XS	Pin 33 Crystal Selected	Pin 32 Crystal Selected
CALKILL	H Calibration Loop Enabled	H Calibration Loop Disabled
INTSEL	Fast Vertical Time Constant Selected	Slow Vertical Time Constant Selected
BAI	22 Blanked Lines Selected	11 Blanked Lines Selected
FSI	50 Hz Field Rate Selected	100 Hz Field Rate Selected
S-VHS C	Chroma From Take Off Filter Selected	Direct Chroma From I/P Selected
S-VHS Y	Luma From Notch/Peak Delay Selected	Luma By Passing Notch/Peak Delay

FLAGS RETURNED BY THE MC44001

When the Address Read/Write bit is high the last two bytes of I^2C data are read by the MCU as status flags; a listing of these may be found in Table 4. The MC44001 is designed to be part of a closed-loop system with the MCU; these flags are the feedback mechanism which allow the MCU to interact with the MC44001.

A brief description of each of the flags, its significance and possible uses are given below.

Table 4. Flags Returned

Clock #	Flag (Bit High)
10	Horizontal Flyback Present
11	Horizontal Drive Enabled
12	Horizontal Out Of Lock
13	Excess Average Beam Current
14	Less Than 576 Lines
15	Vertical Countdown Engaged
16	Overload Average Beam Current
17	Reserved
18	(Acknowledge)
19	Grid 2 Voltage Up Request
20	Grid 2 Voltage Down Request
21	OK
22	Fault
23	ACC Active
24	PAL Identified
25	SECAM Identified
26	Excess Peak Beam Current
27	(Acknowledge)

Horizontal Flyback Present – A sense of the horizontal flyback is taken via a current limiting series resistor from one of the flyback transformer secondaries to Pin 13. This is used for the H-phase shift control, but the presence of the pulse is also flagged to the MCU. Should the flag be missing after the chassis has been started up then the MCU would have to shut down the set immediately.

Horizontal Drive Enabled – Indicates that the horizontal drive pulse output at Pin 15 has been enabled. This occurs after the stored values in the nonvolatile memory have been transferred to the MC44001 memory.

Horizontal Out of Lock – This flag is high when no valid signal is being received by the MC44001. Possible action in this case would be to change the phase detector gain and time constant bits to ensure rapid capture and locking to a new signal.

Excess Average Beam Current – Is one of two conditions whose threshold levels are determined by an external component network connected to beam current sensing Pin 9. This condition indicates an excess beam current as compared to the manufacturer's set maximum level during normal usage. A typical response to this warning indicator would be for the MCU to reduce the brightness and/or contrast.

Less Than 576 Lines – Output from the line counter in the vertical timebase. If there is a count of less than 576 this is indicative of a 525 line system being received. If the flag is low then a 625 line system is being received. This information can be used as a part of an automatic system selection software.

Vertical Countdown Engaged – The vertical timebase is based on a countdown system. The timebase starts in Injection Lock mode and when vertical retrace is initiated a 4-bit counter is set to zero. A coincidence detector looks for counts of 625 lines. In Auto mode each coincidence causes the counter to count up. When eight consecutive coincidences are detected the countdown is engaged. The MSB of the counter is used to set this flag to the processor.

Overload Average Beam Current – This is the second threshold level which is set by the external component network on Pin 9. The flag warns of an overload in anode current which could damage the CRT if allowed to continue. Appropriate action in this case is therefore to shut down the set.

Grid 2 Voltage Up/Down Requests – These flags indicate when the RGB output loops are about to go out of the control range necessary for correct gray scale tracking.

OK and Fault – These two flags are included as a check on the communication line between the MCU and MC44001. The OK flag is permanently wired high and Fault is permanently wired low. The MCU can use these flags to verify that the data received is valid.

ACC Active – This flag is high when there is a sufficient level of burst present in PAL and NTSC modes during the video back porch period. The flag goes low when the level of burst falls below a set threshold or if the signal becomes too noisy. The flag is used to implement a software color killer in PAL and NTSC and is also available for system identification purposes. Since in SECAM there is line carrier present during the gating period, it is quite likely that the ACC will be on, or will flicker on and off in this mode.

*** PAL Identified** – Recognizes the line-by-line swinging phase characteristic of the PAL burst. When this flag is on together with the ACC flag, this is positive identification for a PAL signal.

*** SECAM Identified** – Senses the changing line-by-line reference frequencies (Fo1 and Fo2) present during the back porch period of the SECAM signal. This flag alone provides identification that SECAM is being received.

* These two flags are set in opposition to one another such that they can never both be on at the same time. This has been done to try to prevent misidentification from occurring. Often it is very difficult to distinguish between PAL and SECAM especially when broadcast material has been transcoded, sometimes badly, leaving e.g. large amounts of SECAM carrier in a transcoded PAL signal (also often with noise). With this method the strongest influence will win out making a misidentification much less likely.

Excess Peak Beam Current – A voltage threshold is set on the beam current feedback on Pin 20, which is also used for the RGB output loops for current sampling. When the threshold is reached the flag is set, indicating too high a peak beam current which may be in only a part of the screen. The response of the MCU might be to reduce the contrast of the picture. This flag together with the excess average beam flag already described perform the function of beam limiting. The exact way in which this is handled is left to the discretion of the user who will have their own requirements, which may be incorporated by the way in which the software is written.

READING AND WRITING TO THE MC44001

Flag reading may be done at any time during a field. However, writing to the MC44001 must be restricted to certain times. If writing of new data is done during the middle of a field, a disturbance will be seen on the screen, particularly for the four user controls. While writing during the vertical interval may appear to be the obvious solution for this, there is a limited time available due to the contrast control function which is carried out with RGB sampling loops during this interval. Writing during this particular time can cause the sampling loops to become unstable.

The time available for writing new data is approximately 1.2 ms from the beginning of the field flyback pulse to the beginning of the RGB sampling. It is only the third byte (data byte) which is restricted to this time interval. The first two bytes may be sent previous to this, or also during this time.

Table 5. System Identification

Flags From Chroma 4				Crystal (MHz)	Standard Selected By MCU
<576 Lines	ACC On	PAL	SECAM		
0	0	0	0	17.7	Kill
0	0	0	1	17.7	SECAM
0	0	1	0	17.7	Kill
0	0	1	1	17.7	I^2C Bus Error
0	1	0	0	17.7	Kill
0	1	0	1	17.7	SECAM
0	1	1	0	17.7	PAL
0	1	1	1	17.7	I^2C Bus Error
1	0	0	0	14.3	Kill
1	0	0	1	14.3	Kill
1	0	1	0	14.3	Kill
1	0	1	1	14.3	I^2C Bus Error
1	1	0	0	14.3	NTSC
1	1	0	1	14.3	NTSC
1	1	1	0	14.3	NTSC
1	1	1	1	14.3	I^2C Bus Error

NOTES: 1. The table above can be used for color standard selection between the normal PAL (I, BG), SECAM (L, BG) and NTSC (3.58 MHz – M) Standards. To detect the hybrid VCR standard (525 lines with 4.4 MHz chrominance) would entail switching back to the 17.7 MHz crystal in the event of there being no flags present with the 14.3 MHz crystal.

2. Chroma 4 could also be used for the PAL M & N Standards that are used in some parts of South America, but because the subcarrier frequencies used differ by some kHz from the normal, crystals with a different center frequency would be required.

Table 6. Mode Definitions

Mode Selected	Control Bits				
	XS*	NORM*	SSA	SSB	SSC
Kill (17.7 MHz)	0	0	1	1	0
Kill (14.3 MHz)	1	1	1	1	0
PAL (I, BG)	0	0	0	1	0
SECAM	0	0	0	0	0
NTSC (M)	1	1	1	0	0

*Control bits XS and NORM are always changed together.

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