

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

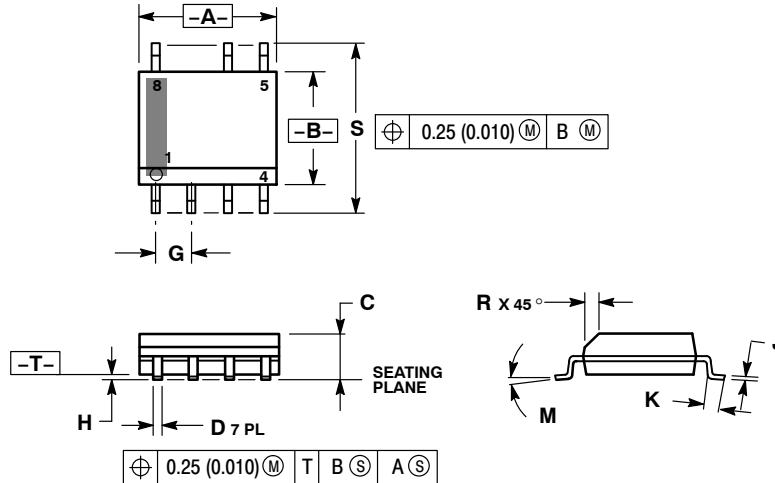
ON Semiconductor®



SCALE 1:1

SOIC-7
CASE 751U-01
ISSUE E

DATE 20 OCT 2009

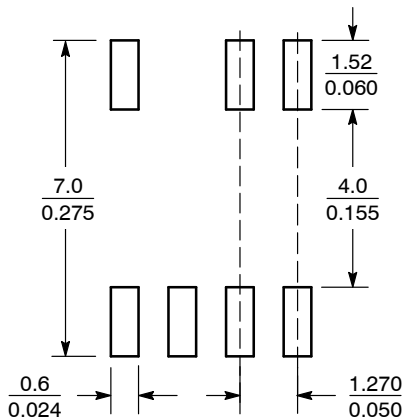


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

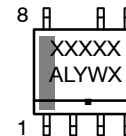
SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



- XXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98AON12199D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	7-LEAD SOIC	PAGE 1 OF 3

SOIC-7
CASE 751U-01
ISSUE E

DATE 20 OCT 2009

STYLE 1:

- PIN 1. EMITTER
- 2. COLLECTOR
- 3. COLLECTOR
- 4. EMITTER
- 5. EMITTER
- 6.
- 7. NOT USED
- 8. EMITTER

STYLE 2:

- PIN 1. COLLECTOR, DIE, #1
- 2. COLLECTOR, #1
- 3. COLLECTOR, #2
- 4. COLLECTOR, #2
- 5. BASE, #2
- 6. EMITTER, #2
- 7. NOT USED
- 8. EMITTER, #1

STYLE 3:

- PIN 1. DRAIN, DIE #1
- 2. DRAIN, #1
- 3. DRAIN, #2
- 4. DRAIN, #2
- 5. GATE, #2
- 6. SOURCE, #2
- 7. NOT USED
- 8. SOURCE, #1

STYLE 4:

- PIN 1. ANODE
- 2. ANODE
- 3. ANODE
- 4. ANODE
- 5. ANODE
- 6. ANODE
- 7. NOT USED
- 8. COMMON CATHODE

STYLE 5:

- PIN 1. DRAIN
- 2. DRAIN
- 3. DRAIN
- 4. DRAIN
- 5.
- 6.
- 7. NOT USED
- 8. SOURCE

STYLE 6:

- PIN 1. SOURCE
- 2. DRAIN
- 3. DRAIN
- 4. SOURCE
- 5. SOURCE
- 6.
- 7. NOT USED
- 8. SOURCE

STYLE 7:

- PIN 1. INPUT
- 2. EXTERNAL BYPASS
- 3. THIRD STAGE SOURCE
- 4. GROUND
- 5. DRAIN
- 6. GATE 3
- 7. NOT USED
- 8. FIRST STAGE Vd

STYLE 8:

- PIN 1. COLLECTOR (DIE 1)
- 2. BASE (DIE 1)
- 3. BASE (DIE 2)
- 4. COLLECTOR (DIE 2)
- 5. COLLECTOR (DIE 2)
- 6. EMITTER (DIE 2)
- 7. NOT USED
- 8. COLLECTOR (DIE 1)

STYLE 9:

- PIN 1. EMITTER (COMMON)
- 2. COLLECTOR (DIE 1)
- 3. COLLECTOR (DIE 2)
- 4. EMITTER (COMMON)
- 5. EMITTER (COMMON)
- 6. BASE (DIE 2)
- 7. NOT USED
- 8. EMITTER (COMMON)

STYLE 10:

- PIN 1. GROUND
- 2. BIAS 1
- 3. OUTPUT
- 4. GROUND
- 5. GROUND
- 6. BIAS 2
- 7. NOT USED
- 8. GROUND

STYLE 11:

- PIN 1. SOURCE (DIE 1)
- 2. GATE (DIE 1)
- 3. SOURCE (DIE 2)
- 4. GATE (DIE 2)
- 5. DRAIN (DIE 2)
- 6. DRAIN (DIE 2)
- 7. NOT USED
- 8. DRAIN (DIE 1)

DOCUMENT NUMBER:	98AON12199D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	7-LEAD SOIC	PAGE 2 OF 3



ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY M. JONES	14 NOV 2002
A	REPLACED ALL PIN 7 IN STYLES WITH "NOT USED". REQ BY M. JONES	06 DEC 2002
B	ADMINISTRATIVE CHANGE	07 JAN 2003
C	CORRECTED DIMENSIONS K AND H. REQ. BY M. JONES	03 JAN 2005
D	CORRECTED DEVICE MARKING INFORMATION FROM "AYWW" TO ALYW". ADDED PIN 1 BARS TO DIAGRAMS. REQ. BY S. BROW.	25 MAY 2007
E	ADDED SOLDER FOOTPRINT. REQ. BY D. BRIGGS.	20 OCT 2009

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.