BR93LC46 BR93LC46A BR93LC46F BR93LC46AF

64 × 16 bit serial EEPROM

The BR93LC46/F and BR93LC46A/AF are CMOS serial input/output-type memory circuits (EEPROMs) that can be programmed electrically. Each can store up to 1024 bits in 64 sixteen bit words. Each word can be accessed separately.

Operational control is performed using five types of commands. The commands, addresses, and data are input through the DI pin under the control of the CS and SK pins.

In a write operation, the internal status signal (Ready or $\overline{\text{Busy}}$) can be output from the DO pin.

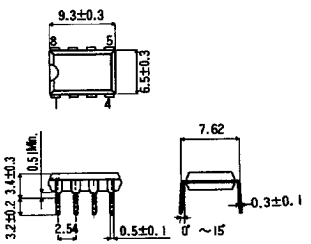
The difference between the BR93LC46/F and the BR93LC46A/AF is the write enable and disable voltages.

Features

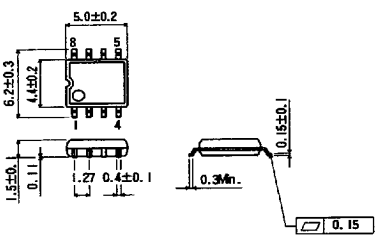
- available in DIP8 and SOP8 packages
- voltage supply 2.0 ~ 5.5 V (suitable for portable, battery powered equipment)
- low current consumption
  - — during operation: 3 mA at 5 V (max)
  - — while standby: 5 μA at 5 V (max)
- can be rewritten at least 100 000 times
- data can be stored for 10 years without corruption
- addresses can be incremented automatically during read operations
- auto erase and auto complete functions can be used during write operations

Dimensions (Units : mm)

BR93LC46 and BR93LC46A (DIP8)



BR93LC46F and BR93LC46AF (SOP8)

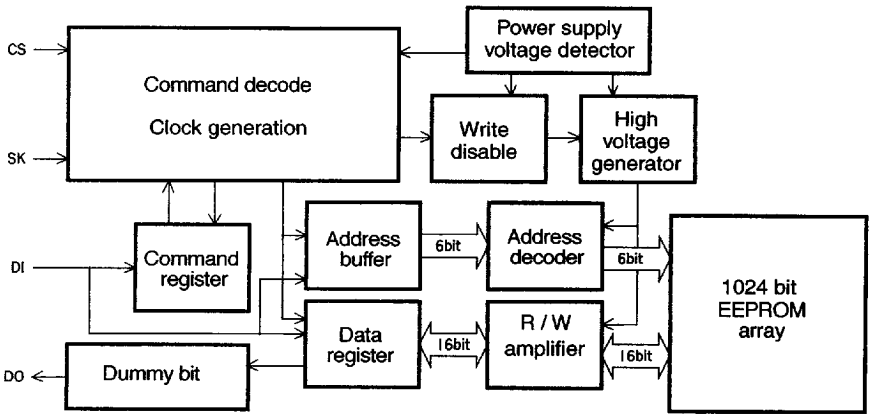


- write inhibit instruction code allows:
  - — write protection when V_{CC} is low
  - — write disable state at power up
  - — write disable and write enable states can be set by software

Applications

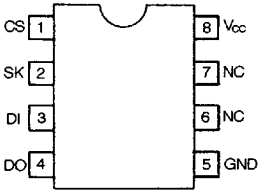
- video cassette recorders
- televisions
- printers
- car stereo radio cassette players
- cordless telephones
- short wave radios
- programmable DIP switches

Block diagram

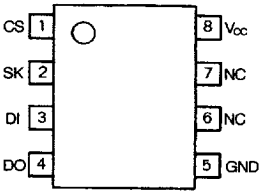


Pin connections

BR93LC46 and BR93LC46A



BR93LC46F and BR93LC46AF



Pin no.		Pin name	Description
BR93LC46 BR93LC46A	BR93LC46F BR93LC46AF		
1	3	CS	Chip select input
2	4	SK	Serial clock input
3	5	DI	Serial data input, start bit, operating code, address
4	6	DO	Serial data output, READY/$\overline{\text{BUSY}}$ internal state display output
5	7	GND	Ground
6	8	NC	Not used
7	1	NC	Not used
8	2	V_{CC}	Power supply

Input and output equivalent circuits

Input circuits

Figure 1

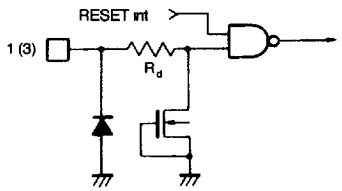


Figure 2

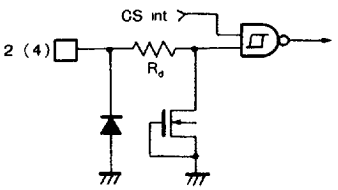
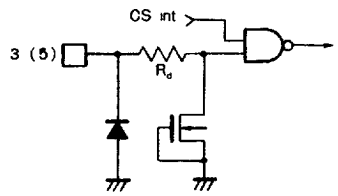
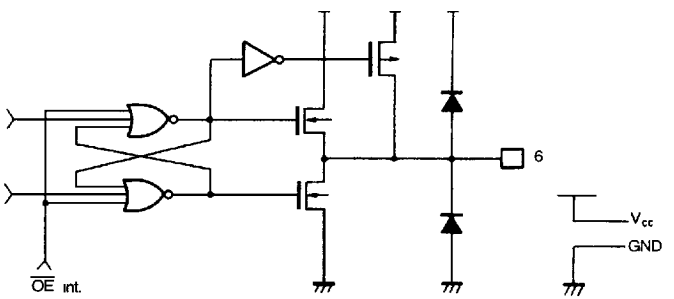


Figure 3



Output circuit

Figure 4



Note: Numbers in parentheses are for SOP packages.

Absolute maximum ratings (T_a = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Supply voltage		V_{CC}	–0.3 ~ +6.0	V	
Power dissipation	BR93LC46 BR93LC46A	P_d	500	mW	Reduce power by 5 mW/°C for each degree above 25°C
	BR93LC46F BR93LC46AF		350		Reduce power by 3.5 mW/°C for each degree above 25°C
Voltage per pin			–0.3 ~ V_{CC} + 0.3	V	
Storage temperature		T_{stg}	–65 ~ +125	°C	
Operating temperature		T_{opr}	–40 ~ +85	°C	

Recommended operating conditions (T_a = 25°C)

Parameter		Symbol	Min	Typical	Max	Unit	Conditions
Supply voltage	WRITE	V_{CC}	2.7 (4.5)		5.5	V	Supply voltage for BR93LC46A and BR93LC46AF shown in parentheses
	READ		2.0		5.5	V	
Input voltage		V_{IN}	0		V_{CC}	V	

Electrical characteristics (unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 5 V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test figure
Input voltage low	V_{IL}	–0.3		0.8	V		
Input voltage high	V_{IH}	2.0		V_{CC} + 0.3	V		
Output voltage 1 low	V_{OL1}			0.4	V	I_{OL} = 2.1 mA	5
Output voltage 1 high	V_{OH1}	2.4			V	I_{OH} = –0.4 mA	6
Output voltage 2 low	V_{OL2}			0.2	V	I_{OL} = 10 µA	5
Output voltage 2 high	V_{OH2}	V_{CC} – 0.4			V	I_{OH} = –10 µA	6
Input leak current	I_{LI}	–1		+1	µA	V_{IN} = 0 V ~ V_{CC}	7
Output leak current	I_{LO}	–1		+1	µA	V_{OUT} = 0 V ~ V_{CC}, CS = GND	8
Operating current 1	I_{CC1}		1.5	3	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 1 MHz, WRITE	9
Operating current 2	I_{CC2}		0.7	1.5	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 1 MHz, READ	9
Standby current	I_{SB}		1.0	5	µA	CS = SK = DI = GND, DO = OPEN	10

Electrical characteristics (Unless otherwise noted, T_a = -40 ~ +80°C, V_{CC} = 3 V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test figure
Input voltage low	V_{IL}	–0.3		$0.15\times V_{CC}$	V		
Input voltage high	V_{IH}	$0.7\times V_{CC}$		$V_{CC}+0.3$	V		
Output voltage low	V_{OL}			0.2	V	I_{OL} = 10 µA	5
Output voltage high	V_{OH}	$V_{CC}-0.4$			V	I_{OH} = –10 µA	6
Input leak current	I_{LI}	–1		+1	µA	V_{IN} = 0 V ~ V_{CC}	7
Output leak current	I_{LO}	–1		+1	µA	V_{OUT} = 0 V ~ V_{CC}, CS = GND	8
Operating current 1	I_{CC1}		0.5	2	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 250 kHz, WRITE	9
Operating current 2	I_{CC2}		0.2	1	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 250 kHz, READ	9
Standby current	I_{SB}		0.4	3	µA	CS = SK = DI = GND, DO = OPEN	10

Electrical characteristics (Unless otherwise noted, T_a = -40 ~ +85°C, V_{CC} = 2.0 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions	Test figure
Input voltage low	V_{IL}	–0.3		$0.15\times V_{CC}$	V		
Input voltage high	V_{IH}	$0.7\times V_{CC}$		$V_{CC}+0.3$	V		
Output voltage low	V_{OL}			0.2	V	I_{OL} = 10 µA	5
Output voltage high	V_{OH}	$V_{CC}-0.4$			V	I_{OH} = –10 µA	6
Input leak current	I_{LI}	–1		+1	µA	V_{IN} = 0 V ~ V_{CC}	7
Output leak current	I_{LO}	–1		+1	µA	V_{OUT} = 0 V ~ V_{CC}, CS = 0 V	8
Operating current 2	I_{CC2}		0.2	1	mA	V_{IN} = V_{IH} / V_{IL}, DO = OPEN, f = 200 kHz, READ	9
Standby current	I_{SB}		0.4	3	µA	CS = SK = DI = 0 V, DO = OPEN	10

Test circuits

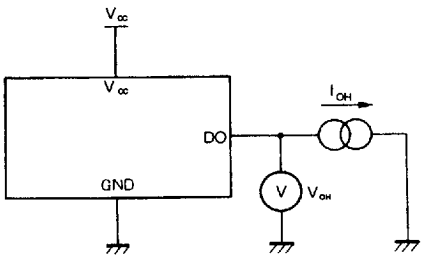


Figure 5 Output voltage low

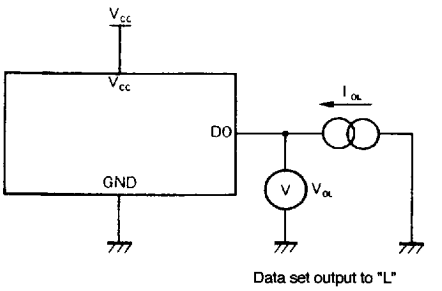


Figure 6 Output voltage high

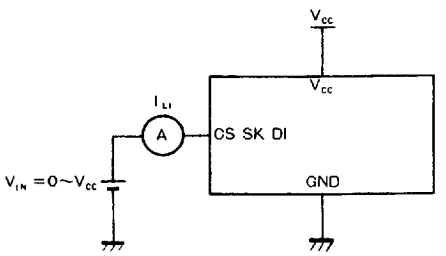


Figure 7 Input leak current

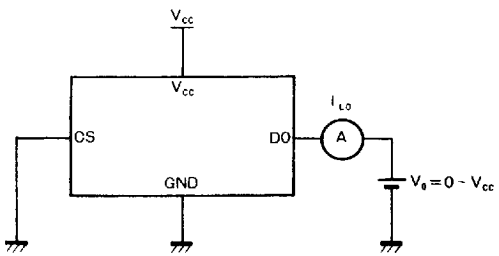


Figure 8 Output leak current

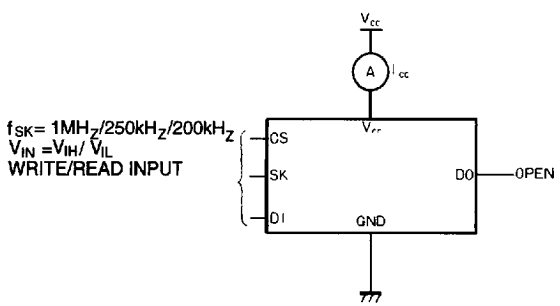


Figure 9 Operating current

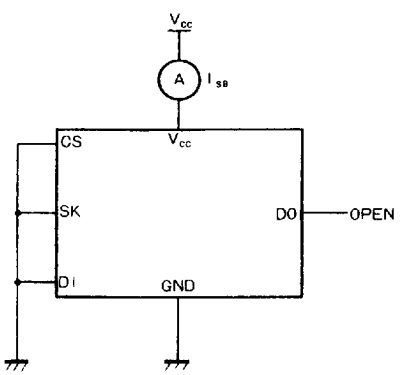


Figure 10 Standby current

Circuit operation

Command mode

Commands are not recognized or acted upon until the start bit is received. The start bit is taken as the first 1 that is received after the CS pin rises. Following is a list of commands that can be used to operate this IC.

Command	Start bit	Operating code	Address	Data	Notes
Read (READ)	1	10	A5 ~ A0		After setting the read command and a continuous SK clock is input, the designated address is output. The upper address data is then output in sequence. (Auto increment function)
Write enabled (WEN)	1	00	11XXXX		
Write (WRITE)	1	01	A5 ~ A0	D15 ~ D0	When the write or write all addresses command is executed, data is written into the selected memory cell. Any data in the cell is automatically erased.
Write all addresses (WRAL)	1	00	01XXXX	D15 ~ D0	
Write disabled (WDS)	1	00	00XXXX		
Erase (ERASE)	1	11	A5 ~ A0		This modes are optional modes. Please contact ROHM for further information.
Chip erase (ERAL)	1	00	10XXXX		

Operating timing characteristics (T_a = 40 ~ 85°C, V_{CC} = 5 V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit
SK clock frequency	f_{SK}			1	MHz
SK time high	t_{SKH}	450			ns
SK time low	t_{SKL}	450			ns
CS time low	t_{CS}	450			ns
CS set up time	t_{CSS}	50			ns
DI set up time	t_{DIS}	100			ns
CS hold time	t_{CSH}	0			ns
DI hold time	t_{DIH}	100			ns
Data "1" output delay time	t_{PD1}			500	ns
Data "0" output delay time	t_{PD0}			500	ns
Time from CS to output confirmation	t_{SV}			500	ns
Time from CS to output high impedance	t_{DF}			100	ns
Write cycle time	$t_{E/W}$			10	ms

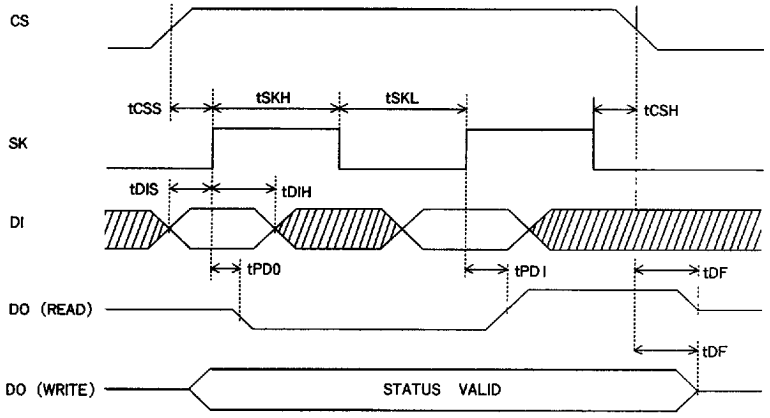
Operating timing characteristics at low voltage (T_a = -40 ~ +85°C, V_{CC} = 3 V ±10%)

Parameter	Symbol	Min	Typical	Max	Unit
SK clock frequency	f_{SK}			250	MHz
SK time high	t_{SKH}	1			µs
SK time low	t_{SKL}	1			µs
CS time low	t_{CS}	1			µs
CS set up time	t_{CSS}	200			ns
DI set up time	t_{DIS}	400			ns
CS hold time	t_{CSH}	0			ns
DI hold time	t_{DIH}	400			ns
Data "1" output delay time	t_{PD1}			2	µs
Data "0" output delay time	t_{PD0}			2	µs
Time from CS to output confirmation	t_{SV}			2	µs
Time from CS to output high impedance	t_{DF}			400	ns
Write cycle time	$t_{E/W}$			25	ms

Operating timing characteristics when reading at low voltage (T_a = -40 ~ +85°C, V_{CC} = 2.0 V)

Parameter	Symbol	Min	Typical	Max	Unit
SK clock frequency	f_{SK}			200	MHz
SK time high	t_{SKH}	2			µs
SK time low	t_{SKL}	2			µs
CS time low	t_{CS}	2			µs
CS set up time	t_{CSS}	400			ns
DI set up time	t_{DIS}	800			ns
CS hold time	t_{CSH}	0			ns
DI hold time	t_{DIH}	800			ns
Data "1" output delay time	t_{PD1}			4	µs
Data "0" output delay time	t_{PD0}			4	µs
Time from CS to output confirmation	t_{DF}			800	ns

Figure 11 Timing chart



Data is acquired from DI in synchronization with the SK rise.

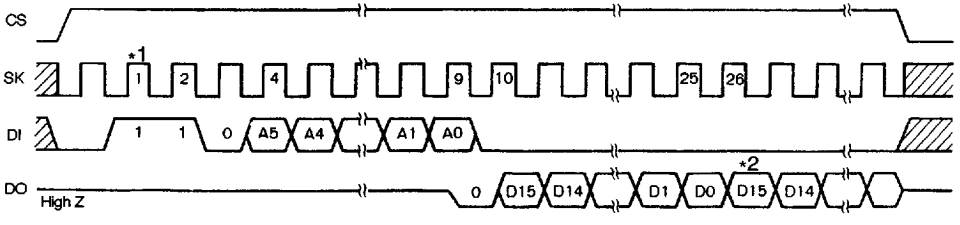
During a READ operation, data is output from DO in synchronization with the SK rise.

A STATUS VALID (READY or $\overline{\text{BUSY}}$) during a WRITE operation is valid from the time CS is HIGH until time t_{CS} after CS falls after the input of a write command and before the output of the next command start bit. Also, CS must be in a High-Z state when DO is LOW.

After the completion of each mode, make sure to set CS LOW (to reset the internal circuit) before changing modes.

Read command

Figure 12 Read cycle timing (READ)



When the read command is executed, the inputted address data (16 bit) is output serially. The data is synchronized with the SK rise during A0 acquisition and a "0" (dummy bit) is output first. All further data is output in synchronization with the SK pulse rises.

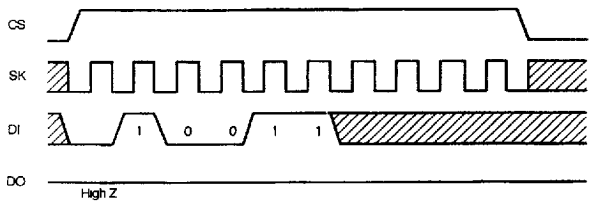
Start bit: (See ✳1 in Figure 12.) When the first data "1" is input after the CS rise, this is taken to be the start bit. Also, the input of a "1" after many "0"s is taken to be a start bit. All operations start after the start bit is recognized. This is common to all commands described following.

Address auto increment function: (See ✳2 in Figure 12.) This IC has an address auto increment function that is valid only during read commands. This allows the upper address data to be read in sequence by using the continual input of the SK clock after the read command is initiated. Make sure to maintain CS HIGH when using auto increment.

Write enabled command

This IC is set to the write disabled state by the internal RESET circuit when the power is turned on. Therefore, before performing a write command, the write enable command must be executed. When this command is executed, it remains valid until a write disable command is issued or the power is cut. Read commands are possible when in the write enable or the write disable state.

Figure 13 Write enabled timing cycle

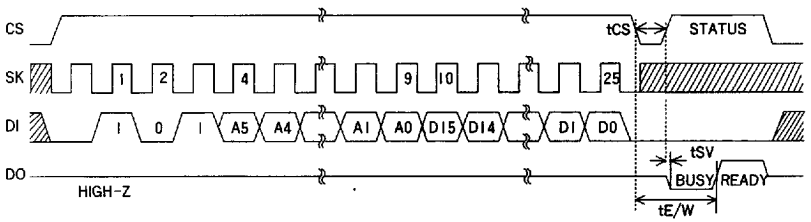


Write command (see Figure 14)

This command writes the inputted 16-bit data (D15 ~ D0) to the designated address (A5 ~ A0). The actual write begins after CS falls after the 25th clock pulse after the start bit input, and DO is in the acquire state.

STATUS is not detected if CS = LOW after the time $t_{E/W}$. When STATUS is detected (CS = HIGH), no commands are accepted while DO is LOW ($\overline{BUSY}$). Therefore. do not perform input commands during this period.

Figure 14 Write cycle timing



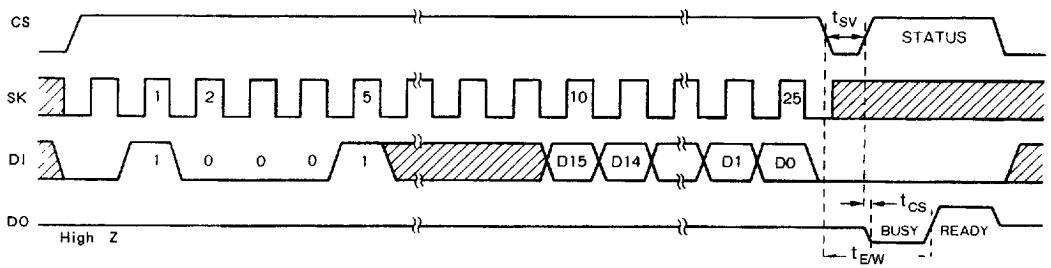
STATUS: After time t_{CS} after CS falls (after the write command input) if CS is set to HIGH, the write execute = BUSY (LOW) and the command wait state = READY (HIGH) are output.

If in the command wait state (STATUS = READY), the next command can be performed within the time $t_{E/W}$. Thus, if data is input via SK and DI with CS = HIGH in the $t_{E/W}$ period, erroneous operations may be performed. Therefore, make sure that DI = LOW when CS = HIGH. (Caution is especially important when common input ports are used.) This is common to all the write commands.

All address write

When this command is issued, the inputted 16-bit data is written simultaneously to all the addresses (64 words). To perform a write of everything in one lot and not write one word at a time, the write time is $t_{E/W}$.

Figure 15 All address write cycle timing



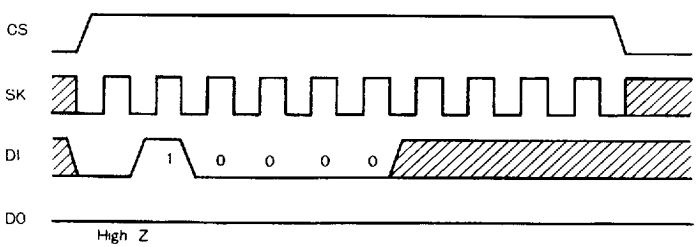
Write disable

When power is turned on, the IC enters the write disable state. Similarly, when the write disable command is issued, the IC enters the same state. When in this state, all write commands are ignored. However, read commands may be executed.

In the write enable state, a write can start even with the erroneous input of a write command.

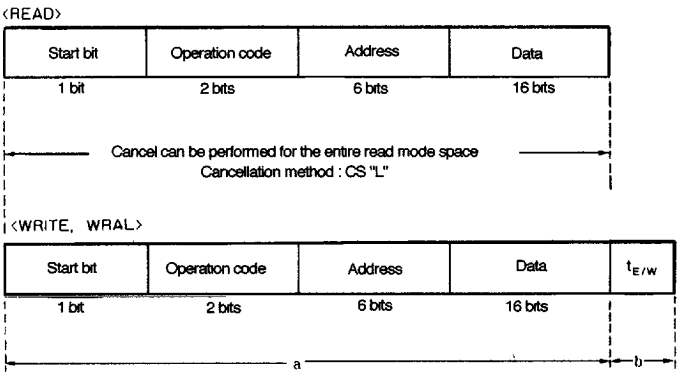
To avoid such errors, we recommend executing a write disable command after completing a write.

Figure 16 Write disable cycle timing (WDS)



Precautions for use

Figure 17 Canceling modes



In time a, modes can be canceled by setting CS to LOW or removing the power supply V_{CC}. Make sure to set V_{CC} OFF after setting CS to LOW

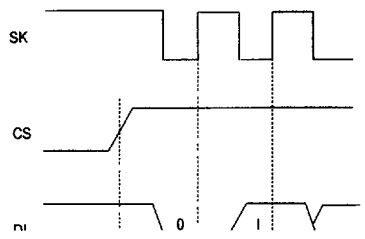
In time b: cancelation is not possible by any method. If the power is removed in this time, the data in the designated addresses is not secured.

Timing in the standby mode

As shown in Figure 18, during standby, if CS rises when SK is HIGH, the DI state may be read on the rising edge. If this happens, and DI is HIGH, this is taken to be the start bit, causing a bit error (see state a in Figure 18).

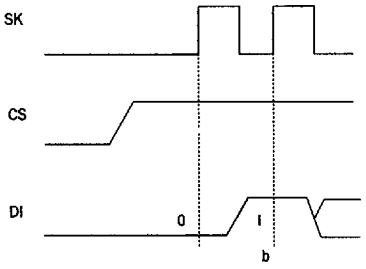
Make sure all inputs are LOW during standby or when turning power supply ON or OFF. (Refer to Figure 19)

Figure 18 Erroneous operation timing



Key
a: start bit position during an erroneous operation
b: actual start bit position

Figure 19 Normal operation timing



Precautions when turning power on and off

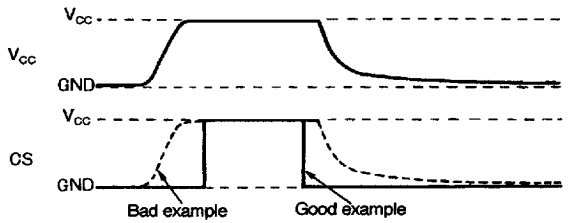
Make certain to set CS to LOW when turning power on or off. (Refer to Figure 20)

When CS is HIGH, the EEPROM enters the active state. Turning power on in this situation can result in erroneous operations and erroneous writes due to the influence of noise. To avoid this, make sure to set CS to LOW (disable mode) when turning power on. (When CS is LOW, all input is canceled.)

When the power supply is turned off, the low power state can continue for a long time because of the capacity of the power supply line. Erroneous operations and erroneous writes can occur at such times for the same reasons as described above. Therefore, make sure to set CS to LOW before turning off the power supply.

To avoid erroneous writes when the voltage is low, a circuit which resets the write command when V_{CC} is less than 2.0 V is installed. (V_{CC}-lockout circuit). (For BR93LC46A, the trip is set at 3.0 V typically)

Figure 20 Relationship between V_{CC} and CS



In the bad example shown in Figure 20, the CS pin pulls up to V_{CC}. In this situation, CS is HIGH (active state). The EEPROM may perform erroneous operations or erroneous writes due to the influence of noise.

Caution is required because such problems can occur even when the CS input is HIGH-Z.

In the good example, CS is LOW until the IC reaches V_{CC} and is set to LOW well before the voltage starts to fall when the EEPROM is de-energized.

Clock (SK) rise conditions

If there is excessive noise on the signal line, erroneous operations can occur due to erroneous counts in the clock. To avoid this, a Schmitt trigger is built into the SK input.

Furthermore, the hysteresis width of this circuit is set at about 0.2 V. Therefore, if the noise exceeds the SK input, make sure to set the noise amplitude to less than 0.2 $V_{pk\text{-}pk}$. Also, make sure to accelerate rises and falls in the clock as much as possible.

Power supply noise

The BR93LC46/BR93LC46AF discharge high loads of high voltage when a write is completed. The power supply may fluctuate at such times. Therefore, make sure to connect a 1000 pF or greater capacitor between V_{CC} (pin 8) and GND (pin 5) (In the SOP version, V_{CC} is pin 2, GND is pin 7).

Connecting DI and DO directly

The BR93LC46 and BR93LC46 F have an independent input pin (DI) and output pin (DO). These are treated as individual signals on the timing chart but can be controlled through one control line.

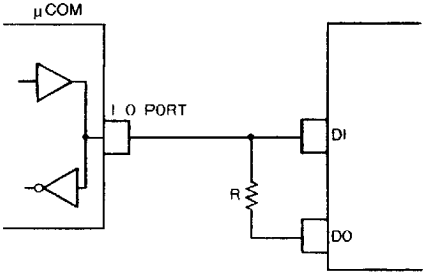
Data collision between the μ-COM output and the DO output

Within the input and output timing of the BR93LC46/BR93LC46A, the drive from the μ-COM output to the DI input and a signal output from the DO output can be emitted at the same time. This happens only for the 1 clock cycle (a dummy bit "0" is output to the DO pin) which acquires the A0 address data during a read cycle.

Especially when the address data A0 = 1, the μ-COM output becomes a direct current source for the DO pin. The resistor R is the only resistance that limits this current (see Figure 21). Therefore, a resistor with a value which satisfies the μ-COM and the BR93LC46/BR93LC46A current capacity is required.

When using a single control line, when a dummy bit "0" is output to the DO, the μ-COM I/O address data A0 is also output. Therefore, the dummy bit cannot be detected.

Figure 21 Output resistor R



Feedback to the DI input from the DO output

Data is output from the DO pin and then feeds back into the DI input through the resistor R. This happens when

- DO data is output during a READ operation
- READY/$\overline{\text{BUSY}}$) signal is output during a WRITE or WRAL operation

Such feedback does not cause problems in the basic operation of the BR93LC46 or the BR93LC46A.

The μ-COM input level must be adequately maintained for the voltage drop at R which is caused by the total input lead current for the μ-COM and the BR93LC46 or BR93LC46A.

In the state in which SK is input, when the READY/$\overline{\text{BUSY}}$ function is used, make sure that CS is dropped to LOW within 4 clock pulses of the output of the READY signal HIGH and the standby mode is restored. For input after the fifth clock pulse, the READY HIGH will be taken as the start bit and WDS or some other mode will operate, depending on the DI state.