Data International Co., Ltd.

DATAVISION

APPROVAL SHEET

Customer	:	
Part Name	:	**LCD MODULE**
Model No.	:	**DV-40200-S2RB/R22**
Drawing No.	:	
Approved by	:	
Date	:	

Approved	Checked	Prepared	Sheet Code:
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CONTENTS

1. SCOPE

The DV-40200-S2RB/R22, dot-matrix LCD unit of a 5 x 7- dot 40-character 2-line dot-matrix LCD panel, LCD driver, controller LSI on a single PCB. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the unit can efficiently display the desired characters under microprocessor control.

2. PRODUCT SPECIFICATIONS

2.1 General

- The LCD of the unit is STN (Super Twisted Nematic) Gray Reflective , Normal temperature type.
- Low power consumption with the dot-matrix LCD panel and CMOS LSI.
- Thin, lightweight design permits easy installation in a variety of equipment.
- Allowing for being connected at general-purpose CMOS signal level, the unit can be easily interfaced to a microprocessor with common 4-bit and 8-bit parallel inputs and outputs.
- Multiplexing driving : 1/16duty, 1/4bias, 6 o' clock
- Built-in character generator ROM and RAM, and display data RAM:
  Character generator ROM
    225 different 5 x 7 dot-matrix character patterns (Alphanumeric and symbols)
  Character generator RAM
    8 different user programmed 5 x 7 dot-matrix patterns
  Display data RAM
    80 x 8 bits
- Numerous instructions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Blink character, Cursor shift, Display shift

2.2 Mechanical Characteristics

Item	Characteristic
Number of Characters	40 × 2
Dot dimensions(mm)	0.6 × 0.65
Dot spacing (mm)	0.05
Character Size (mm)	3.2 × 5.5
Module dimensions (Horizontal × Vertical × Thickness, mm)	175.0 × 33.5 × 14.1max.
Viewing area (Horizontal × Vertical, mm)	154.0 × 16.5
Active area (Horizontal × Vertical, mm)	147.5 × 11.5

2.3 Absolute Maximum Ratings (Without back-light)

Characteristic	Symbol	Unit	Value
Power Supply Voltage(1)	V_{DD}	V	-0.3 ~ +7.0
Power Supply Voltage(2)	V_{LCD}	V	V_{DD}-15.0 ~ V_{DD}+0.3
Input Voltage	V_{IN}	V	-0.3 ~ V_{DD}+0.3

NOTE: Voltage greater than above may damage the circuit.
$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

2.4 Electrical Characteristics (Without back-light)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-	4.5	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=5.0 V, fosc = 270 kHz)	-	0.35	0.6	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	2.2	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (2) (OSC1)	V_{IH2}	-	V_{DD}-1.0	-	V_{DD}	V
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.205 mA	2.4	-	-	V
	V_{OL1}	I_{OL} = 1.2 mA	-	-	0.4	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O = -40 µA	0.9V_{DD}	-	-	V
	V_{OL2}	I_O = 40 µA	-	-	0.1V_{DD}	
Voltage Drop	Vd_{COM}	I_O = ± 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IKG}	V_{IN} = 0 V to V_{DD}	-1	-	1	µA
Input Low Current	I_{IL}	V_{IN} = 0 V, V_{DD} = 5 V (PULL UP)	-50	-125	-250	
Internal Clock (external Rf)	f_{OSC1}	Rf = 91 kΩ ± 2% (V_{DD} = 5 V)	190	270	350	kHz
External Clock	f_{OSC}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R, t_F		-	-	0.2	µs
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 Bias)	3.0	-	13.0	V

2.5 Optical Characteristics

Absolute maximum ratings

Item	Symbol	Rating	Unit	Remarks
Storage temperature range	Tst	-20~60	°C	No condensation
Operating temperature range	Top	0~50	°C	No condensation
Maximum AC applied voltage	VAC	10	V	Less than 1 hour
Maximum DC applied voltage	VDC	50	mV	--

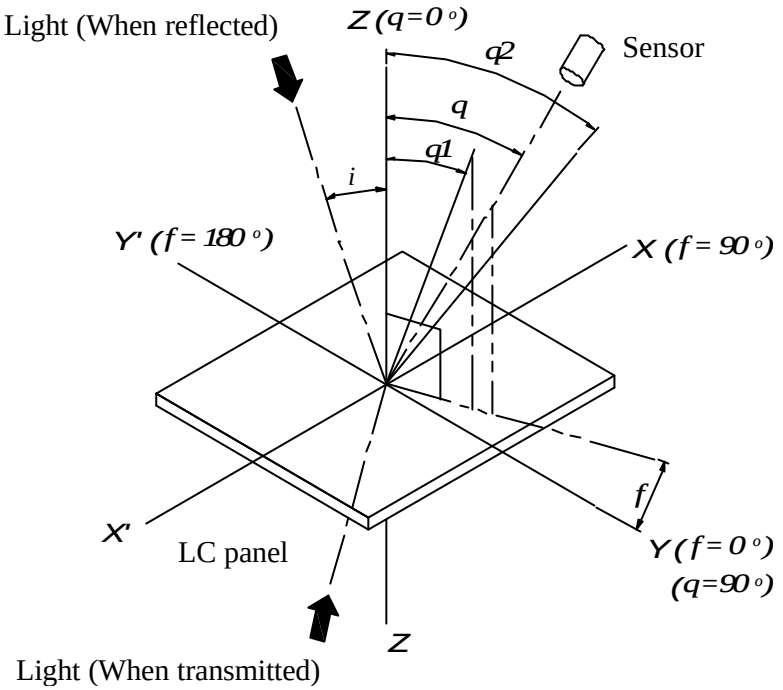
2.6 Optical Characteristics

1/16 duty, 1/4 bias, Vop=4.3V

Item	Symbol	Temp.	Min.	Typ.	Max.	Unit
Driving voltage	Vop	0°C	4.35	4.55	4.75	V
		25°C	4.10	4.30	4.50	
		50°C	3.65	3.85	4.05	
Contrast	Cr	25°C	4	7	--	--
Frame freq.	f	--	--	64	--	Hz
Viewing angle*	θ_1	25°C	--	50	--	deg.
	θ_2		--	130	--	
Response time	t_{on}	25°C	--	100	200	ms
	t_{off}		--	210	340	

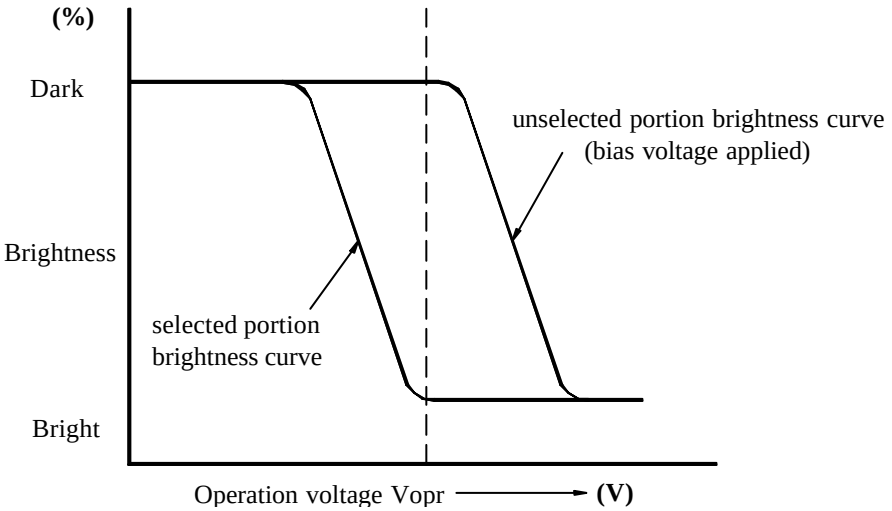
2.6.1 Definition of optical characteristics

* Definition of angles ϕ and θ

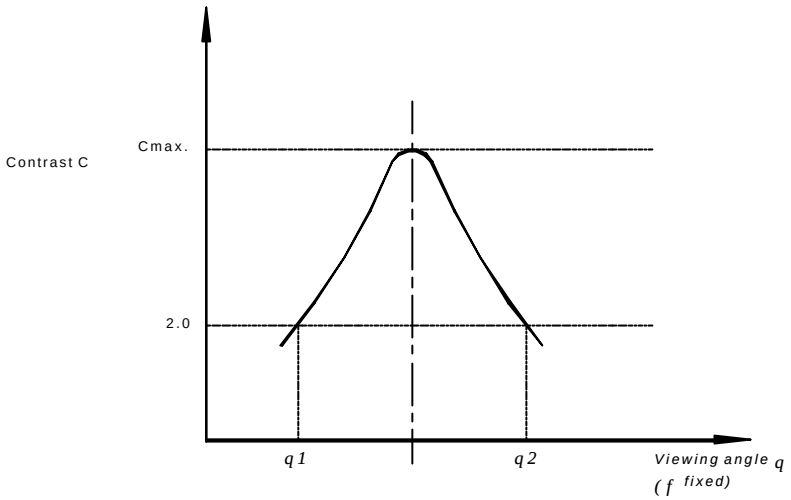


*Definition of contrast C

$$C = \frac{B1}{B2} = \frac{\text{Brightness of selected portion}}{\text{Brightness of unselected portion}}$$

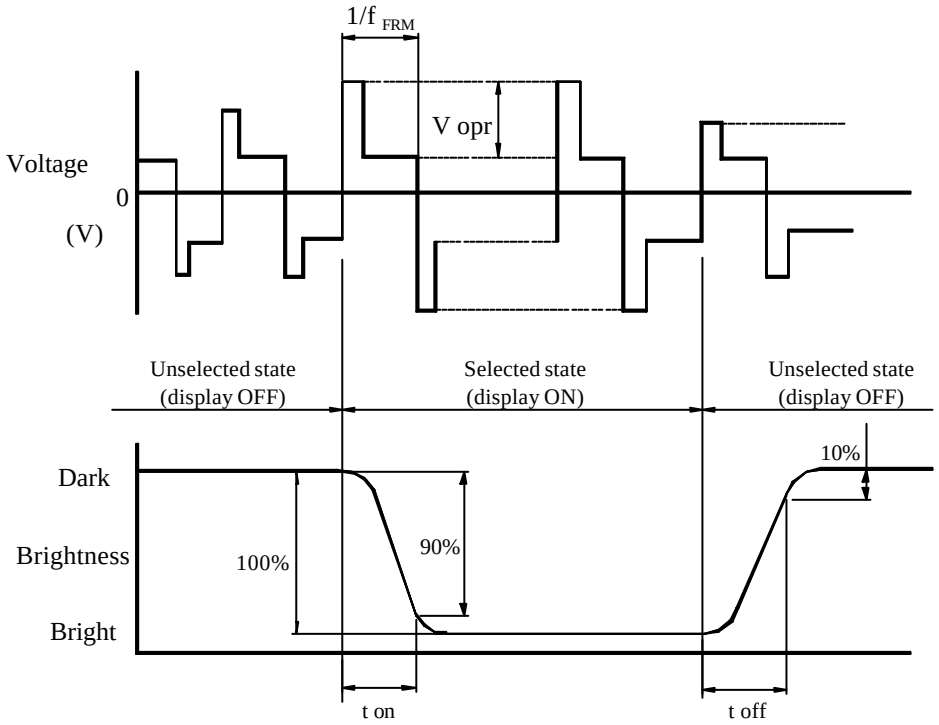


* Definition of viewing angles θ1 and θ2



Note : Optimum vision with the naked eye and viewing angle θ at Cmax above are not always the same.

* Definition of response time



Vop : Operating voltage (V)
fFRM : Frame frequency (Hz)
ton : Response time (rise) (ms)
toff : Response time (fall) (ms)

3. RELIABILITY

3.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40°C±2°C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	60°C±2°C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	-20± ~ +60°C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	-20±2°C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

* Dissipation current, contrast and display functions

** Polarizing filter deterioration, other appearance defects

3.2 Liquid crystal panel service life

100,000 hours minimum at 25°C±10°C

3.3 Definition of panel service life

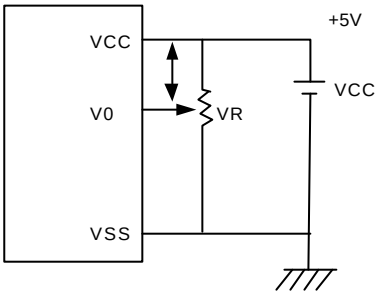
- Contrast becomes 30% of initial value
- Current consumption becomes three times higher than initial value
- Remarkable alignment deterioration occurs in LCD cell layer
- Unusual operation occurs in display functions

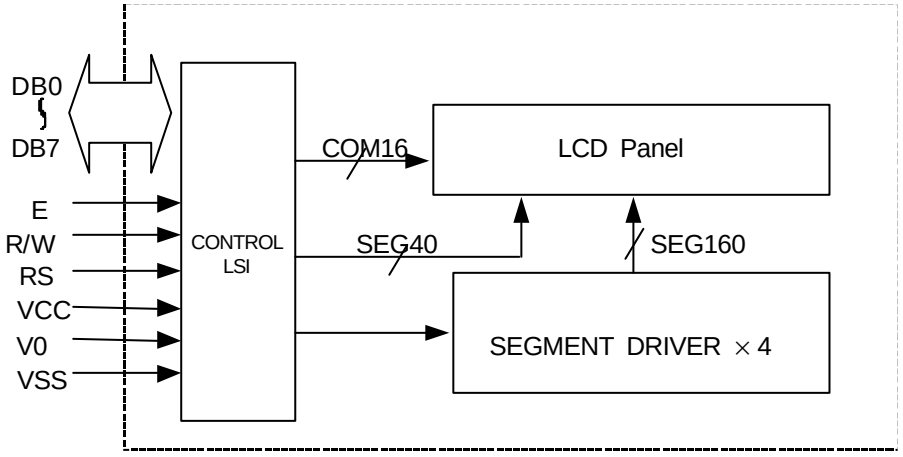
4. OPERATING INSTRUCTIONS

4.1 Input signal Function

NO.	Symbol	Function
1	VSS	Ground (0V)
2	VCC	Power supply for Logic circuit
3	V0	Power Supply for Driving the LCD
4	RS	Data / Instruction select
5	R/W	Read / Write select
6	E	Enable signal
7-14	DB0-DB7	Data Bus line

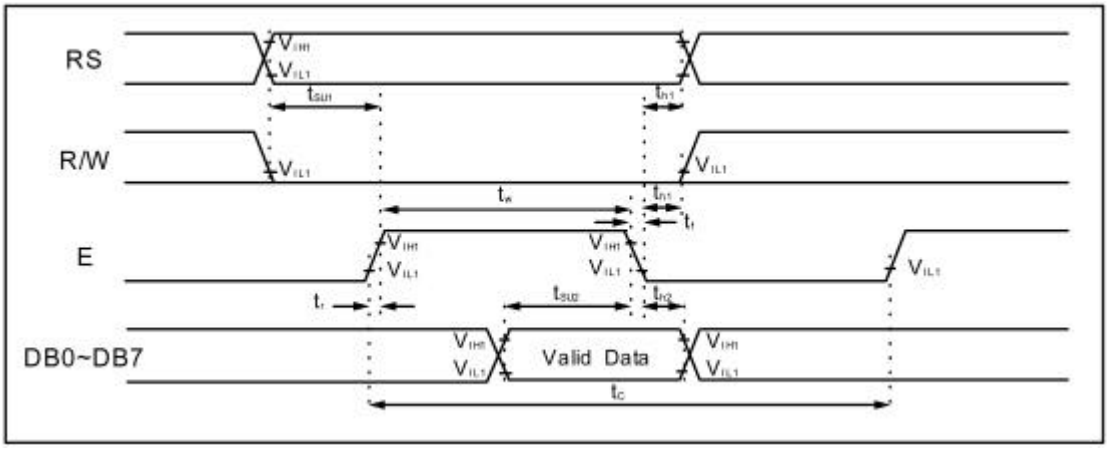
4.2 Block diagram



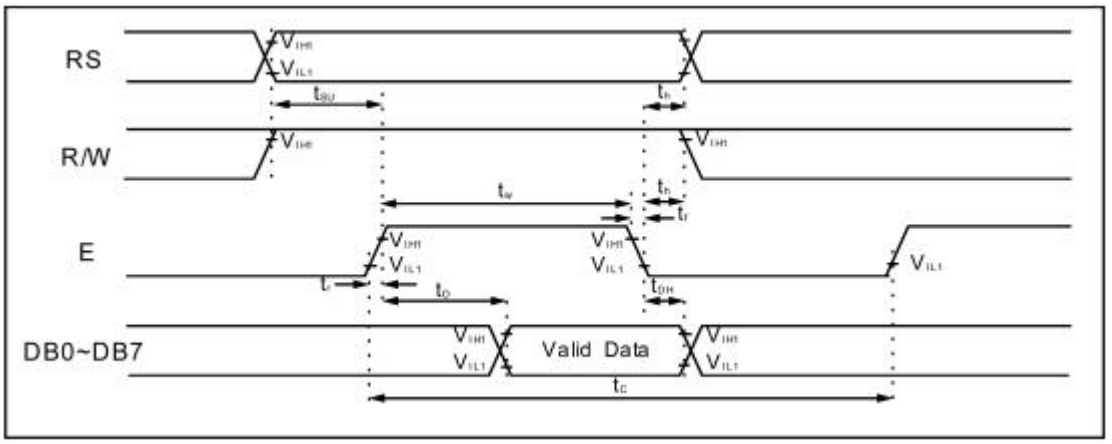


4.3 Timing Characteristics

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	



Write Mode Timing Diagram



Read Mode Timing Diagram

4.4 Instruction Description

INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control informations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 7).
Instructions can be divided largely into four groups:

1) KS0066U function set instructions (set display methods, set data length, etc.)
2) address set instructions to internal RAM
3) data transfer instructions with internal RAM
4) others

The address of the internal RAM is automatically increased or decreased by 1.

Note: During internal operation, Busy Flag (DB7) is read "High".
Busy Flag check must be preceded by the next instruction.
When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to 'Low".

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address,
and set DDRAM address to "00H" into AC (address counter).
Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display.
Make the entry mode increment (I/D = 'High').

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

* "-": dont care

Return Home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH = "Low", shifting of entire display is not performed.
If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value
(I/D = "High": shift left, I/D = "Low": shift right).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data remains in DDRAM.

C: Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.(Refer to Table 6)
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

Table 6. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.

F: Display font type control bit
When F = "Low", 5 ×8 dots format display mode is set.
When F = "High", 5 ×11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = Low), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = High), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not.
If the resultant BF is "High", internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not Yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.
After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM read operation, display shift may not be executed correctly.

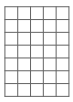
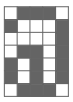
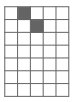
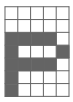
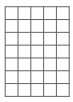
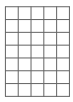
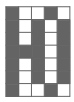
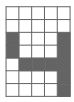
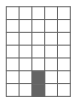
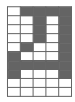
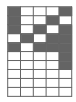
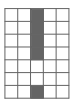
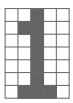
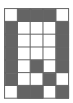
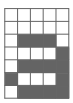
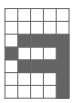
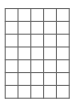
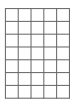
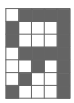
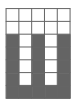
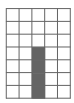
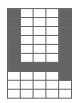
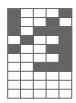
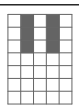
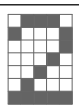
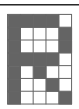
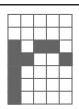
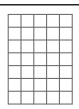
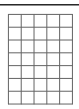
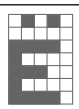
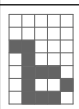
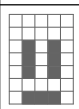
NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

4.5 Instruction table

Instruction	Instruction Code										Description	Execution time (fosc= 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.53 ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5×11dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

* "-": don't care

4.6 Font table S6A0066-22

Upper 4bit / Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														

5. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is $25^{\circ}C \pm 10^{\circ}C$ and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

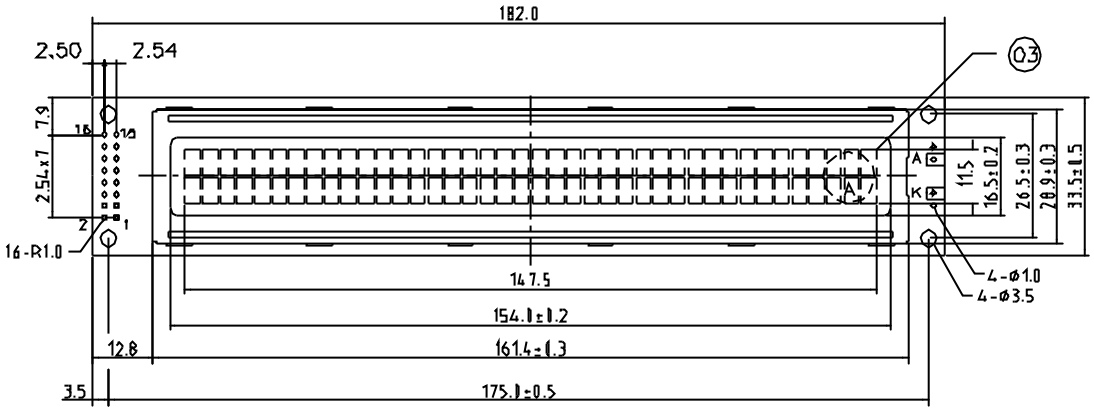
Cleaning

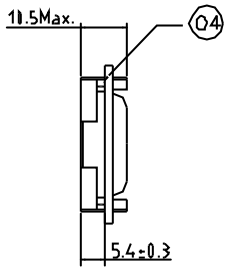
- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

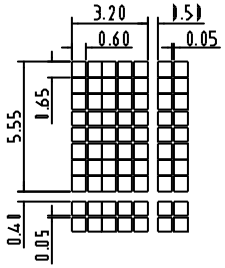
6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

REVISION RECORD		
REV	DATE	DESCRIPTION

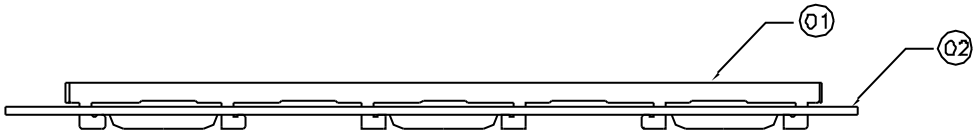






SCALE 5:1

A BLOCK



PIN
1.VSS
2.VDD
3.V0
4.RS
5.R/W
6.E
7.DB0
~
14.DB7
15.LED A
16.LED K

TOLERANCE GRADE(±)		
GRADE	A	B
~ 6	0.05	0.1
6 ~ 18	0.08	0.18
18 ~ 50	0.1	0.25
50 ~ 180	0.2	0.4
180~	0.3	0.5

NO	PART NO	QTY
04	1604020003(ZEBRA)	2
03	1004020010(LCD)	1
02	1704020008(PCB)	1
01	1604020000(BEZEL)	1

DATA INTERNATIONAL CO.,			APPROVED	TITLE	DV-4020S2RB/R22
UNLESS OTHERWISE SPECIFIED TOLERANCE ARE "B"GRADE			CHECKED		P88-6
DECIMAL	ANGULAR	MATERIAL	DESIGNED	REV	DRAWING NUMBER
			DRAWN ALEX	00	3075100058
SCALE	THIRD ANGLE PROJECTION	UNIT ☒ M/M ☐ INCH	DATE 04/15/02'	FINISHED LCM-ASSY	SHEET 1 OF 1