19-1156; Rev 2; 6/98

MAXIM

+2.7V to +5.25V, Low-Power, 10-Bit Serial ADCs in SO-8

General Description

The MAX1242/MAX1243 are low-power, 10-bit analog-to-digital converters (ADCs) available in 8-pin packages. They operate with a single +2.7V to +5.25V supply and feature a 7.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed, 3-wire serial interface.

Power consumption is only 3mW (V_{DD} = 3V) at the 73ksps maximum sampling speed. A 2µA shutdown mode reduces power at slower throughput rates.

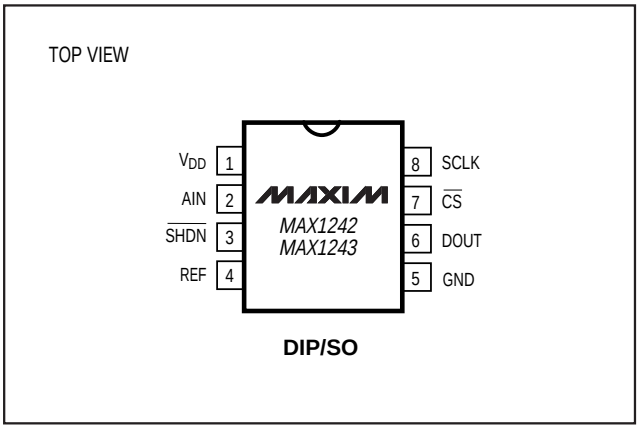
The MAX1242 has an internal 2.5V reference, while the MAX1243 requires an external reference. The MAX1243 accepts signals from 0V to V_{REF}, and the reference input range includes the positive supply rail. An external clock accesses data from the 3-wire interface, which connects directly to standard microcontroller I/O ports. The interface is compatible with SPI™, QSPI™, and Microwire™.

Excellent AC characteristics and very low power combined with ease of use and small package size make these converters ideal for remote-sensor and data-acquisition applications, or for other circuits with demanding power consumption and space requirements. The MAX1242/MAX1243 are available in 8-pin DIP and SO packages.

Applications

Portable Data Logging
Test Equipment
Isolated Data Acquisition
Process Control Monitoring
Temperature Measurement

Pin Configuration



Features

- **+2.7V to +5.25V Single-Supply Operation**
- **10-Bit Resolution**
- **Internal 2.5V Reference (MAX1242)**
- **Small Footprint: 8-Pin DIP and SO Packages**
- **Low Power: 3.7mW (73ksps, MAX1242)**
  3mW (73ksps, MAX1243)
  66µW (1ksps, MAX1243)
  5µW (power-down mode)
- **Internal Track/Hold**
- **SPI™/QSPI™/Microwire™ 3-Wire Serial Interface**
- **Pin-Compatible 12-Bit Upgrades: MAX1240/MAX1241**

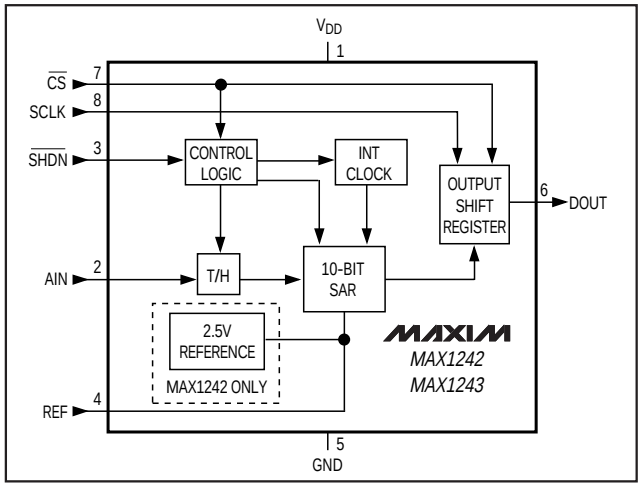
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1242ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1242BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1242ACSA	0°C to +70°C	8 SO	±1/2
MAX1242BCSA	0°C to +70°C	8 SO	±1
MAX1242AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1242BEPA	-40°C to +85°C	8 Plastic DIP	±1

Ordering Information continued at end of data sheet.

Note: *Order the MAX1242A in place of the MAX1242C. Order the MAX1242B in place of the MAX1242D.*

Functional Diagram



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+2.7V to +5.25V, Low-Power, 10-Bit Serial ADCs in SO-8

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND.....-0.3V to +6V
DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
DOUT Current.....±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX1242/MAX1243_C_A.....0°C to +70°C
MAX1242/MAX1243_E_ A .....-40°C to +85°C
MAX1242/MAX1243_MJA .....-55°C to +125°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V; 73ksps; f_{SCLK} = 2.1MHz (50% duty cycle); MAX1242—4.7µF capacitor at REF pin, MAX1243—external reference; V_{REF} = 2.5V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note1)						
Resolution			10			Bits
Relative Accuracy (Note 2)		MAX124_A			±0.5	LSB
		MAX124_B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX124_A			±1	LSB
		MAX124_B			±2	
Gain Error (Note 3)		MAX124_A			±1	
		MAX124_B			±2	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.5p-p, 73ksps, f_{SCLK} =2.1MHz)						
Signal-to-Noise Plus Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time	t_{CONV}		5.5		7.5	µs
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Throughput Rate		f_{SCLK} = 2.1MHz			73	ksps
Aperture Delay	t_{AP}	Figure 9		30		ns
Aperture Jitter				<50		ps
ANALOG INPUT						
Input Voltage Range			0		V_{REF}	V
Input Capacitance				16		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; 73ksps; f_{SCLK} = 2.1MHz (50% duty cycle); MAX1242—4.7µF capacitor at REF pin, MAX1243—external reference; V_{REF} = 2.5V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL REFERENCE (MAX1242 only)							
REF Output Voltage		T_A = +25°C (Note 4)		2.470	2.500	2.530	V
REF Short-Circuit Current						30	mA
REF Temperature Coefficient		MAX1242			±30		ppm/°C
Load Regulation (Note 5)		0mA to 0.2mA output load			0.35		mV
Capacitive Bypass at REF				4.7			µF
EXTERNAL REFERENCE (VREF = 2.5V)							
Input Voltage Range				1.00		V_{DD} + 50mV	V
Input Current					100	150	µA
Input Resistance				18	25		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V			±0.01	10	µA
Capacitive Bypass at REF				0.1			µF
DIGITAL INPUTS: SCLK, $\overline{CS}$, $\overline{SHDN}$							
SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$		2.0			V
		V_{DD} > 3.6V		3.0			
SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}					0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{SL}					0.4	V
$\overline{SHDN}$ Input Current		$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{SM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = float			V_{DD} / 2		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = float				±100	nA
DIGITAL OUTPUT: DOUT							
Output Voltage Low	V_{OL}	I_{SINK} = 5MA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 6)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			2.7		5.25	V
Supply Current	I_{DD}	Operating mode (MAX1242)	V_{DD} = 3.6V		1.4	2.0	mA
			V_{DD} = 5.25V		1.8	3.0	
		Operating mode (MAX1243)	V_{DD} = 3.6V		0.9	1.5	
			V_{DD} = 5.25V		1.6	2.5	
		Power-down	V_{DD} = 3.6V		1.9	10	µA
			V_{DD} = 5.25V		3.5	15	
Power-Supply Rejection (Note 7)	PSR	V_{DD} = $V_{DD(min)}$ to $V_{DD(max)}$, full-scale input			±0.3		mV

+2.7V to +5.25V, Low-Power, 10-Bit Serial ADCs in SO-8

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, circuit of Figure 9, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	$\overline{CS}$ = V_{DD} (Note 8)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX124_ _C/E	20		200	ns
			MAX124_ _M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
SCLK Clock Frequency	f_{SCLK}			0		2.1	MHz
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CS0}			50			ns
DOUT Rise to SCLK Rise (Note 6)	t_{STR}			0			ns
$\overline{CS}$ Pulse Width	t_{CS}			240			ns

Note 1: Tested at V_{DD} = +2.7V.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.
Note 3: Offset nulled.
Note 4: Sample tested to 0.1% AQL.
Note 5: External load should not change during conversion for specified accuracy.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: Measured as [V_{FS} ($V_{DD(min)}$) - V_{FS} ($V_{DD(max)}$)].
Note 8: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.

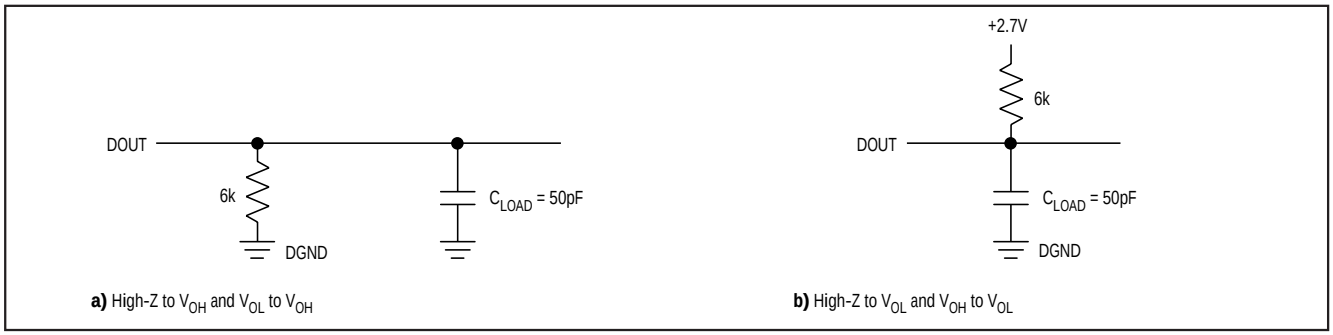


Figure 1. Load Circuits for DOUT Enable Time

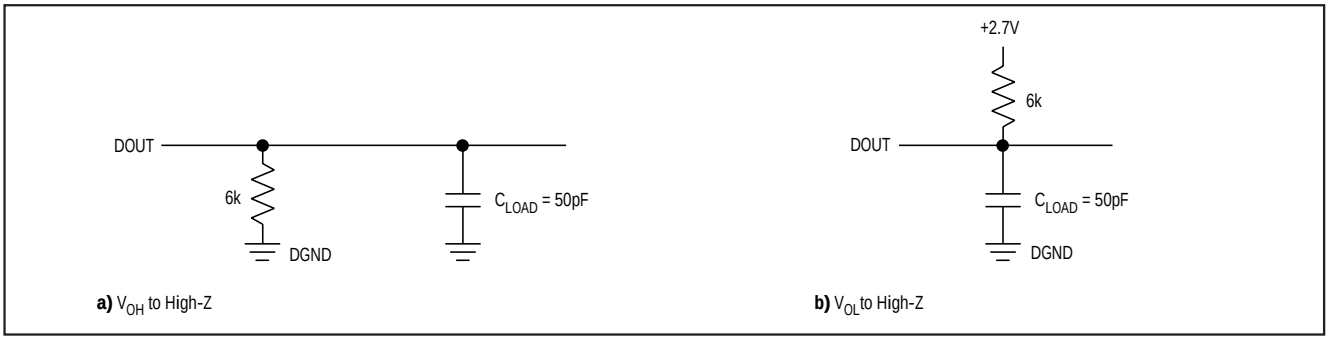
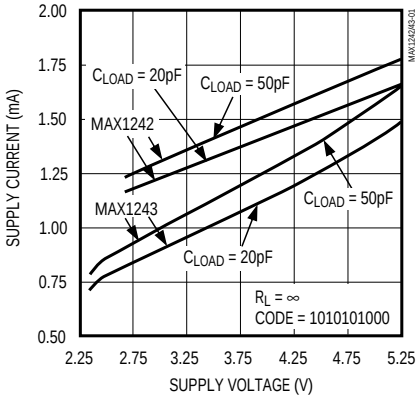
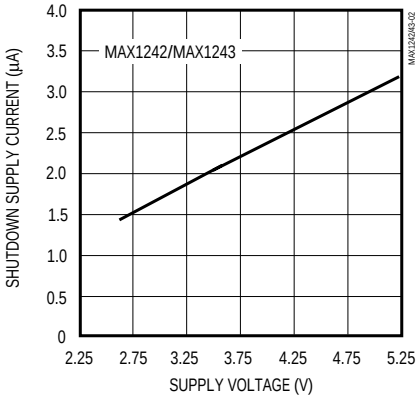


Figure 2. Load Circuits for DOUT Disable Time

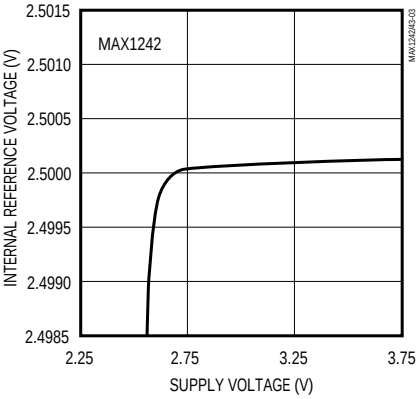
SUPPLY CURRENT vs. SUPPLY VOLTAGE



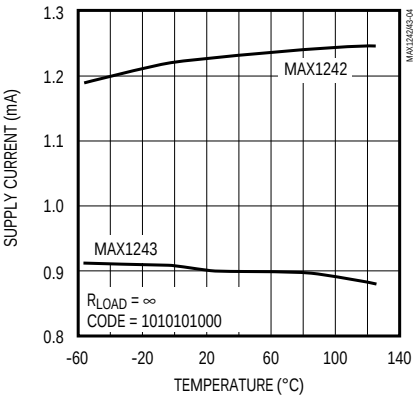
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



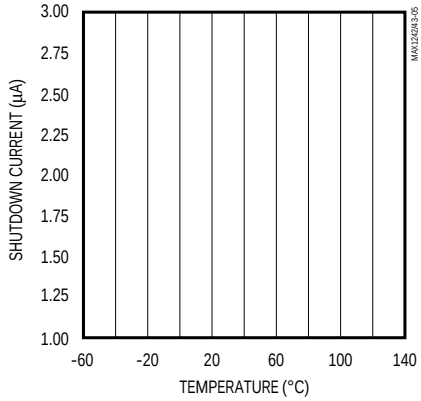
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



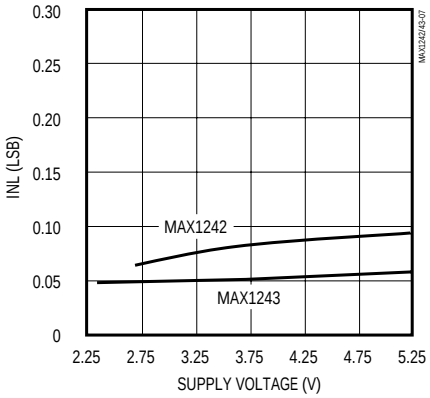
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



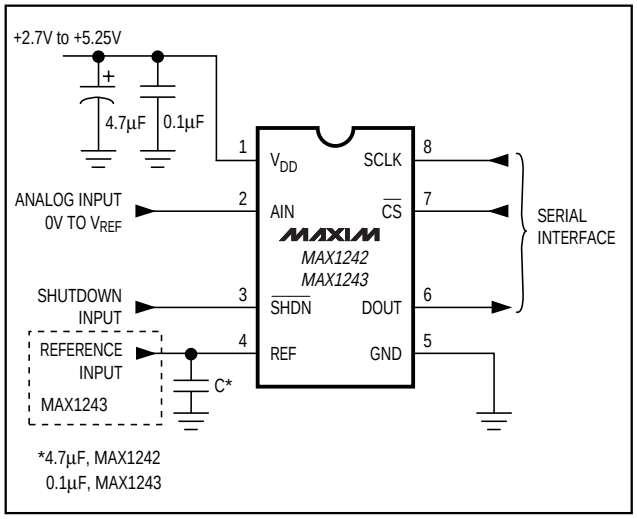


Figure 3. Operational Diagram

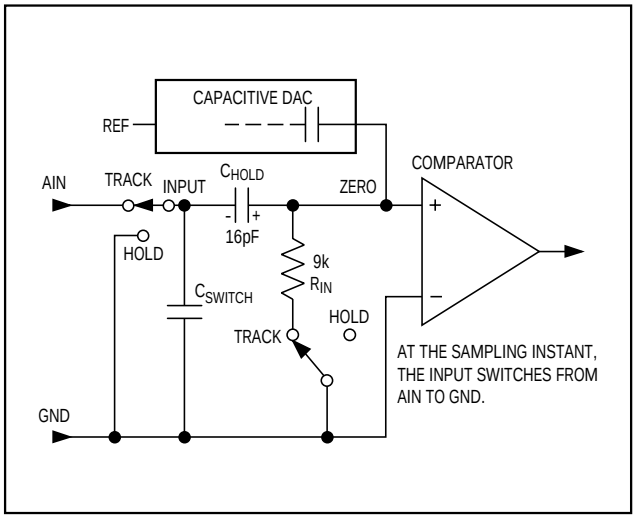


Figure 4. Equivalent Input Circuit

where R_{IN} = 9kΩ, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.5µs. Source impedances below 4kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's input signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to 2mA.

Internal Reference (MAX1242)

The MAX1242 has an on-chip voltage reference trimmed to 2.5V. The internal reference output is connected to REF and also drives the internal capacitive DAC. The output can be used as a reference voltage source for other components and can source up to 400µA. Bypass REF with a 4.7µF capacitor. Larger capacitors increase wake-up time when exiting shutdown (see *Using $\overline{SHDN}$ to Reduce Supply Current*). The internal reference is enabled by pulling the $\overline{SHDN}$ pin high. Letting $\overline{SHDN}$ float disables the internal reference, which allows the use of an external reference, as described in the *External Reference* section.

External Reference

The MAX1242/MAX1243 operate with an external reference at the REF pin. To use the MAX1242 with an external reference, disable the internal reference by letting $\overline{SHDN}$ float. Stay within the voltage range 1.0V to V_{DD} to achieve specified accuracy. The minimum input impedance is 18kΩ for DC currents. During conversion, the external reference must be able to deliver up to 250µA of DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

+2.7V to +5.25V, Low-Power, 10-Bit Serial ADCs in SO-8

Serial Interface

Initialization after Power-Up and Starting a Conversion

When power is first applied, and if $\overline{SHDN}$ is not pulled low, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy. With an external reference, the internal reset time is 10µs after the power supplies have stabilized. No conversions should be performed during these times.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using $\overline{SHDN}$ to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX1242/MAX1243 between conversions. Figure 6 shows a plot of average supply current vs. conversion rate. Because the MAX1243 uses an external reference voltage (assumed to be present continuously), it "wakes up" from shutdown more quickly, providing lower average supply currents. The wake-up time, t_{WAKE}, is the time from $\overline{SHDN}$ deasserted to the time when a conversion may be initiated (Figure 5). For the MAX1242, this time depends on the time in shutdown (Figure 7) because the external 4.7µF reference bypass capacitor loses charge slowly during shutdown. The MAX1243's wake-up time is largely dependent on the external reference's power-up time. If the external reference is not shut down, the wake-up time is approximately 4µs.

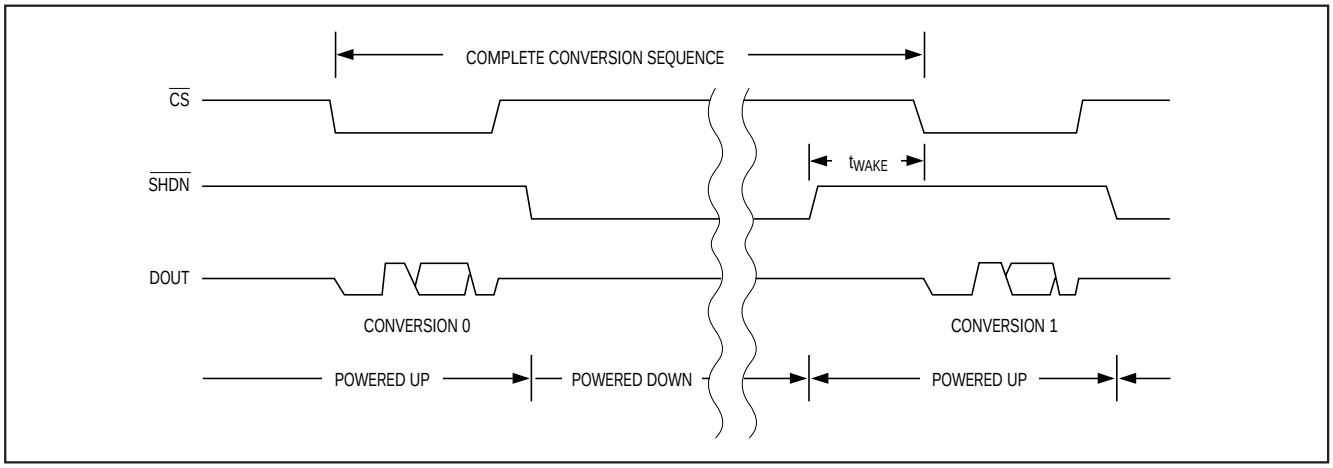


Figure 5. Shutdown Sequence

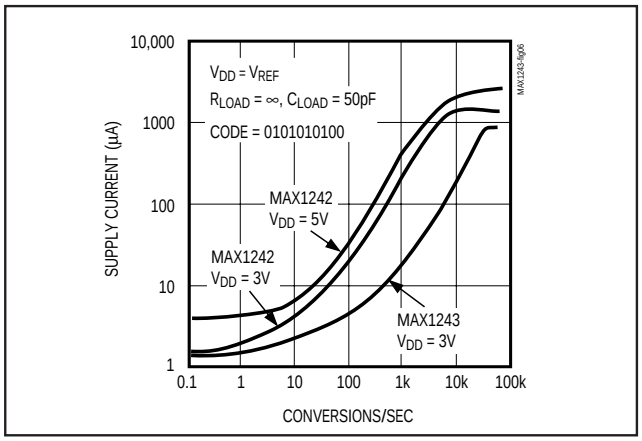


Figure 6. Average Supply Current vs. Conversion Rate

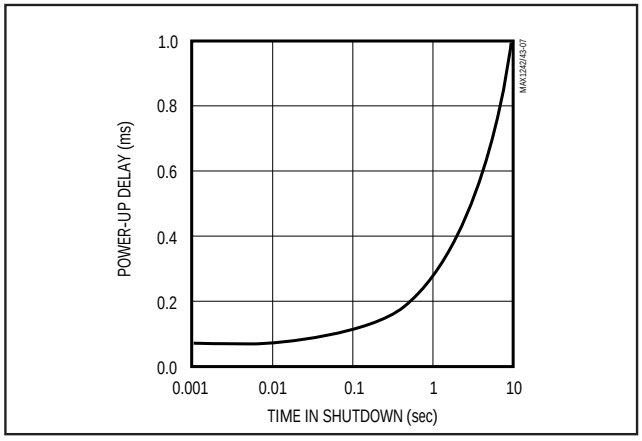


Figure 7. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

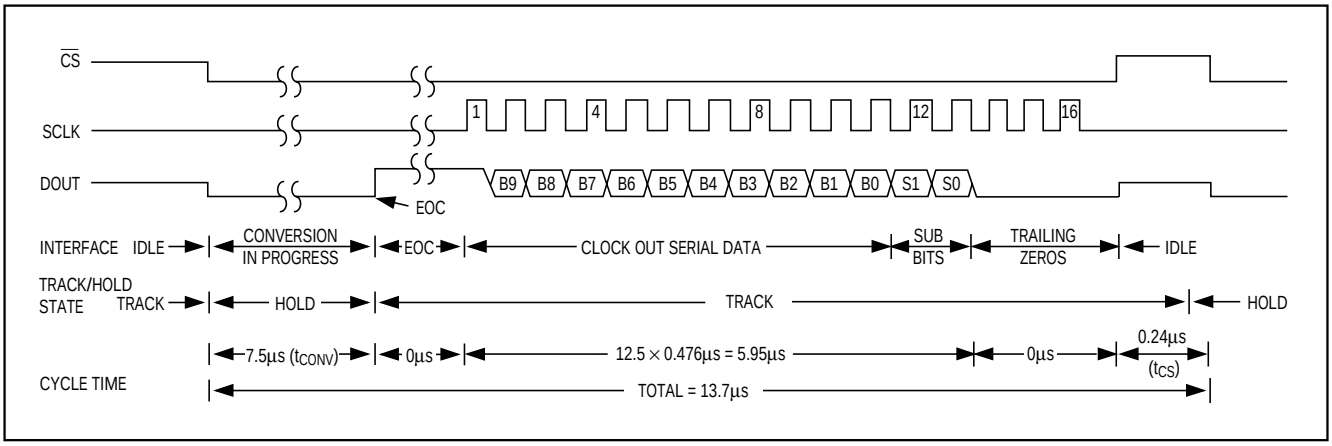


Figure 8a. Interface Timing Sequence

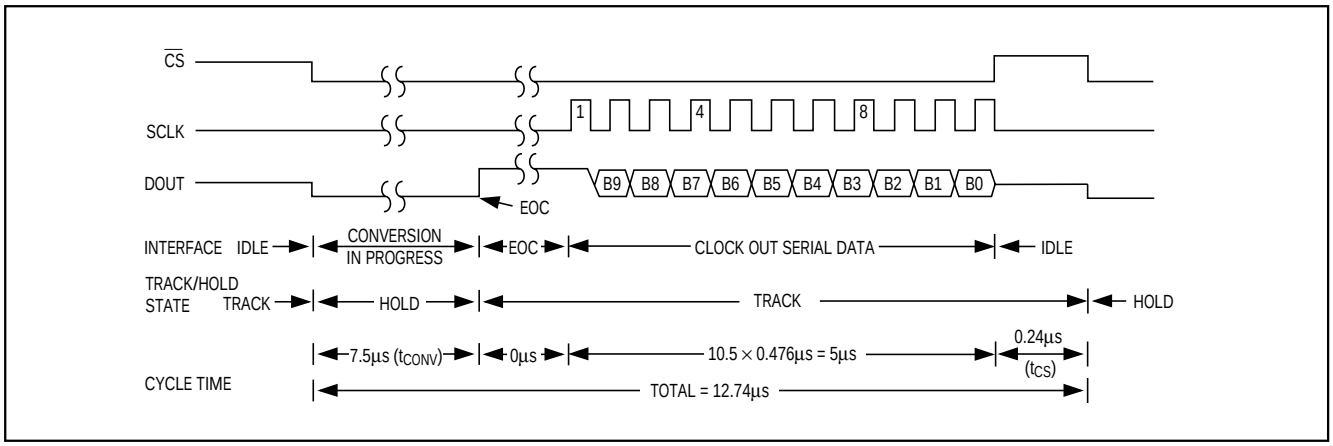


Figure 8b. Interface Timing Sequence—Minimum Cycle Time

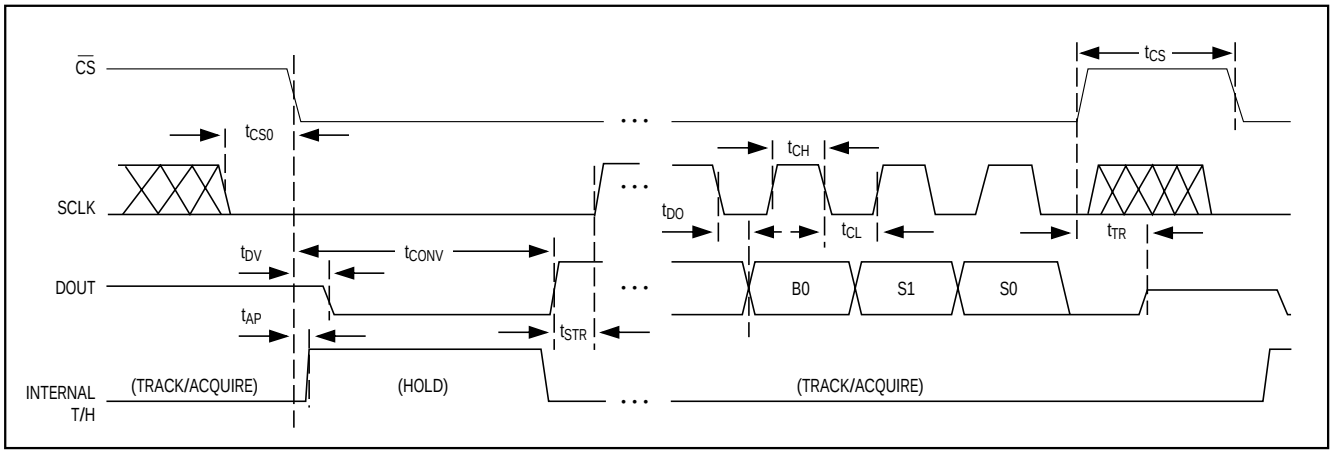


Figure 9. Detailed Serial-Interface Timing

+2.7V to +5.25V, Low-Power, 10-Bit Serial ADCs in SO-8

External Clock

The actual conversion does not require the external clock. This allows the conversion result to be read back at the µP's convenience at any clock rate up to 2.1MHz. The clock duty cycle is unrestricted if each clock phase is at least 200ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline serial-interface operation.

A $\overline{CS}$ falling edge initiates a conversion sequence: the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept low during the conversion. An internal register stores the data when the conversion is in progress.

EOC is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 10 data bits, two sub-bits, and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing zeros at DOUT and have no effect on converter operation.

For minimum cycle time, use DOUT's rising edge as the EOC signal and then clock out the data with 10.5 clock cycles at full speed (Figure 8b). Pull $\overline{CS}$ high after reading the conversion's LSB. After the specified minimum time, t_{CS}, pull $\overline{CS}$ low again to initiate the next conversion.

Output Coding and Transfer Function

The data output from the MAX1242/MAX1243 is binary. Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB values. If V_{REF} = 2.5V, then 1LSB = 2.44mV or 2.5V / 1024.

Applications Information

Connection to Standard Interfaces

The MAX1242/MAX1243 serial interface is fully compatible with SPI, QSPI, and Microwire standard serial interfaces (Figure 11).

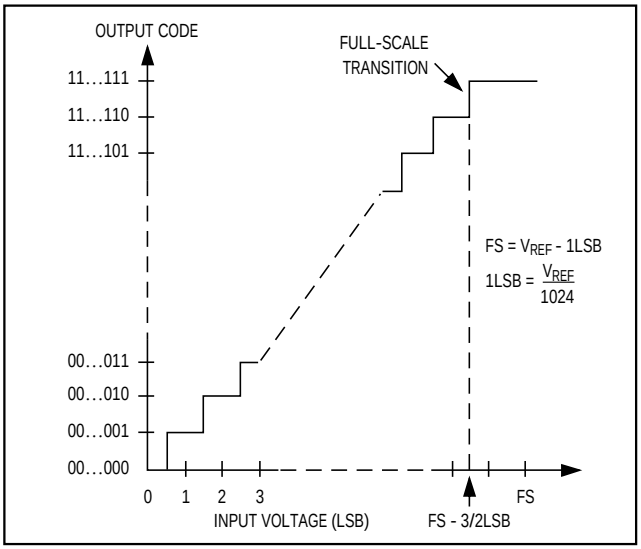


Figure 10. Unipolar Transfer Function, Full Scale (FS) = V_{REF} - 1LSB, Zero Scale (ZS) = GND

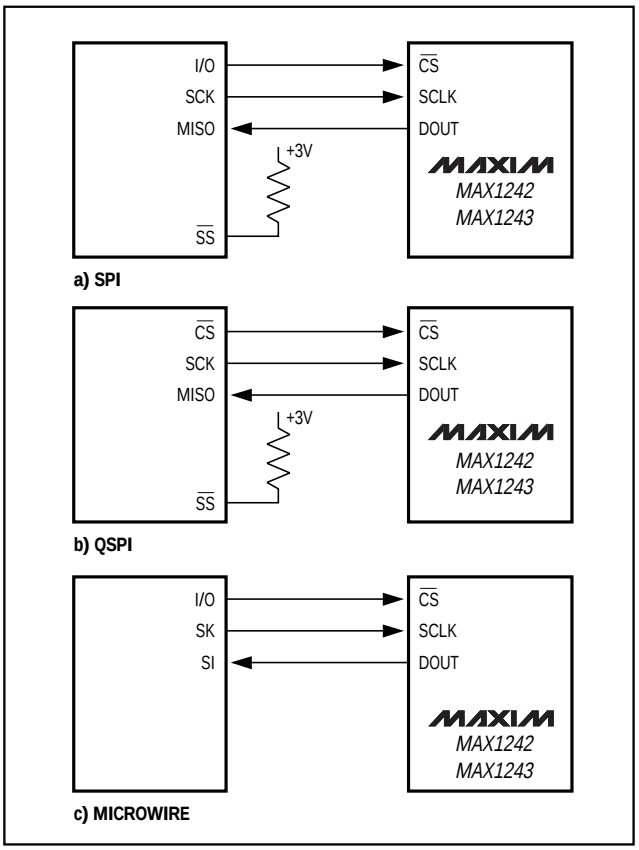


Figure 11. Common Serial-Interface Connections to the MAX1242/MAX1243

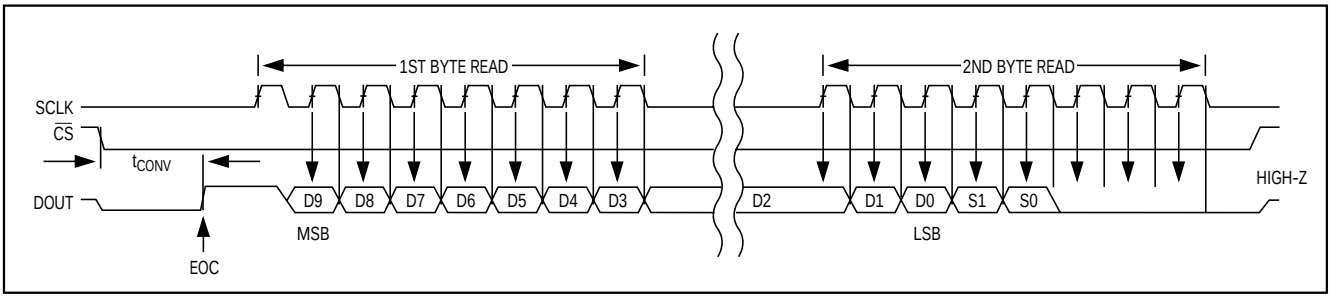


Figure 12. SPI/Microwire Serial-Interface Timing (CPOL = CPHA = 0)

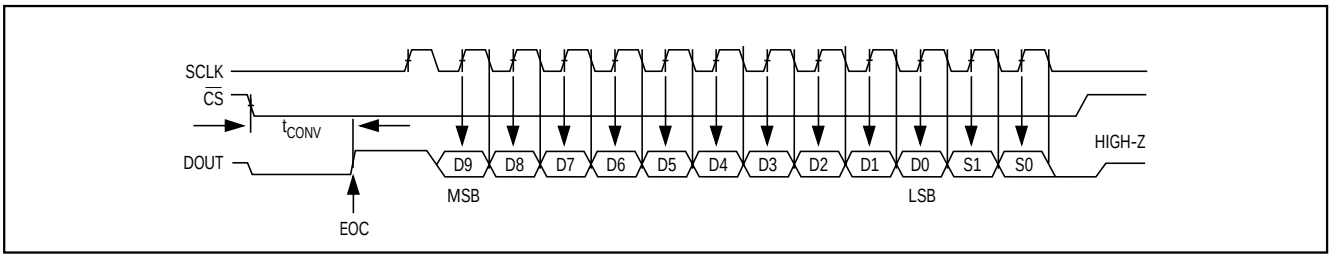


Figure 13. QSPI Serial-Interface Timing (CPOL = CPHA = 0)

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.1MHz.

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2) Wait the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3) Activate SCLK for a minimum of 11 clock cycles. The first falling clock edge produces the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK-to-DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4) Pull $\overline{CS}$ high at or after the 11th falling clock edge. If $\overline{CS}$ remains low, the two sub-bits and trailing zeros are clocked out after the LSB.
5) With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, before initiating a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversion's end, wait the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in two bytes or continuously, as shown in Figures 8a and 8b. The bytes contain the result of the conversion padded with one leading 1, two sub-bits, and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion is in progress. Wait until DOUT goes high or until the maximum specified 7.5µs conversion time elapses. Two consecutive 1-byte reads are required to get the full 10+2 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1, and seven bits of conversion result. The second byte contains the remaining three bits, two sub-bits, and three trailing zeros. See Figure 11 for connections and Figure 12 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 10 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1242/MAX1243 require 11 clock cycles from the µP to clock out the 10 bits of data. Additional clock cycles clock out the two sub-bits followed by trailing zeros (Figure 13). The maximum clock frequency to ensure compatibility with QSPI is 2.097MHz.

Layout and Grounding

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

+2.7V to +5.25V, Low-Power, 10-Bit Serial ADCs in SO-8

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1242AESA	-40°C to +85°C	8 SO	±1/2
MAX1242BESA	-40°C to +85°C	8 SO	±1
MAX1242AMJA	-55°C to +125°C	8 CERDIP*	±1/2
MAX1242BMJA	-55°C to +125°C	8 CERDIP*	±1
MAX1243ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1243BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1243ACSA	0°C to +70°C	8 SO	±1/2
MAX1243BCSA	0°C to +70°C	8 SO	±1
MAX1243AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1243BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1243AESA	-40°C to +85°C	8 SO	±1/2
MAX1243BESA	-40°C to +85°C	8 SO	±1
MAX1243AMJA	-55°C to +125°C	8 CERDIP*	±1/2
MAX1243BMJA	-55°C to +125°C	8 CERDIP*	±1

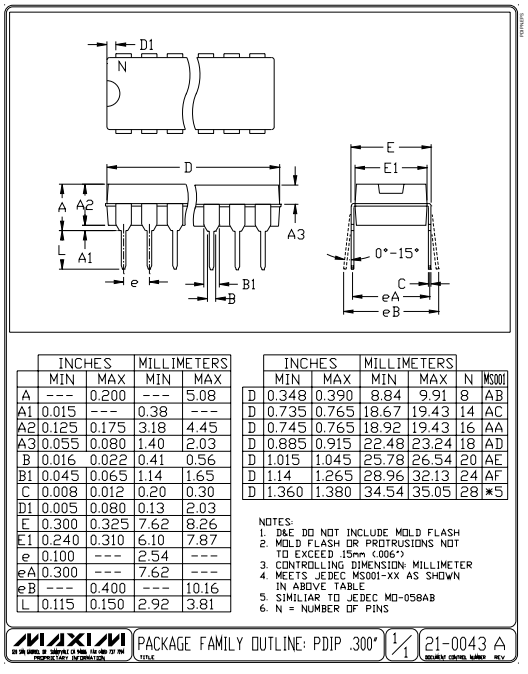
**Contact factory for availability and processing to MIL-STD-883.*
Note: *Order the MAX1242A in place of the MAX1242C. Order the MAX1242B in place of the MAX1242D.*

Chip Information

TRANSISTOR COUNT: 2559

SUBSTRATE CONNECTED TO GND

Package Information

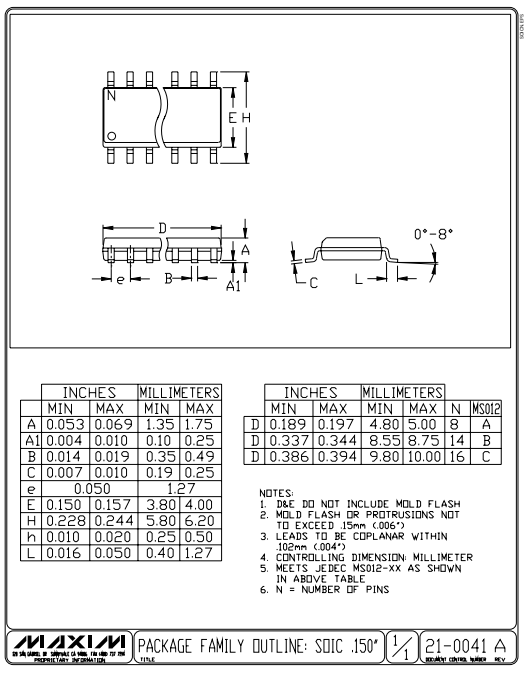


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A

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