ANALOG DEVICES

1 GSPS Direct Digital Synthesizer

Preliminary Technical Data AD9858

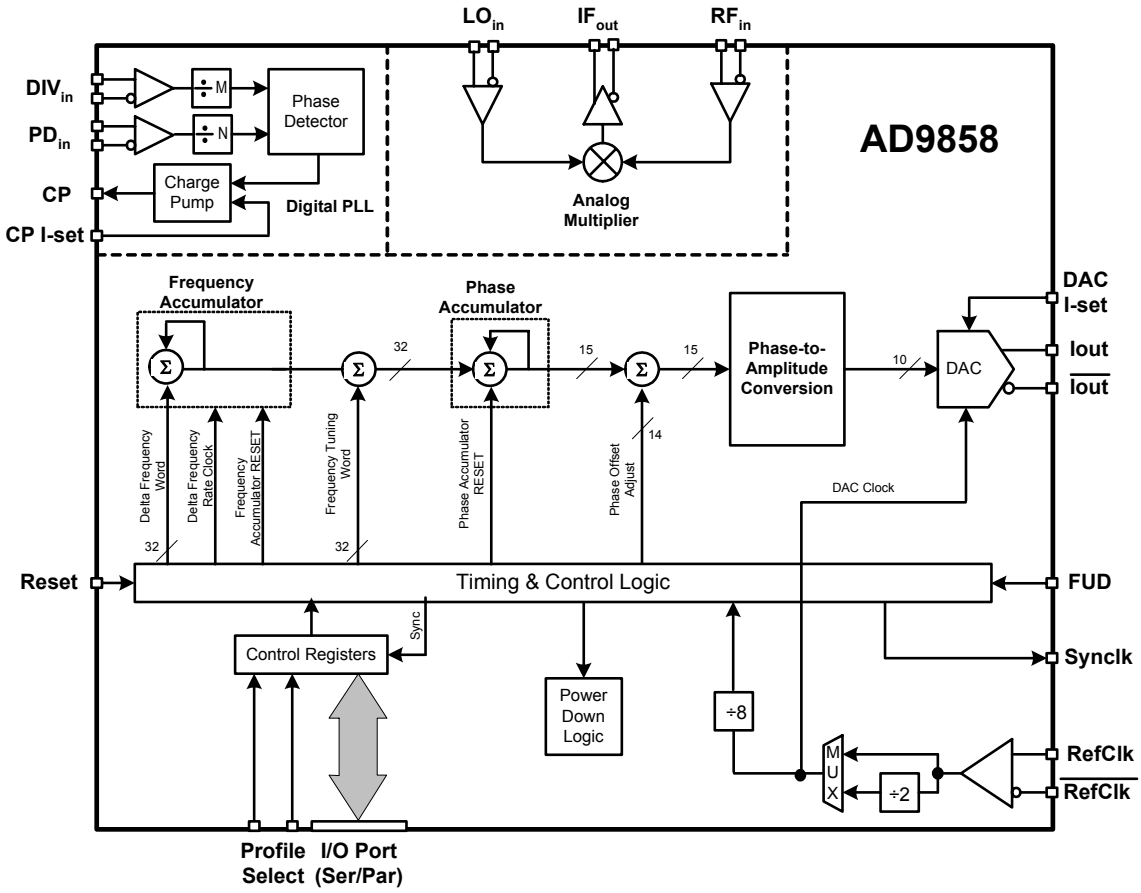
FEATURES

1 GSPS Internal Clock Speed
Up to 2GHz Input Clock (selectable divide by 2)
Integrated 10-bit D/A Converter
Phase Noise <130 dBc/Hz @ 1 kHz Offset (DAC output)
32-bit Programmable Frequency Register
Simplified 8-bit parallel and SPI Serial Control Interface
Automatic Frequency Sweeping capability
4 Frequency Profiles
3.3V Power Supply
Power Dissipation <2 Watts
100-lead EPAD-TQFP package
Integrated Programmable Charge Pump and Phase Frequency Detector with Fast Lock Circuit
Isolated Charge Pump Supply up to 5V
Integrated 2GHz Mixer

APPLICATIONS

VHF/UHF-LO Synthesis
Tuners
Instrumentation
Agile Clock Synthesis
Cellular Basestation Hopping Synthesizer
Radar
Sonet/SDH Clock Synthesis

Functional Block Diagram



REV PrB 1/28/2003

One Technology Way, P.O. Box 9106 Norwood MA 02062-9106, USA
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

CONTENTS

GENERAL DESCRIPTION

The AD9858 is a Direct Digital Synthesizer (DDS) featuring a 10-bit DAC operating up to 1GSPS. The AD9858 uses advanced DDS technology, coupled with an internal high-speed, high performance D/A converter to form a digitally-programmable, complete high-frequency synthesizer capable of generating a frequency-agile analog output sinewave at up to 400+ MHz. The AD9858 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9858 via parallel (8-bit) or serial loading formats. The AD9858 contains an Integrated Charge Pump (CP) and Phase Frequency Detector (PFD) for synthesis applications requiring the combination of a high speed DDS along with Phase Locked Loop (PLL) functions. An analog mixer is also provided on-chip for applications requiring the combination of a DDS, PLL and Mixer, such as frequency translation loops, tuners, etc. The AD9858 also features a divide-by-two on the clock input, allowing the external clock to be as high as 2 GHz.

The AD9858 is specified to operate over the extended industrial temperature range of -40° to +85°C.

ABSOLUTE MAXIMUM RATINGS *

Maximum Junction Temp ..... +150° C
AV_{DD} ..... +4 V
DV_{DD} ..... +4 V
CPV_{DD} ..... +6 V
Digital Input Voltage ..... -0.7 V to $+V_{DD}$
Digital Output Current ..... 5 mA
Storage Temperature ..... -65° C to +150° C
Operating Temp ..... -40° C to +85° C
Lead Temp. (10 sec. soldering) ..... +300° C
θ_{JA} ..... 25° C/W
θ_{JC} ..... tbd° C/W

***** Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

AD9858 PRELIMINARY ELECTRICAL SPECIFICATIONS

(Unless otherwise noted: V_{DD}=+3.3V ±5%, CPV_{DD}=5V ±5%, R_{SET}=2 kΩ, C_{PISET}=2.4kΩ, Reference Clock Frequency=1GHz)

Parameter	Temp	Test Level	AD9858 Min	AD9858 Typ	AD9858 Max	Units
REF CLOCK INPUT CHARACTERISTICS[1]						
Reference Clock Frequency Range (Divider Off)	FULL	VI	10		1000	MHz
Reference Clock Frequency Range (Divider On)	FULL	VI	20		2000	MHz
Duty Cycle	+25°C	V		50		%
Input Capacitance	+25°C	V		3		pF
Input Impedance	+25°C	IV		1500		Ω
DAC OUTPUT CHARACTERISTICS						
Resolution				10		Bits
Full-Scale Output Current			5	20	40	mA
Gain error	+25°C	I	-10		+10	%FS
Output Offset	+25°C	I			1	uA
Differential Non-linearity	+25°C	I		0.5	1	lsb
Integral Non-linearity	+25°C	I		1	1	lsb
Output Impedance	+25°C	I		100		kΩ
Voltage Compliance Range	+25°C	I	AV_{DD} - 1.5		AV_{DD} +0.5	V
Wideband SFDR (DC to Nyquist)						
40 MHz Fout	+25°C	V		64		dBc
100 MHz Fout	+25°C	V		60		dBc
180 MHz Fout	+25°C	V		58		dBc
360 MHz Fout	+25°C	V		52		dBc
Narrowband SFDR[3]						
40 MHz Fout (± 15 MHz)	+25°C	V		75		dBc
40 MHz Fout (± 1 MHz)	+25°C	V		80		dBc
40 MHz Fout (± 50 kHz)	+25°C	V		84		dBc
100 MHz Fout (± 15 MHz)	+25°C	V		75		dBc
100 MHz Fout (± 1 MHz)	+25°C	V		80		dBc
100 MHz Fout (± 50 kHz)	+25°C	V		84		dBc
180 MHz Fout (± 15 MHz)	+25°C	V		75		dBc
180 MHz Fout (± 1 MHz)	+25°C	V		80		dBc
180 MHz Fout (± 50 kHz)	+25°C	V		84		dBc
360 MHz Fout (± 15 MHz)	+25°C	V		75		dBc
360 MHz Fout (± 1 MHz)	+25°C	V		80		dBc
360 MHz Fout (± 50 kHz)	+25°C	V		84		dBc
OUTPUT PHASE NOISE CHARACTERISTICS (@40MHz I_{out})						
@ 1 kHz offset	+25°C	V		130		dBc/Hz
@ 10 kHz offset	+25°C	V		135		dBc/Hz
@ 100 kHz offset	+25°C	V		140		dBc/Hz
OUTPUT PHASE NOISE CHARACTERISTICS (@180MHz I_{out})						
@ 1 kHz offset	+25°C	V		130		dBc/Hz
@ 10 kHz offset	+25°C	V		135		dBc/Hz
@ 100 kHz offset	+25°C	V		140		dBc/Hz

AD9858 PRELIMINARY ELECTRICAL SPECIFICATIONS

(Unless otherwise noted: V_{DD}=+3.3V ±5%, CPV_{DD}=5V ±5%, R_{SET}=2 kΩ, CP_{ISET}=2.4kΩ, Reference Clock Frequency=1GHz)

PHASE DETECTOR and CHARGE PUMP						
Phase Detector Frequency	+25°C	VI			150	MHZ
Charge Pump Sink and Source Current [4]	+25°C	VI			2	mA
Fast Lock Current (acquisition only)	+25°C	VI			7.5	mA
Open Loop Current (acquisition only)	+25°C	VI			30	mA
Sink And Source Current Absolute Accuracy [5]	+25°C	VI			5	%
Sink and Source Current Matching [5]	+25°C	VI			3	%
Input Sensitivity PD_{IN} and DIV_{IN} (50ohms)[6]	+25°C	VI	-5		0	dBm
Input Impedence PD_{IN} and DIV_{IN} (single-ended)	+25°C	V		1		k Ω
Phase Noise @100MHZ Input Frequency						
@10kHZ offset	+25°C	V		110		dBc/Hz
@100kHZ offset	+25°C	V		140		dBc/Hz
@1MHZ offset	+25°C	V		148		dBc/Hz
Charge Pump Output Range [7]	+25°C	V	0		CPV_{DD}	V
MIXER						
IF_{OUT} [8]	+25°C	V		400		MHz
F_{RF}	+25°C	VI			2	GHz
F_{LO}	+25°C	VI			2	GHz
Conversion Gain	+25°C	VI	tbd	3.5	tbd	dB
LO Level	+25°C	VI	-6		6	dBm
RF Level	+25°C	VI	-40		0	dBm
RF Input Sensitivity (50ohms)	FULL		-10		2	dBm
Input IP3	+25°C	VI		11		dBm
Noise Figure	+25°C	V		tbd		dB
1dB input compression power[9]	+25°C	VI	tbd	1.5	tbd	dBm
Input Impedance (single-ended)						
LO	+25°C	V		1		k Ω
RF	+25°C	V		1		k Ω
LOGIC INPUTS						
Logic "1" Voltage	+25°C	VI	2.0			V
Logic "0" Voltage	+25°C	VI			0.8	V
Logic "1" Current	+25°C	VI			12	uA
Logic "0" Current	+25°C	VI			12	uA
Input Capacitance	+25°C	V		3		pF
POWER SUPPLY						
P_{DISS} (Worst Case Conditions – everything on PFD input freq 150MHz)	+25°C	I		1.9		W
P_{DISS} (Power-down Mode)	+25°C	I		10		mW
P_{DISS} Mixer only	+25°C	I				mW
P_{DISS} PFD and CP (@150MHz) only	+25°C	I				mW
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	Full	IV			10	MHz
Minimum Clock Pulse Width Low (t_{PWL})	Full	IV	30			ns
Minimum Clock Pulsewidth High (t_{PWH})	Full	IV	30			ns
Maximum Clock Rise/Fall Time	Full	IV			1	ms
Minimum Data Setup Time (t_{DS})	Full	IV	25			ns
Mimimum Data Hold Time (t_{DH})	Full	IV	0			ns
Maximum Data Valid Time (t_{DV})	Full	IV	30			ns
Parallel Control Bus						
Ref Clk to Sync Clk	Full	V		tbd		ns

NOTES
[1] The reference clock input is configured to accept a differential or single-ended sinewave input or a 3 V CMOS-level pulse input.
[2] Refclk input is internally DC biased. AC coupling should be used.
[3] Reference clock frequency is selected to insure second harmonic is out of the bandwidth of interest.
[4] The Charge Pump current is programmable in four discrete steps.
[5] For $0.5<V_{CP}<CPV_{DD}-0.75V$
[6] These differential inputs are internally DC biased. AC coupling should be used.
[7] The Charge Pump Supply Voltage can range from 3.135 to 5.25V
[8] Output interface is differential open collector
[9] For 1dB output compression; input power measured at 50 Ω

EXPLANATION OF TEST LEVELS

I – 100% Production Tested.
III – Sample Tested Only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for industrial operating temperature range.

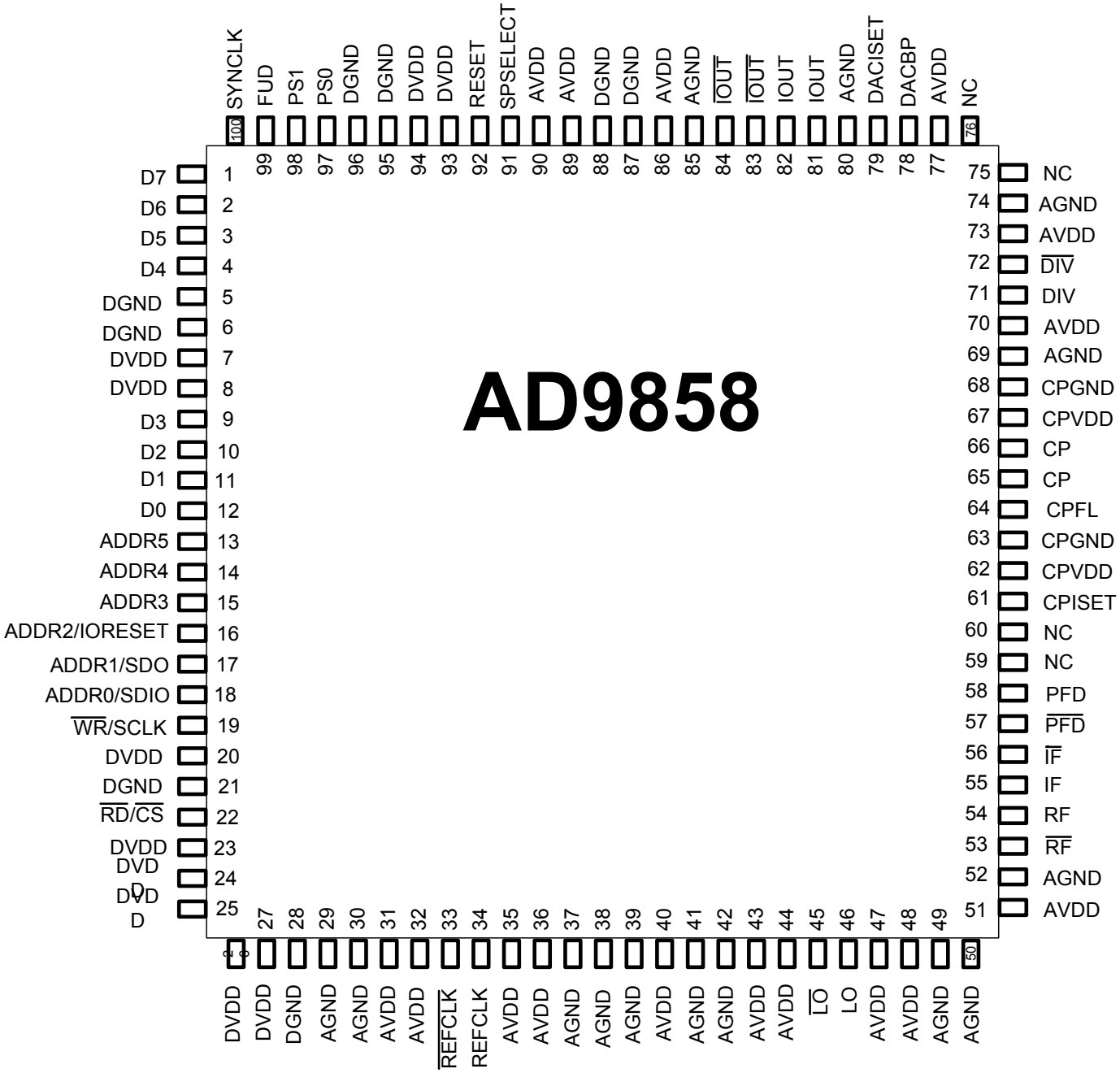
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9858BSV	-40°C to +85°C	100-lead EPAD	SV-100
AD9858PCB	+25°C	Evaluation Board	

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9858 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD9858

AD9858 Pinout



Pin Function Descriptions

Pin #	Pin Name	I/O	Description
1 – 4, 9 – 12	D7 – D0	I/O	Parallel port DATA. NOTE: The functionality of these pins is only valid when the I/O port is configured as a Parallel Port.
5, 6, 21, 28, 87, 88, 95, 96	DGND	-	Digital ground.
7, 8, 20, 23-27, 93, 94	DVDD	-	Digital supply voltage.
13 - 18	ADDR5 - ADDR0	I	When the I/O port is configured as a Parallel Port these pins serve as a 6-bit Address select for accessing the on-chip registers. (see IORESET, SDO, and SDIO pins below for Serial Port mode).
(16)	IORESET	I	NOTE: Only valid for Serial Programming Mode. Active high input signal which resets the serial I/O bus controller. It is intended to serve as a means of recovering from an unresponsive serial bus caused by improper programming protocol. Asserting an I/O Reset does not affect the contents of previously programmed registers, nor does it invoke their default values.
(17)	SDO	O	NOTE: Only valid for Serial Programming Mode. When operating the I/O port as a *3-wire* serial port this pin serves as a unidirectional serial data output pin. When operated as a *2-wire* serial port this pin is unused.
(18)	SDIO	I or I/O	NOTE: Only valid for Serial Programming Mode. When operating the I/O port as a *3-wire* serial port this pin is the serial data input. When operated as a 2-*wire* serial port this pin is the bidirectional serial data pin.
19	WR/ SCLK	I	When the I/O port is configured for Parallel Programming Mode this pin functions as an active low write pulse (WR). When configured for Serial Programming Mode this pin functions as the serial data clock (SCLK).
22	RD/ CS	I	When the I/O port is configured for Parallel Programming Mode this pin functions as an active low read pulse (RD). When configured for Serial Programming Mode this pin functions as an active low Chip Select (CS) that allows multiple devices to share the serial bus.
29, 30, 37-39, 41, 42, 49, 50, 52, 69, 74, 80, 85	AGND	I	Analog Ground.

31, 32, 35, 36, 40, 43, 44, 47, 48, 51, 70, 73, 77, 86,89,90	AVDD	I	Analog Supply Voltage.
33	REFCLK	I	Reference Clock complementary input (2 GHz max). NOTE: When the REFCLK port is operated in single-ended mode REFCLK should be decoupled to AVDD with a 0.1µF capacitor.
34	REFCLK	I	Reference Clock input (2 GHz max).
45	LO	I	Mixer Local Oscillator (LO) complementary input (2 GHz max). **NOTE:** When the LO port is operated in single-ended mode LO should be decoupled to AVDD with a 0.1µF capacitor.
46	LO	I	Mixer Local Oscillator (LO) input (2 GHz max).
53	RF	I	Analog Mixer RF complementary input (2 GHz max). **NOTE:** When the RF port is operated in single-ended mode RF should be decoupled to AVDD with a 0.1µF capacitor.
54	RF	I	Analog Mixer RF input (2 GHz max).
55	IF	O	Analog Mixer IF output (tbd MHz max).
56	IF	O	Analog Mixer IF complementary output (tbd MHz max).
57	PFD	I	Phase Frequency Detector complementary input (150 MHz max directly, 400MHz when /4 option enabled).When PFD port is operated in single-ended mode PFD should be decoupled to AVDD with a 0.1µF capacitor.
58	PFD	I	Phase Frequency Detector input (150 MHz max directly, 400MHz when /4 option enabled).
59, 60, 75, 76	NC	-	No connection.
61	CPISET	I	Charge Pump output current control. A resistor connected from CPISET to CPGND establishes the reference current for the charge pump.
62, 67	CPVDD	I	Charge pump supply voltage.
63, 68	CPGND	I	Charge pump ground.
64	CPFL	O	Charge Pump Fast Lock output.
65, 66	CP	O	Charge Pump output.
71	DIV	I	Phase Frequency Detector Feedback input (150MHz max directly, 400MHz when /4 option enabled).
72	DIV	I	Phase Frequency Detector Feedback complementary input (150MHz max directly, 400MHz when /4 option enabled). **NOTE:** When the DIV port is operated in single-ended mode DIV should be decoupled to AVDD with a 0.1µF capacitor.
78	DACBP	-	DAC baseline decoupling pin, typically bypassed to pin 77 with a 0.1µF capacitor.
79	DACISET	I	A resistor connected from DACISET to AGND establishes the reference current for the DAC.
81, 82	IOUT	O	DAC output.

83, 84	IOUT	O	DAC complementary output.
91	SPSELECT	I	I/O port Serial/Parallel Programming Mode select pin. Logic 0: SERIAL programming mode. Logic 1: PARALLEL programming mode.
92	RESET	I	Active high hardware reset pin. Assertion of the RESET pin forces the AD9858 to its default operating conditions.
97, 98	PS0, PS1	I	Used to select one of the four internal profiles. These pins are synchronous to the SYNCLK output.
99	FUD	I	Frequency Update. The rising edge transfers the contents of the internal buffer registers to the Memory registers. This pin is synchronous to the SYNCLK output.
100	SYNCLK	O	Clock output pin which serves as a synchronizer for external hardware. SYNCLK runs at REFCLK/8

Theory of Operation

Overview

The AD9858 direct digital synthesizer (DDS) is a flexible device that can address a wide range of applications. The device consists of an NCO with a 32-bit phase accumulator, 14-bit phase offset adjustment, a power-efficient DDS core, and a one giga-samples per second (1 GSPS) 10-bit digital-to-analog converter. The AD9858 incorporates additional capabilities for automated frequency sweeping. The device also offers an analog mixer capable of operating at 2 GHz, a phase-frequency detector (PFD), and a programmable charge pump (CP) with advanced fast-lock capability. These RF building blocks can be used for various frequency synthesis loops, or as needed in the system design.

The AD9858 can directly generate frequencies up to 400+ MHz when driven at a 1 GHz internal clock speed. This clock can be derived from an external clock source of up to 2 GHz by using the on-chip divide-by-2 feature. The on-chip mixer and PFD/CP make possible a variety of synthesizer configurations capable of generating frequencies in the 1-2 GHz range, or higher.

The AD9858 offers the advantages of a DDS with the additional flexibility to work in concert with analog frequency synthesis techniques (PLL, mixing) to generate precision frequency signals with high frequency resolution, fast frequency hopping, fast settling time, and automated frequency sweeping capabilities.

The AD9858 is easily configured by writing data to its on-chip digital registers that control all operations of the device. The AD9858 offers a choice of both serial and parallel ports for controlling the device. There are four user profiles that can be selected by a pair of external pins. These profiles allow independent setting of the frequency tuning word and the phase offset adjustment word for each of four selectable configurations.

AD9858

The AD9858 can be programmed to operate in single tone mode or in a frequency-sweeping mode. To save on power consumption, there is also a programmable full-sleep mode, during which most of the device is powered down to reduce current flow.

The operation of a DDS is described in detail in a tutorial available from Analog Devices at **http://www.analog.com/dds**.

Component Blocks

DDS Core

The DDS core generates the numeric values that represent a sinusoid in the digital domain. Depending on the operating mode of the DDS, this sinusoid may be changed in frequency, phase, or perhaps modulated by an information carrying signal. The frequency of the output signal is determined by a user-programmed frequency tuning word (FTW). The relation of the output frequency of the device to the system clock (SYSCLK) is determined by the following equation: $Fo = \frac{(FTWxSYSCLK)}{2^N}$, where for the AD9858 N = 32. For a more detailed explanation of a DDS core, please consult the DDS tutorial at http://www.analog.com/dds.

DAC Output

The AD9858 incorporates an integrated 10-bit current output DAC. Two complementary outputs provide a combined full-scale output current (I_{out}). Differential outputs reduce the amount of common-mode noise that might be present at the DAC output, offering the advantage of an increased signal-to-noise ratio. The full-scale current is controlled by means of an external resistor (R_{set}) connected between the DACISET pin and analog ground. The full-scale current is proportional to the resistor value as follows:

$$R_{set} = 39.19/I_{out}$$

The maximum full-scale output current of the combined DAC outputs is 20mA, but limiting the output to 10mA provides the best spurious-free-dynamic-range (SFDR) performance. The DAC output compliance range is (AVDD-1.5V) to (AVDD +0.5V). Voltages developed beyond this range will cause excessive DAC distortion and could potentially damage the DAC output circuitry. Proper attention should be paid to the load termination to keep the output voltage within this compliance range. When terminating the differential outputs into a transformer, the center tap should be referenced to AVDD.

PLL Frequency Synthesizer

The PLL frequency synthesizer is a group of independent synthesis blocks, designed to be used with the DDS to expand the range of synthesis applications. These blocks are a digital Phase Frequency Detector (**PFD**) that drives a Charge Pump (**CP**). The Charge Pump incorporates Fast-Locking Logic, described below. Based on system requirements, the user supplies an external loop-filter and one or more VCO's. A high-speed analog mixer is included for translation synthesis loops. Using the different blocks in the PLL frequency synthesizer in conjunction with the DDS,

the user can create translation loops (also known as offset loops), fractional divider loops, as well as traditional PLL loops to multiply the output of the DDS in frequency.

Phase-Frequency Detector

The Phase Detector has two inputs, PD_{in} and DIV_{in}. Both are analog inputs that can be operated in differential or single-ended mode. Both are designed to operate at frequencies up to 150MHz, although signals of up to 400MHz can be accommodated on the inputs when the divide-by-four functions are used. The expected input level for both the PD and DIV inputs is in the range of 800mV peak-to-peak (differential), 400mV peak-to-peak (single-ended). A programmable divider that offers division ratios of M, N = {1, 2, 4} immediately follows the input. The division ratio is controlled by means of the Control Function Register.

Charge Pump

The Charge Pump output reference current is determined by an external resistor (~2.4KΩ) which establishes a 500μA maximum internal baseline current ($\mathbf{I_{CP0}}$). The baseline current is scaled to provide the appropriate drive current for the CP's various operating modes (*frequency detect mode*, *wide closed-loop*, and *final closed-loop*). The amount of scaling in each mode is programmable by means of the values stored in the Control Function Register, giving the user maximum flexibility of the PLL's frequency locking capability.

The CP polarity can be configured as either positive or negative with respect to the PD input. When the CP polarity is positive, if the DIV input leads the PD input, the charge pump will attempt to decrease the voltage at the VCO control node. If the DIV input lags the PD input, the charge pump will work to increase the voltage at the VCO control node. When the CP polarity is negative, the opposite occurs. This allows the user to define either input as the feedback path. This also allows the AD9858 to accommodate ground-referenced or supply-referenced VCOs. This functionality is defined by Charge Pump Polarity (CPP) bit in the Control Function Register. When CPP = 0 (*default*), the Charge Pump is set up for operation with a ground-referenced VCO. When CPP = 1, the Charge Pump is set up for a supply-referenced VCO.

Internal to the CP, the I_{CP0} current is scaled to provide different output drive current values for the various modes of operation. The final closed loop mode can be programmed to scale I_{CP0} by 1, 2, 3 or 4. The wide closed-loop mode can be programmed to scale I_{CP0} by 0, 2, 4, 6, 8, 10, 12 or 14. The frequency detect mode can be programmed to scale I_{CP0} by 0, 20, 40 or 60. The different modes of operation, controlled by the fast-locking logic, are discussed in the next section.

The CP has an independent set of power pins that can operate at up to 5.25 volts. While the device can operate from ground to rail, the voltage compliance should be kept in the range of 0.5 to 4.5V to ensure the best steady-state performance. The combination of programmable output current, programmable polarity, wide compliance range and proprietary fast-lock capability offers the flexibility necessary for the digital PLL to operate within a broad range of PLL applications.

Fast Locking Logic

The Charge Pump includes a fast-locking algorithm that helps to overcome the traditional limitations of PLLs with regards to frequency switching time. The Fast Lock algorithm works in conjunction with the loop filter shown in figure N to provide extremely fast frequency switching performance.

Based on the error seen between the feedback signal and the reference signal, the fast locking algorithm puts the charge pump into one of three states: frequency detect mode; a wide closed-loop mode and a final closed-loop mode. In the frequency detect mode, the feedback and reference signals are registering substantial phase and frequency errors. Rather than operating in a continuous closed loop feedback mode, the charge pump supplies a fixed current of the correct polarity to the VCO control node that drives the loop towards frequency lock. Once frequency lock is detected, the fast locking logic shifts the part into one of the closed loop modes. In the closed loop modes, either wide or final, the charge pump supplies current to the loop filter as directed by the phase-frequency detector PFD. The frequency-detect mode is intended to bring the system to a level of frequency lock from which the intermediary closed-loop system will be able to quickly achieve phase lock.

The level of frequency lock accuracy aimed for is typically referred to as the lock range. Once the frequency is within the lock range, the time required to achieve phase lock can be determined by standard PLL transient analysis methods. Note that the charge pump current sources associated with the frequency detect mode are connected to pin 64, while the closed loop current sources are connected to pins 65 and 66. Pin 64 is connected directly to the loop filter zero compensation capacitor as shown in Fig N. This connection allows the smoothest transition from the frequency detect mode to the closed loop modes and enables faster overall switching times. Pins 65 and 66 are connected to the loop filter in the conventional manner.

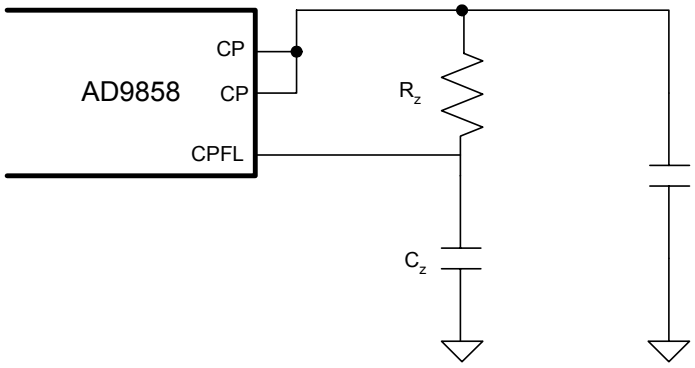


Figure N Symbolic Representation of the Charge Pump to Loop Filter Connection

The frequency detection block works as follows. The comparison logic in the frequency detection circuitry operates one eighth of the DDS system clock. A comparison is made of the frequencies present at the PD Input and the DIV Input over nineteen DDS clock cycles.

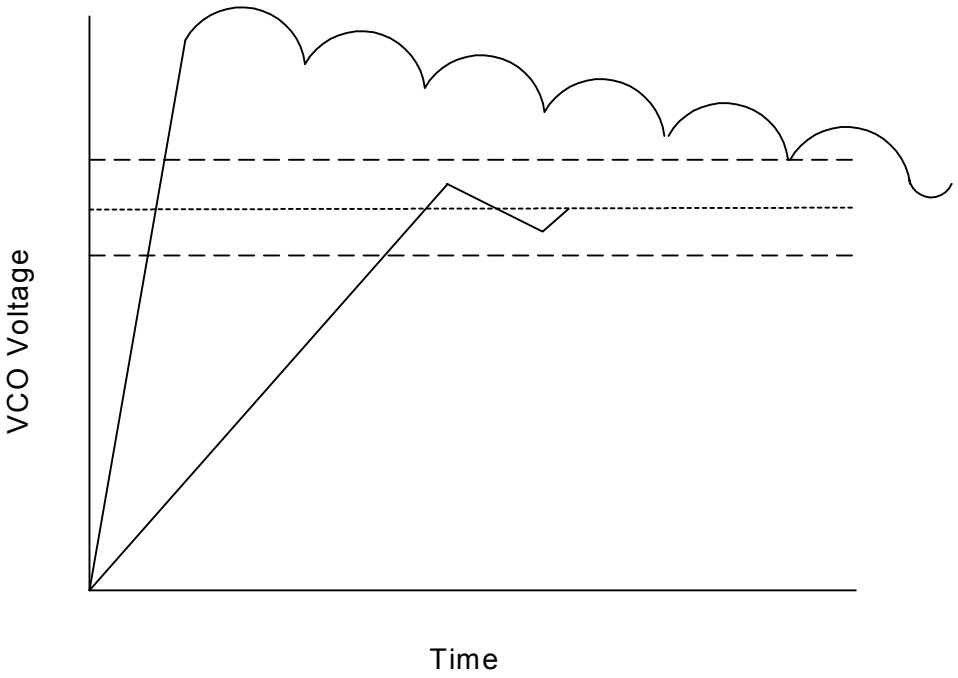
In order to insure that frequency lock detection is achieved while the frequency difference is within the PLL Lock range, the slew rate of the VCO input should be limited such that the Lock range cannot be traversed within nineteen DDS clock cycles. The slew rate of the VCO input is

determined by the programmed level of frequency detect current and the size of the zero compensation capacitor according to the following relation: $\frac{dV}{dt} = \frac{I_{f\,\det}}{C_z}$.

Once frequency detection occurs, the loop will be closed and the loop will lock based on the current programmed for the wide closed loop mode. It is important that the loop is designed for closed loop stability while in the wide closed loop mode. In this mode, less phase margin can usually be tolerated as this mode is just used to enhance the lock time but is not used in the "locked" free running state. Once the wide closed loop mode achieves phase lock as determined by an internal lock detector, the phase-detector/charge pump will transition into the final closed loop state. If no wide closed loop current is programmed, the loop will transition directly from the frequency detect mode into the final closed loop state. In the final closed loop state the loop characteristics should be optimized for the desired free running loop bandwidth.

The frequency detect mode is primarily useful in offset, or translation loop applications where the phase detector inputs are more likely to be detect large frequency transitions. For loop applications where there are significant amounts of division in the feedback loop, the frequency detection mode may not activate. This is due to the limited amount of frequency difference that is experienced at the phase detector inputs. For these applications the primary means of accelerating frequency settling time is to design the loop to acquire lock with the wide closed loop setting and then switching to the final closed loop setting since they are usually close to being within the lock range anyway.

As mentioned earlier, care should be taken when planning for a large transition using the frequency detect mode to ensure that the charge pump does not cause the VCO to overshoot the closed-loop range, as cycle slipping could occur which would result in extended delays. The figure below shows two system responses. In the first, the Charge Pump output current is maximized during the frequency-detect mode so that after 19 clock cycles, the VCO voltage has exceeded the closed-loop lock range. The second system provides less current during the frequency detect mode. While this results in a longer delay in approaching the closed-loop lock range, because the system does not exceed the closed-loop range, the fast-locking logic shifts the charge pump into intermediary closed-loop mode, resulting in a shorter overall frequency switching time.



Analog Mixer

The analog mixer is included for translation loops, also known as offset loops. The RF (Radio Frequency) and LO (Local Oscillator) inputs are designed to operate at frequencies up to 2GHz. Both inputs are differential analog input stages. Both input stages are internally DC biased and should be connected through an external AC coupling mechanism. The expected input level is in the range of 800mV peak-to-peak (differential). The IF (Intermediate Frequency) output is a differential analog output stage designed to operated at frequencies under 400MHz. This mixer is based on the Gilbert Cell architecture.

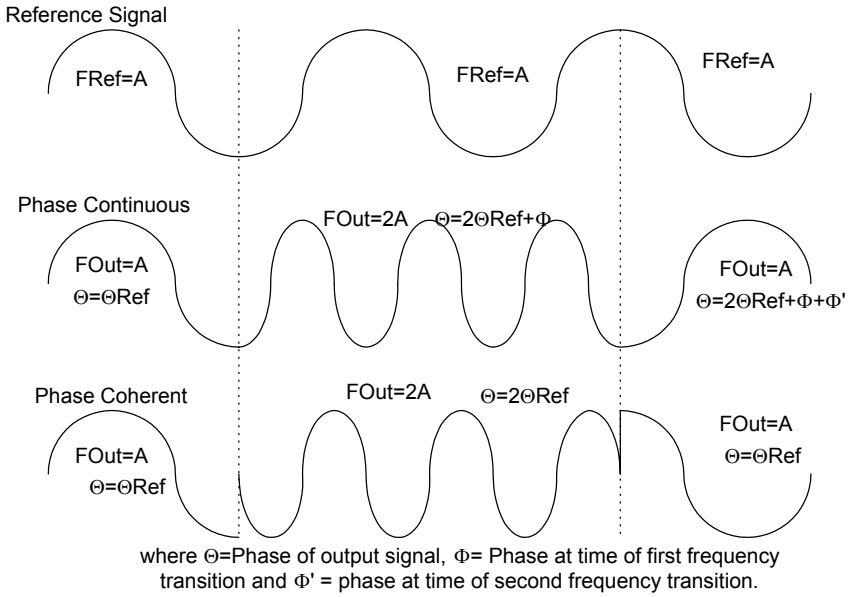
Modes of Operation

The AD9858 DDS section has three modes of operation – single-tone, frequency sweeping and full-sleep. The RF building blocks (PFD, CP, Mixer) can be active or powered down, used or unused, in either of the active modes.

In the single-tone mode the device generates a single output frequency determined by a 32-bit word (frequency tuning word – FTW) loaded to an internal register. This frequency can be changed as desired, and frequency hopping can be accomplished at a rate limited only by the time required to update the appropriate registers. If even faster hopping is desired, the 4 profiles allow rapid hopping among the 4 frequencies stored in them by means of external select pins.

The frequency-sweeping mode allows for the automation of most of the frequency-sweeping task, making chirp and other frequency-sweeping applications possible without the inconvenience and possible speed limitations imposed by multiple register operations via the I/O port.

Whichever mode the device is operating in, changes in frequency are phase-continuous, which means that changes in frequency do not cause discontinuities in the phase of the output signal. The first phase value after a frequency change is an increment of the last phase value before the change, but at the new tuning word's phase increment value (FTW). (Note: This is not the same as phase-coherent over frequency changes; see Fig # below.)



Single-Tone Mode

When in single-tone mode, the AD9858 generates a signal, or tone, of a single desired frequency. This frequency is set by the value loaded by the user into the chip's frequency tuning word (FTW) register. This frequency can be between 0 Hz and somewhat below one-half of the DAC sampling frequency (SYSCLK). One-half of the sampling frequency is commonly called the "Nyquist" frequency. The practical upper limit to the fundamental frequency range of a DDS is determined by the characteristics of the external low-pass filter, known as the reconstruction filter, which must follow the DAC output of the DDS. This filter reconstructs the desired analog sine-wave output signal from the stream of sampled amplitude values output by the DAC at the sample rate (SYSCLK).

A DDS is a sampled-data system (see Fig. xx, sampled data spectrum, with sinc envelope, showing fundamental, Nyquist, and images). As the fundamental frequency of the DDS approaches the Nyquist frequency, the lower first image approaches the Nyquist frequency from above. As the fundamental frequency approaches the Nyquist frequency, it becomes difficult, and finally impossible, to design and construct a low-pass filter which will provide adequate attenuation for the first image frequency component.

The maximum usable frequency in the fundamental range of the DDS is typically between 40% and 45% of the Nyquist frequency, depending on the reconstruction filter. With a 1 GHz SYSCLK, the AD9858 is capable of producing maximum output frequencies of between 400 MHz and 450 MHz, depending on the reconstruction filter and the application system requirements.

For a desired output frequency (FO) and sampling rate (SYSCLK), the frequency tuning word (FTW) of the AD9858 is calculated according to the following equation:

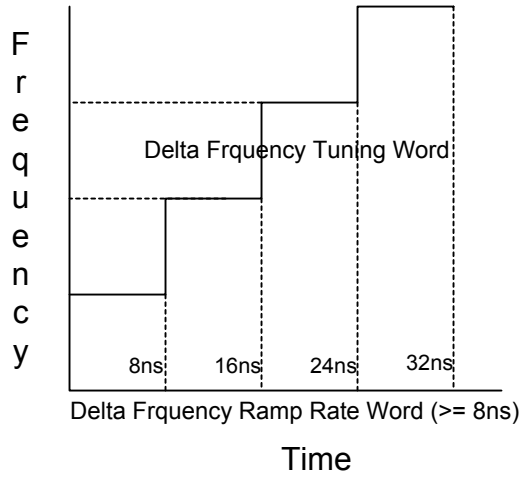
$$FTW=(FO * 2^N) / SYSCLK$$

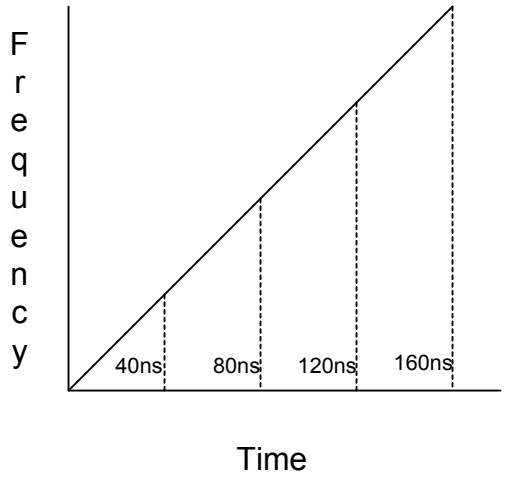
Where N is the phase accumulator resolution in bits (32 in the AD9858), FO is in Hz, and the FTW is a decimal number. Once a decimal number has been calculated, it must be rounded to an integer and converted to a 32-bit binary value. The frequency resolution of the AD9858 is 0.233 Hz when the SYSCLK is 1 GHz.

Frequency-Sweeping Mode

The AD9858 provides automated frequency sweeping capability. This allows the AD9858 to generate frequency-swept signals for chirp radar or other applications. The AD9858 includes features that automate much of the task of executing frequency sweeps.

The frequency sweep feature is implemented through the use of a frequency accumulator (not to be confused with the phase accumulator). The frequency accumulator repeatedly adds a frequency incremental quantity to the current value, thereby creating new instantaneous frequency tuning words, causing the frequency generated by the DDS to change with time. The frequency increment, or step size, is loaded into a register known as the delta frequency tuning word (DFTW). The rate at which the frequency is incremented is set by another register, the delta frequency ramp rate word (DFRRW). Together these two registers enable the AD9858 to sweep from a beginning frequency set by the FTW, upwards or downwards, at a desired rate and frequency step size. The result is a very linear frequency sweep, or chirp.





The delta frequency ramp rate word (DFRRW) functions as a countdown timer, in which the value of the DFRRW is decremented at the rate of SYSCLK / 8. This means the most rapid frequency word update occurs when a value of "1" is loaded into the DFRRW, and results in a frequency increment at $1/8^{th}$ of the SYSCLK rate. With a SYSCLK of 1GHz, the frequency can be incremented at a maximum rate of 125 MHz (DFRRW = 1). The delta frequency tuning word (DFTW) must specify whether the frequency sweep should proceed up or down from the starting

frequency (FTW). Therefore the DFTW is expressed as a 2s-complement binary value, in which positive indicates up, and negative down.

A DFRRW value of 0 written to the register stops all frequency sweeping. There is no automatic stop-at-a-given-frequency function. The user must calculate the time interval required to reach the final frequency and then issue a command to write 0 into the DFRRW register. The time required for a frequency sweep is calculated by the following formula:

$$T = \frac{|f_F - f_S| \times 2^{35}}{SysClk^2} \times \frac{DFRRW}{DFTW}$$

where T is the duration of the sweep in seconds

f_S is the starting frequency, determined by $f_S = \frac{FTW}{2^{32}} \times SysClk$

f_F is the final frequency

The delta frequency step size is given by

$\Delta f = \frac{DFTW \times SysClk}{2^{32}}$, remembering that *DFTW* is a signed (2s complement) value.

The time between each frequency step (Δt) is given by:

$$\Delta t = \frac{8 \times DFRRW}{SysClk}$$

The value of the stop frequency f_F is determined by:

$$f_F = f_S + T \times \frac{\Delta f}{\Delta t}$$

Returning to starting frequency

The original frequency tuning word (FTW), which was written into the frequency tuning register, does not change at any time during a sweeping operation. This means the DDS may be returned to the sweep starting frequency at any time during a sweep. Setting the control bit named *AutoClear Frequency Accumulator* forces the frequency accumulator to zero, instantly returning the DDS to the frequency stored as FTW.

Full Sleep Mode

Setting all of the Power Down bits in the Control Function Register activates full Sleep Mode. During the power down condition the clocks associated with the various functional blocks of the device are turned off, thereby offering a significant power savings.

Synchronization

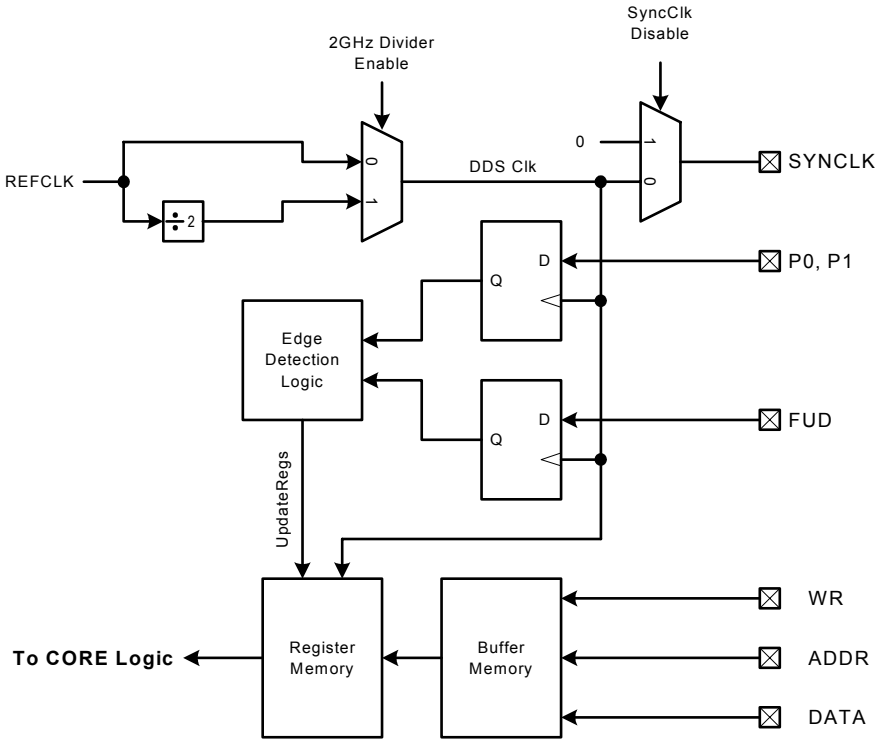
SYNCLK and FUD Pins

Timing for the AD9858 is provided via the user-supplied REFCLK input. The REFCLK input is buffered and is the source for the internally generated SYSCLK. The frequency of SYSCLK can either be the same as REFCLK or half that of REFCLK (via a programmable divide-by-2 function set in the control function register CFR). The REFCLK input is capable of handling input frequencies as high as 2GHZ. However, the device is designed for a maximum SYSCLK frequency of 1GHz. Thus, it is mandatory that the "divide-by-2" SYSCLK function be enabled when the frequency of REFCLK is greater than 1GHz.

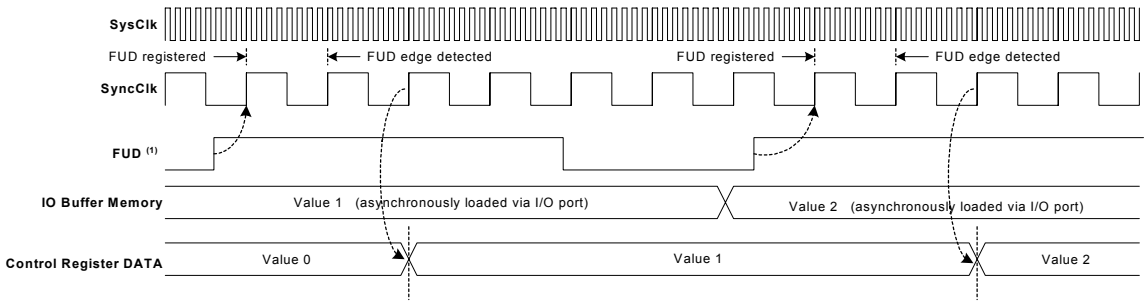
SYSCLK serves as the "sample clock" for the DAC; and is fed to a Divide-by-8 frequency divider to produce DDSCLK. DDSCLK is provided to the user on the SYNCLK pin. This enables synchronization of external hardware with the AD9858's internal DDS clock. External hardware that is synchronized to the SYNCLK signal can then be used to provide the FUD (Frequency UpDate) signal to the AD9858. The FUD signal and SYNCLK are used to transfer the internal buffer register contents into the memory registers of the device. A block diagram of the synchronization methodology is provided below. Also included below is an I/O synchronization timing diagram.

It should be noted that SYNCLK is also used to synchronize the assertion of the Profile Select pins (PS0, PS1). The FUD, PS0, and PS1 pins must be setup and held around the rising edge of SYNCLK. These device inputs are designed for zero-hold-time and <TBD> setup time.

I/O Synchronization Block Diagram



I/O Synchronization Timing Diagram



(1) FUD is an input provided by the user that must be setup and held around rising edges of SyncClk. The occurrence of the rising edge of SyncClk during the high state of the UpdateRegs signal causes the buffer memory contents to be transferred into the Control Registers. Similarly, a state change on the PS0 or PS1 pins is equivalent to asserting a valid FUD sequence. NOTE: I/O updates are synchronous to the SyncClk signal regardless of the synchronization mode selected.

Programming the AD9858

The transfer of data from the user to the DDS core of the device is a two-step process. In a write operation, the user first writes the data to the I/O buffer using either the parallel port (which includes bits for address and data) or serial mode (where the address and data are combined in a serial word). Regardless of the method used to enter data to the I/O Buffer, the DDS core cannot access the data until the data is latched into the memory registers from the I/O buffer. Toggling the FUD pin or changing one of the profile select pins causes an update of all elements of the I/O buffer memory into the DDS core's register memory.

I/O Port Functionality

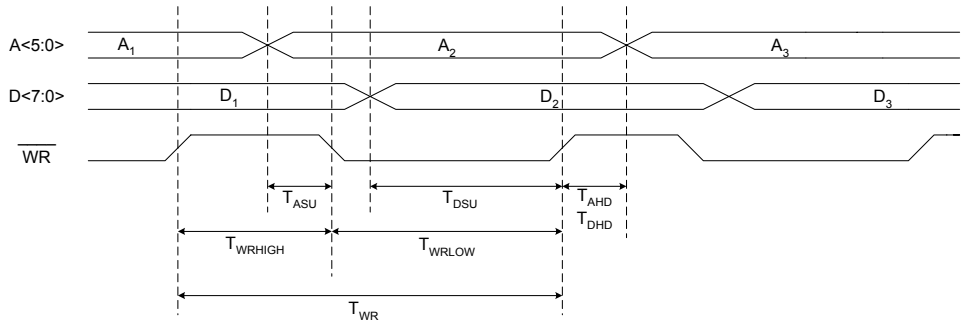
The I/O Port can be operated in either SERIAL or PARALLEL programming mode. Mode selection is accomplished via the S/P Select pin. Logic 0 on this pin configures the I/O Port for SERIAL programming, while logic 1 configures the I/O Port for PARALLEL programming.

The ability to read back the contents of a register is provided in both modes to facilitate the debug process during the user's prototyping phase of a design. In either mode, however, the reading back of profile registers requires that the profile select pins (P0, P1) be configured to select the desired register bank. When reading a register that resides in one of the profiles, the register address acts as an offset to select one of the registers among the group of registers defined by the profile. The profile select pins control the base address of the register bank and selects the appropriate register grouping.

PARALLEL Programming Mode

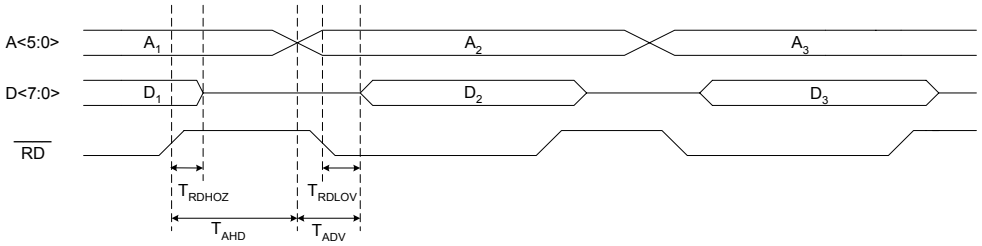
In Parallel Programming Mode the I/O Port makes use of 8 bidirectional *data* pins (D0-D7), 6 *address* input pins (ADDR5-ADDR0), a *read* input pin (RD), and a *write* input pin (WR). A register is selected by providing the proper address combination as defined in the Register Map. Read or write functionality is invoked by pulsing the appropriate pin (RD or WR), the two operations are mutually exclusive. The read or write data is transported on the D7-D0 pins. The correlation between the D7-D0 data bits and their functionality at a specific register address is detailed in the register map and register bit description.

Parallel I/O operation allows write access to each byte of any register in the I/O buffer memory in a single I/O operation at a 100MHz rate. However, unlike write operation, read back capability is NOT guaranteed at the 100MHz rate. It is intended as a low speed function for debug purposes. Timing for both read and write cycles is depicted in the diagrams below.



Specification	Value	Description
T_{ASU}	tbd	Address Setup Time To WR Singal Active
T_{DSU}	tbd	Data Setup Time To WR Signal Inactive
T_{ADH}	tbd	Address Hold Time To WR Signal Inactive
T_{DHD}	tbd	Data Hold Time To WR Signal Inactive
T_{WRLOW}	tbd	WR Signal Minimum Low Time
T_{WRHIGH}	$T_{ASU} + T_{AHD}$	WR Signal Minimum High Time
T_{WR}	$T_{WRLOW} + T_{WRHIGH}$	WR Signal Minimum Period

I/O Port *WRITE* Cycle Timing (Parallel)



Specification	Value	Description
T_{ADV}	tbd	Address To Data Valid Time (maximum)
T_{ADH}	tbd	Address Hold Time To RD Signal Inactive (minimum)
T_{RDLOV}	tbd	RD Low to Output Valid (maximum)
T_{RDHOZ}	tbd	RD High To Data Tristate (maximum)

I/O Port *READ* Cycle Timing (Parallel)

SERIAL Programming Mode

In Serial Programming Mode the I/O Port uses a *chip select* pin (CS), a *serial clock* pin (SCLK), an *I/O reset* pin (IO RESET), and either 1 or 2 *serial data* pins (SDIO and/or SDO). The number of serial data pins used depends on the configuration of the I/O Port; i.e., whether it has been configured for 2-wire or 3-wire serial operation as defined by the Control Function Register. In 2-wire mode the SDIO pin operates as a bidirectional serial data pin. In 3-wire mode the SDIO pin operates only as a serial data *input* pin, and the SDO pin acts as the serial output. The maximum rate of SCLK is <TBD>. However, during READ operation, the <TBD> rate is not guaranteed.

The serial port is a SPI-compatible serial interface and its operation is virtually identical to that of the AD9852/4. Serial port communication occurs in 2 phases. Phase 1 is an instruction cycle consisting of an 8-bit word. The MSB of the instruction byte flags the ensuing operation as a read or write operation. The 6 LSBs define the serial address of the target register as defined in the register map. The instruction byte format is given in the table below.

(MSB) **D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	(LSB) **D0**
1: Read 0: Write	X	A5	A4	A3	A2	A1	A0

Phase 2 of a serial port communication contains the data to be routed to/from the addressed register. The number of bytes transferred during Phase 2 depends on the length of the target register. Serial operation requires that ALL bits associated with a serial register address be transferred.

Both phases of a serial port communication require the serial data clock (SCLK) to be operating. When writing to the device, serial bits are transferred on the rising edge of SCLK. When reading

from the device, serial output bits are transferred on the falling edge of SCLK. The bit order for both phases of a serial port communication is selectable via the Control Function Register.

The CS pin serves as a chip select control line. When CS is at a logic 1 state the SDO and SDIO pins are disabled (forced into a high impedance state). Only when the CS pin is at a logic 0 state are the SDO and SDIO pins active. This allows multiple devices to exist on a single serial bus. If multiple devices are connected to the same serial bus, then communication with a single device is accomplished by setting CS to a logic 0 state on the target device but to a logic 1 state on all other devices. In this way serial communication occurs only between the controller and the target device.

In the case where I/O synchronization is lost between the AD9858 and the external controller, the IO RESET pin provides a means to re-establish synchronization without initializing the entire device. Asserting the active high IO RESET pin resets the serial port state machine. This terminates the current I/O operation and puts the device into a state in which the next 8 SCLK pulses are expected to be the instruction byte of the next I/O transfer. NOTE: Any information previously written to the memory registers during the last valid communication cycle prior to loss of synchronization remains intact.

Register Map

The registers are listed in the following table. The serial address and parallel address numbers associated with each of the registers are shown in hexadecimal format. Angle brackets <> are used to reference specific bits or ranges of bits. For example, <3> designates bit 3 while <7:3> designates the range of bits from 7 down to 3, inclusive.

Register Name	Address Ser	Address Par	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value	Profile
Control Function Register (**CFR**)	00h	00h <7:0>	open	2GHz Divider Disable	Sync CLK Out Disable	Mixer Power Down	Phase Detect PwrDwn	Power Down	SDIO Input Only	LSB First	18h	N/A
		01h <15:8>	Freq. Sweep Enable	Enable SINE Output	Charge Pump Offset Bit	**Phase Detector Divider Ratio (N)** (see table below)		Charge Pump Polarity	**Phase Detector Divider Ratio (M)** (see table below)		00h	N/A
		02h <23:16>	AutoClr Freq. Accum	AutoClr Phase Accum	Load Δ-Freq. Timer	Clear Freq. Accum	Clear Phase Accum	open	Fast Lock Enable	Don't use FTW for fast lock	00h	N/A
		03h <31:24>	**Frequency Detect Charge Pump Current** (see table below)		**Final Closed LoopCharge Pump Current** (see table below)			**Wide Closed Loop Charge Pump Current** (see table below)			00h	N/A
Delta-Freq. Tuning Word (**DFTW**)	01h	04h	Delta Frequency Word <7:0>								-	N/A
		05h	Delta Frequency Word <15:8>								-	N/A
		06h	Delta Frequency Word <23:16>								-	N/A
		07h	Delta Frequency Word <31:24>								-	N/A
Δ-Freq Ramp Rate (**DFRRW**)	02h	08h	Delta Frequency Ramp Rate Word <7:0>								-	N/A
		09h	Delta Frequency Ramp Rate Word <15:8>								-	N/A
Frequency Tuning Word #0 (**FTW0**)	03h	0Ah	Frequency Tuning Word #0 <7:0>								00h	0
		0Bh	Frequency Tuning Word #0 <15:8>								00h	0
		0Ch	Frequency Tuning Word #0 <23:16>								00h	0
		0Dh	Frequency Tuning Word #0 <31:24>								00h	0
Phase Offset Word 0 (**POW0**)	04h	0Eh	Phase Offset Word #0 <7:0>								00h	0
		0Fh	open	open	Phase Offset Word #0 <13:8>						00h	0
Frequency Tuning Word #1 (**FTW1**)	05h	10h	Frequency Tuning Word #1 <7:0>								-	1
		11h	Frequency Tuning Word #1 <15:8>								-	1
		12h	Frequency Tuning Word #1 <23:16>								-	1
		13h	Frequency Tuning Word #1 <31:24>								-	1
Phase Offset Word 1 (**POW1**)	06h	14h	Phase Offset Word #1 <7:0>								-	1
		15h	open	open	Phase Offset Word #1 <13:8>						-	1
Frequency Tuning Word #2 (**FTW2**)	07h	16h	Frequency Tuning Word #2 <7:0>								-	2
		17h	Frequency Tuning Word #2 <15:8>								-	2
		18h	Frequency Tuning Word #2 <23:16>								-	2
		19h	Frequency Tuning Word #2 <31:24>								-	2
Phase Offset Word 2 (**POW2**)	08h	1Ah	Phase Offset Word #2 <7:0>								-	2
		1Bh	open	open	Phase Offset Word #2 <13:8>						-	2
Frequency Tuning Word #3 (**FTW3**)	09h	1Ch	Frequency Tuning Word #3 <7:0>								-	3
		1Dh	Frequency Tuning Word #3 <15:8>								-	3
		1Eh	Frequency Tuning Word #3 <23:16>								-	3
		1Fh	Frequency Tuning Word #3 <31:24>								-	3
Phase Offset Word 3 (**POW3**)	0Ah	20h	Phase Offset Word #3 <7:0>								-	3
		21h	open	open	Phase Offset Word #3 <13:8>						-	3
Reserved	0Bh	22h	Reserved, do not write, leave at h'FF								FFh	N/A
		23h	Reserved, do not write, leave at h'FF								FFh	N/A

Register Bit Descriptions

Control Function Register (CFR)

The CFR is comprised of four bytes located in parallel addresses 03h-00h. The CFR is used to control the various functions, features, and modes of the AD9858. The functionality of each bit is detailed below. Note that the register bits are identified according their serial register bit locations beginning with the most significant bit.

CFR<31:30>: Frequency detect mode charge pump current.

These bits are used to set the scale factor for the frequency-detect mode charge pump output current per the table below. The charge pump delivers the scaled output current when the control logic forces the charge pump into its frequency detect operating mode. The charge pump's baseline output current ($\mathbf{I_{CP0}}$) is determined by the external CP I_{SET} resistor and is given by:

$$I_{CP0} = 1.24 / CP\_I_{SET}$$

The recommended nominal value of the CP I_{SET} resistor is 2.4KΩ, which yields a baseline current of 500µA.

CFR<31:30>	Frequency Detect Charge Pump Scale Value	Notes
00b	0	$I_{out} = 0$ *(default)*
01b	2	$I_{out} = 20 \times I_{CP0}$
10b	3	$I_{out} = 40 \times I_{CP0}$
11b	4	$I_{out} = 60 \times I_{CP0}$

CFR<29:27>: Final closed-loop mode charge pump output current.

These bits are used to set the scale factor for the final closed-loop mode charge pump output current per the table below. The charge pump delivers the scaled output current when the control logic forces the charge pump into its final closed-loop mode.

CFR<29:27>	Final Closed Loop CP Scale Value	Notes
0xxb	0	$I_{out} = 0$ *(default)*
100b	1	$I_{out} = I_{CP0}$
101b	2	$I_{out} = 2 \times I_{CP0}$
110b	3	$I_{out} = 3 \times I_{CP0}$
111b	4	$I_{out} = 4 \times I_{CP0}$

CFR<26:24>: Wide Closed Loop charge pump output current

These bits are used to set the scale factor for the wide closed loop charge pump output current per the table below. The charge pump delivers the scaled output current when the control logic forces the charge pump into its wide closed loop operating mode.

CFR<26:24>	Wide Closed-Loop CP Scale Value	Notes
000b	0	I_{out} = 0 *(default)*
001b	2	$I_{out} = 2 \times I_{CP0}$
010b	4	$I_{out} = 4 \times I_{CP0}$
011b	6	$I_{out} = 6 \times I_{CP0}$
100b	8	$I_{out} = 8 \times I_{CP0}$
101b	10	$I_{out} = 10 \times I_{CP0}$
110b	12	$I_{out} = 12 \times I_{CP0}$
111b	14	$I_{out} = 14 \times I_{CP0}$

CFR<23>: AutoClear Frequency Accumulator bit.

When CFR<23> = 0 (*default*), a new delta frequency word is applied to the input of the accumulator and added to the currently stored value.

When CFR<23> = 1, this bit automatically synchronously clears (loads zeros into) the frequency accumulator for one cycle upon reception of the FUD sequence indicator.

CFR<22>: AutoClear Phase Accumulator bit.

When CFR<22> = 0 *(default)*, a new frequency tuning word is applied to the input of the phase accumulator and added to the currently stored value.

When CFR<22> = 1, this bit automatically synchronously clears (loads zeros into) the phase accumulator for one cycle upon reception of the FUD sequence indicator.

CFR<21>: Load Delta-Frequency Timer.

When CFR<21> = 1 *(default)*, the contents of the Delta Frequency Ramp Rate word are loaded into the Ramp Rate Timer (down counter) upon detection of a FUD sequence.

When CFR<21> = 0, the contents of the Delta Frequency Ramp Rate word are loaded into the Ramp Rate Timer upon time-out with no regard to the state of the FUD sequence indicator (i.e., the FUD sequence indicator is ignored).

CFR<20>: Clear Frequency Accumulator bit.

When CFR<20> = 1, the Frequency Accumulator is synchronously cleared and is held clear until CFR<20> is returned to a logic 0 state (*default*).

CFR<19>: Clear Phase Accumulator bit.

When CFR<19> = 1, the Phase Accumulator is synchronously cleared and is held clear until CFR<19> is returned to a logic 0 state (*default*).

CFR<17>: PLL fast-lock Enable bit.

When CFR<17> = 0 (*default*), the PLL's fast-lock algorithm is disabled.
When CFR<17> = 1, the PLL's fast-lock algorithm is active.

CFR<16>: This bit allows the user to control whether or not the PLL's fast-lock algorithm will use the tuning word value to determine whether or not to enter the fast-lock mode.

When CFR<16> = 0 (*default*), the PLL's fast-lock algorithm considers the relationship between the programmed frequency tuning word and the instantaneous frequency as part of the locking process.

When CFR<16> = 1, the PLL's fast-lock algorithm does not use the frequency tuning word as part of the locking process.

CFR<15>: Frequency Sweep Enable bit.

When CFR<15> = 0 (*default*), the device is in the Single Tone mode.
When CFR<15> = 1, the device is in the Frequency Sweep Mode.

CFR<14>: Sine/Cosine select bit.

When CFR<14> = 0 *(default)*, the angle-to-amplitude conversion logic employs a COSINE function.
When CFR<14> = 1, the angle-to-amplitude conversion logic employs a SINE function.

CFR<13>: Charge pump current offset bit.
When CFR<13> = 0 *(default)*, the charge pump operates with normal current settings.
When CFR<13> = 1, the charge pump operates with offset current settings (please see charge pump description)

CFR<12:11>: Phase detector reference input frequency divider ratio.
These bits set the phase detector divide value per the table below.

CFR<12:11>	Phase Detector Divider Ratio (N)	Notes
00b	1	Default value
01b	2	
1xb	4	LSB ignored

CFR<10>: Charge Pump Polarity select bit.

When CFR<10> = 0 (*default*), the Charge Pump is set up for operation with a ground-referenced VCO. In this mode, the Charge Pump sources current when the frequency at PD_{in} is LESS than the frequency at DIV_{in}. It sinks current when the opposite is true.

When CFR<10> = 1, the Charge Pump is set up for a supply-referenced VCO. In this mode, the Charge Pump's source/sink operation is opposite that for a ground-referenced VCO.

CFR<9:8>: Phase detector feedback input frequency divider ratio.

These bits set the phase detector divide value per the table below.

CFR<9:8>	Phase Detector Divider Ratio (M)	Notes
00b	1	Default value
01b	2	
1xb	4	LSB ignored

CFR<7>: Not used

CFR<6>: Disable bit for the 2GHz RefClk divider.

When CFR<6> = 0, the RefClk divide-by-2 function is bypassed.
When CFR<6> = 1, *(default)* the RefClk divide-by-two function (which operates up to 2GHz) is enabled.

CFR<5>: SYNCLK Disable bit.

When CFR<5> = 0 *(default)*, the SYNCLK pin is active.

When CFR<5> = 1, the SYNCLK pin assumes a static logic 0 state (disabled). In this state the pin drive logic is shut down to keep noise generated by the digital circuitry at a minimum. However, the synchronization circuitry remains active (internally) to maintain normal device timing.

CFR<4:2>: Power Down bits.

Active high (logic 1) powers down the respective function. Writing all 3 bits to a logic 1 causes the device to enter Full Sleep mode.

CFR<4> is used to shut down the Analog Mixer stage. (Default =1)
CFR<3> is used to shut down the Phase Detector and Charge Pump circuitry. (Default = 1)
CFR<2> is used to shut down the DDS core, DAC, and stops all internal clocks except SYNCLK (see the figure detailing the I/O Synchronization Block Diagram). (Default = 0).

CFR<1>: SDIO Input Only.

When CFR<1> = 0 (*default*), the SDIO pin has bi-directional operation (2-wire serial programming mode).

When CFR<1> = 1, the serial data I/O pin (SDIO) is configured as an input only pin (3-wire serial programming mode).

CFR<0>: LSB First.

NOTE: *This bit only has an affect on device operation if the I/O port is configured as a serial port.*

When CFR<0> = 0 (*default*), MSB First format is active.
When CFR<0> = 1, LSB First format is active.

Other Registers

Delta Frequency Tuning Word (DFTW)

The DFTW register is comprised of four bytes located in parallel addresses 04h-07h. The contents of the DFTW are applied to the input of the Frequency Accumulator. Unlike the Frequency Tuning word associated with the Phase Register (which is a 32-bit unsigned integer), the DTFW is a 32-bit *signed* integer. Since it controls the rate of change of frequency, which can either be a positive or negative value, the DTFW is by definition a signed number. When the device is in the Frequency Sweep mode, the output of the Frequency Accumulator is added to the Frequency Tuning word and fed to the Phase Accumulator. This provides the frequency sweep capability of the AD9858. The DFTW controls the frequency resolution associated with a frequency sweep.

As shown in the Register Map, the most significant byte of the Delta Frequency Tuning word is located in parallel register address 07h. The lesser significant bytes appear in descending order at parallel register addresses 06h, 05h, and 04h.

Delta Frequency Ramp Rate Word (DFRRW)

The DFRRW is comprised of four bytes located in parallel addresses 08h-09h. The DFRRW is a 16-bit unsigned number that serves as a divider for the timer used to clock the Frequency Accumulator. The timer runs at the DDS Clk rate and generates a clock "tick" to the Frequency Accumulator. The number stored in the DFRRW register determines the number of DDS Clk cycles between subsequent "ticks" to the Frequency Accumulator. Effectively, the DFRRW controls the rate at which the DFTW is accumulated.

As shown in the Register Map, the most significant byte of the DFRRW is located in parallel register address 09h and the least significant byte at address 08h.

User Profile Registers

The user profile registers are comprised of the 4 frequency tuning words and 4 phase adjustment words. Each pair of frequency and phase registers forms a configurable user profile, selected by the user profile pins. Please see the User Profiles section for a more thorough description.

User Profiles

The AD9858 features 4 user profiles (0-3), selected by profile select pins (PS0, PS1) on the device. Each profile has its own frequency tuning word. This allows the user to load a different frequency tuning word into each profile, which can then be selected as desired by the profile select pins. This makes it possible to hop among the different frequencies at rates up to $1/8^{th}$ of the SYSCLK while in the single-tone mode. The AD9858 also provides a 14-bit phase-offset word for each profile. The value in this register is a 14-bit unsigned number (POW) which represents the proportional ($PO/2^{14}$) phase offset to be added to the instantaneous phase value. This allows the phase of the output signal to be adjusted in fine increments of phase (about 0.022 degrees). It is possible to update the FTW and POW of any profile while the AD9858 is operating at the frequency specified by another profile, and then to switch to the profile containing the newly loaded frequency. Changing the current profile will update both parameters so care must be taken to ensure no unwanted parameter changes take place.

It is also possible to repeatedly write a new frequency into the FTW register of a selected profile, and jump to the new frequency by strobing the frequency update pin (FUD). This allows hopping to arbitrary frequencies, but is limited in the rate at which this can be accomplished by the speed of the I/O port (100 MHz in parallel mode) and the necessity to transfer several bytes of data for each new frequency tuning word. This can be accomplished rapidly enough for many applications.

Frequency Tuning Control

The output frequency of the DDS is determined by the 32 bit frequency tuning word (FTW) and the system clock, (SYSCLK). The relationship is described in the following equation: $Fo = \frac{(FTWxSYSCLK)}{2^N}$, where for the AD9858 N = 32. In single tone mode, the FTW is supplied by the active profile. In frequency sweeping mode, the FTW is the output of the frequency accumulator.

Phase Offset Control

A 14-bit phase-offset (θ) may be added to the output of the Phase Accumulator by means of the phase offset words stored in the memory registers. This feature provides the user with three different methods of phase control.

The first method is a static phase adjustment, where a fixed phase-offset is loaded into the appropriate phase-offset register and left unchanged. The result is that the output signal is offset by a constant angle relative to the nominal signal. This allows the user to phase align the DDS output with some external signal, if necessary.

The second method of phase control is where the user regularly updates the appropriate phase-offset register via the I/O Port. By properly modifying the phase-offset as a function of time, the user can implement a phase modulated output signal. The rate at which phase modulation can be performed is limited by both the speed of the I/O Port and the frequency of SYSCLK limit.

The third method of phase control involves the Profile Registers in which the user loads up to four different phase-offset values into the appropriate profiles. The user can then select between the four preloaded phase-offset values via the AD9858 Profile Select pins. Thus, the phase changes are accomplished by driving hardware pins rather than writing to the I/O port, thereby avoiding the speed limitation imposed by the I/O port. However, this method is restricted to only four different phase-offset values (one phase-offset value per profile). Each profile has an associated frequency and phase value. Changing the current profile will update both parameters so care must be taken to ensure no unwanted parameter changes take place.

Note that the phase-offset value is routed through a unit delay (z^{-1}) block. This is done to ensure that updates of the phase-offset values exhibit the same amount of latency as updates of the frequency tuning word. Otherwise, if the user decided to update both frequency and phase offset values, the phase-offset change would propagate through the device before the tuning word change. The presence of the unit delay in the phase-offset path ensures that both frequency and phase offset changes exhibit similar latency.

Profile Selection

A *profile* consists of a specific group of memory registers (see the Register Map). In the AD9858 each profile contains a 32-bit Frequency Tuning word and a 14-bit Phase Offset word. Each

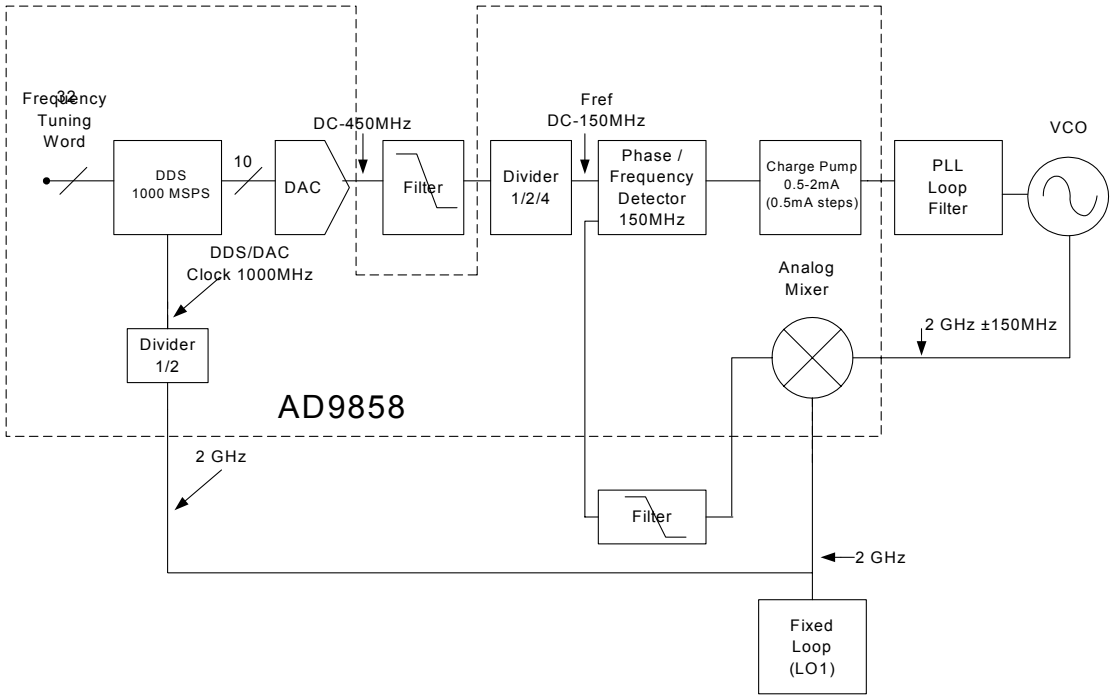
profile is selectable via two external profile select pins (PS0 and PS1) as defined in the table below. The specific mapping of Registers to Profiles is detailed in the Register Map Bit Descriptions section. The user should be aware that selection of a profile is internally synchronized with DDS Clk using the SYNCLK timing. That is, SYNCLK is used to synchronize the assertion of the Profile Select pins (PS0, PS1). Therefore, the PS0 and PS1 pins must be setup and held around the rising edge of SYNCLK. The PS0 and PS1 inputs are designed for zero-hold-time and <TBD> setup time.

PS1	PS0	Profile
0	0	0
0	1	1
1	0	2
1	1	3

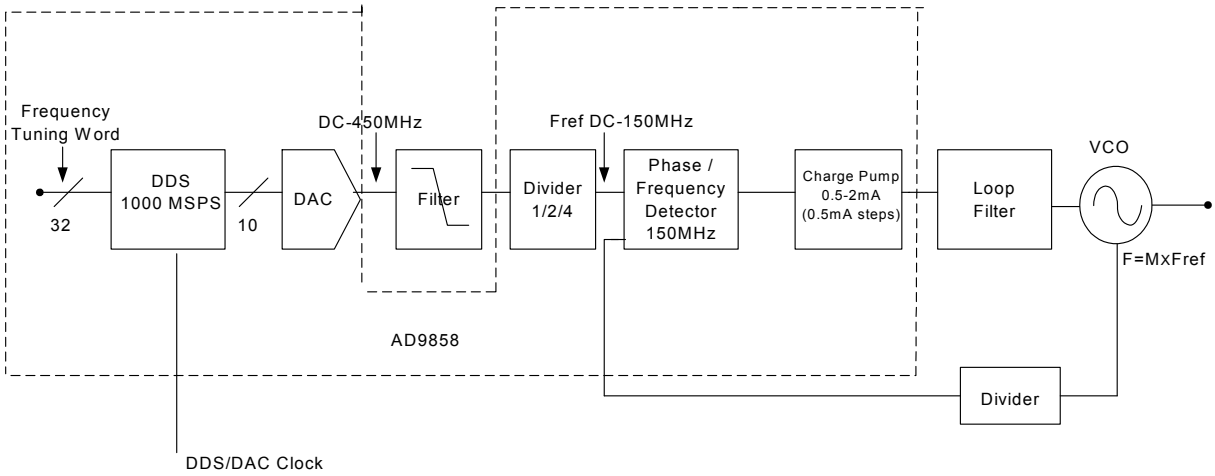
The profiles are available to the user to provide rapid changing of device parameters via external hardware, which alleviates the speed limitations imposed by the I/O port. For example, the user might preprogram the four Phase Offset registers with values that correspond to phase increments of 90°. By controlling the PS0 and PS1 pins, the user can implement $\pi/2$ phase modulation. The data modulation rate would be much higher than that possible by repeatedly reloading a single Phase-Offset register via the I/O port.

AD9858 Application Suggestions

AD9858 DDS Synthesizer
Translation Loop Oscillator
(Translation Loop Evaluation Board)

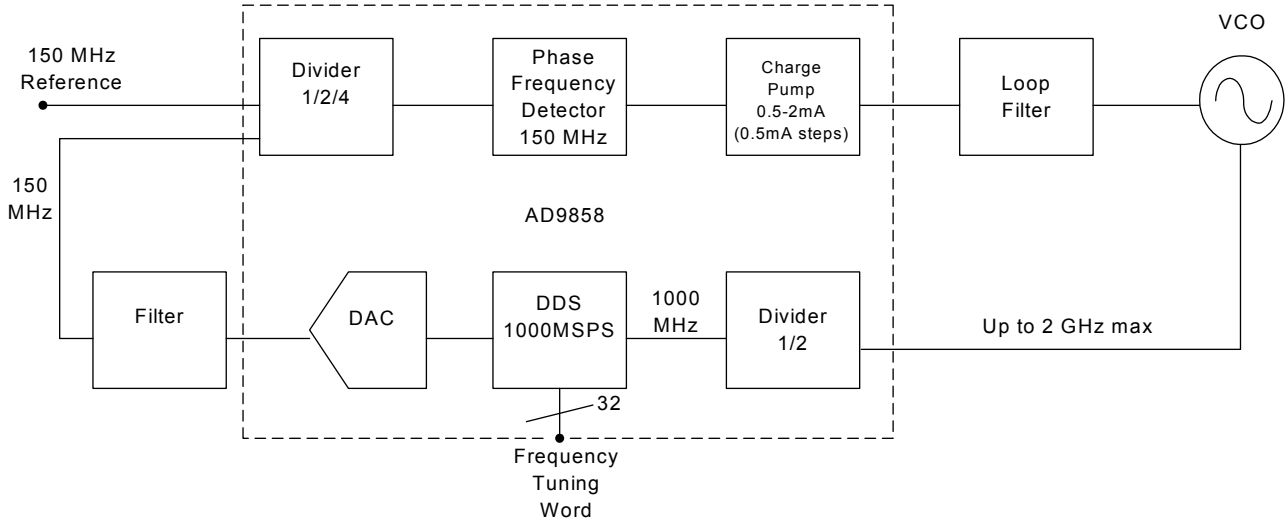


AD9858 DDS Synthesizer
Single Loop PLL Upconversion

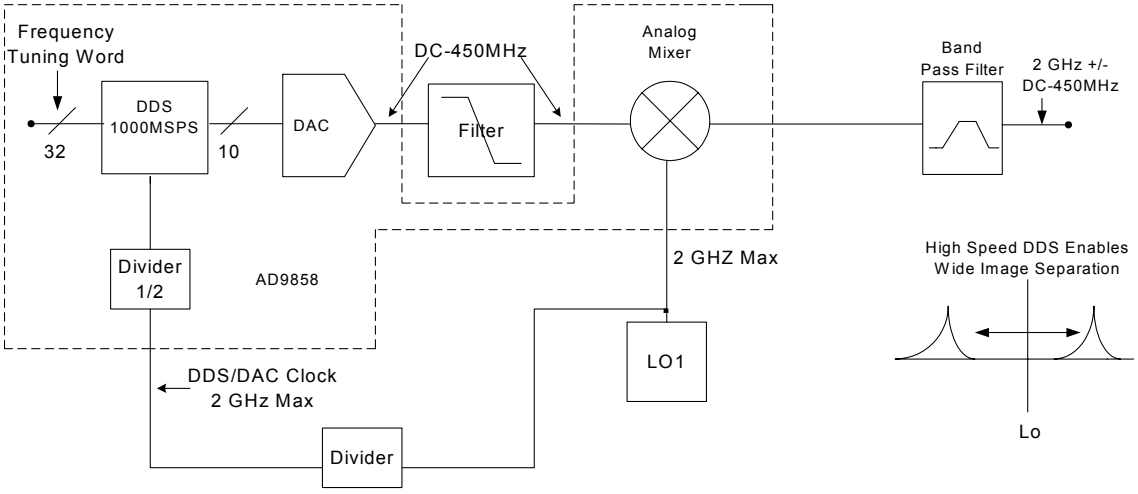


AD9858 Application Suggestions (continued)

AD9858 DDS Synthesizer
AD9858 as Fractional N Synthesizer
(Fractional Divide Evaluation Board)



AD9858 Synthesizer
Direct Upconversion



Evaluation Boards:

The AD9858 will have three different evaluation board designs. The first design is the traditional DDS evaluation board. In this design, the DDS is clocked and the output is taken directly from the DAC. The analog mixer and PLL blocks are not used.

The second design is a fractional-divide loop. This evaluation board was designed to incorporate the DDS, the phase-detector and the charge pump. In this application, the DDS is used in a PLL loop. Unlike a fixed divider used in traditional PLL loops, the output signal is divided and fed back to the phase detector by the DDS. To do this, the output signal of the PLL loop is fed to the DDS as REFCLK. The DDS is programmed to match the reference input frequency. Since the DDS output frequency can take on 2^32 potential values between 0Hz and one half of the PLL loop output frequency, this enables frequency resolution on the order of 470mHz, assuming a PLL loop output frequency of 2GHz.

The third design is a translation loop, or offset loop. In this design, the RF mixer is incorporated into the feedback path of the loop. This allows direct up-conversion to the transmission frequency.

All three evaluation boards have separate schematics, BOMS and instructions. Please see the website for more information: www.analog.com/dds <NOTE: The evaluation board information is not yet on the website. This address is included for future reference>.

Part Number	Description
AD9858/PCB	AD9858 Frequency Synthesizer Board
AD9858/FDPCB	AD9858 Fractional-Divide Loop Frequency Synthesizer Board
AD9858/TLPCB	AD9858 Translation Loop Frequency Synthesizer Board