# High Speed, Half-Duplex *i*Coupler Isolated RS-485 Transceiver

# ADM2486

## FEATURES

- Half-duplex, isolated RS-485 transceiver
- PROFIBUS® compliant
- ANSI EIA/TIA 485-A and ISO 8482: 1987(E) compliant
- 20 Mbps data rate
- 5 V or 3 V operation ($V_{DD1}$)
- High common-mode transient immunity: >25 kV/µs
- Isolated DE status output
- Receiver open-circuit, fail-safe design
- Thermal shutdown protection
- 50 nodes on bus
- Safety and regulatory approvals
  - UL recognition—2500 $V_{RMS}$ for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE Certificate of Conformity
    - DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01
    - DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000
- $V_{IORM}$ = 560 V peak
- Operating temperature range: −40°C to +85°C
- Wide body, 16-lead SOIC package

## APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- PROFIBUS networks
- Industrial field networks
- Multipoint data transmission systems

## GENERAL DESCRIPTION

The ADM2486 differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and complies with ANSI EIA/TIA-485-A and ISO 8482: 1987(E).

The device employs Analog Devices *i*Coupler® technology to combine a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package. The logic side of the device is powered with either a 5 V or a 3 V supply, and the bus side uses an isolated 5 V supply.

## FUNCTIONAL BLOCK DIAGRAM

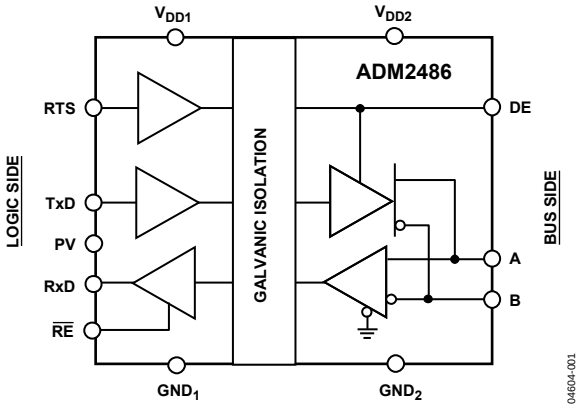



*Figure 1.*

The ADM2486 driver has an active-high enable feature. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output port that imposes minimal loading on the bus when the driver is disabled or when VDD1 or VDD2 = 0 V. Also provided is an active-high receiver disable feature that causes the receive output to enter a high impedance state.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention may cause excessive power dissipation. The part is fully specified over the industrial temperature range and is available in a 16-lead, wide body SOIC package.

**Rev. D**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

# TABLE OF CONTENTS



## REVISION HISTORY

**2/06—Rev. C to Rev. D**

Updated Format ... Universal
Changes to Table 1 ... 3
Changes to Table 8 ... 9
Changes to Figure 22 and Figure 23 ... 13
Changes to Table 9 and Table 10 ... 14
Added PC Board Layout Section ... 16
Changes to Isolated Power Supply Circuit Section and Figure 32 ... 17

**3/05—Rev. B to Rev. C**

Change to Package Characteristics ... 7
Changes to Figure 12, Figure 14, and Figure 15 ... 11
Change to Power_Valid Input Section ... 16

**1/05—Rev. A to Rev. B**

Added PROFIBUS logo ... 1

**11/04—Rev. 0 to Rev. A**

Changes to Figure 1 ... 1
Changes to Figure 6 ... 10
Added Figure 22 through Figure 25 ... 13
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

# SPECIFICATIONS

2.7 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.75 V ≤ $V_{DD2}$ ≤ 5.25 V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DRIVER | | | | | |
| Differential Outputs | | | | | |
| Differential Output Voltage, $V_{OD}$ | | | 5 | V | R = ∞, see Figure 3 |
| | 2.1 | | 5 | V | R = 50 Ω (RS-422), see Figure 3 |
| | 2.1 | | 5 | V | R = 27 Ω (RS-485), see Figure 3 |
| | 2.1 | | 5 | V | $V_{TST}$ = −7 V to +12 V, $V_{DD1}$ ≥ 4.7, see Figure 4 |
| Δ $\|V_{OD}\|$ for Complementary Output States | | | 0.2 | V | R = 27 Ω or 50 Ω, see Figure 3 |
| Common-Mode Output Voltage, $V_{OC}$ | | | 3 | V | R = 27 Ω or 50 Ω, see Figure 3 |
| Δ $\|V_{OC}\|$ for Complementary Output States | | | 0.2 | V | R = 27 Ω or 50 Ω, see Figure 3 |
| Output Short-Circuit Current, $V_{OUT}$ = High | 60 | | 200 | mA | −7 V ≤ $V_{OUT}$ ≤ +12 V |
| Output Short-Circuit Current, $V_{OUT}$ = Low | 60 | | 200 | mA | −7 V ≤ $V_{OUT}$ ≤ +12 V |
| Driver Enable Output, DE Pin | | | | | |
| Output High Voltage | $V_{DD2}$ − 0.1 | | | V | $I_{ODE}$ = 20 μA |
| | $V_{DD2}$ − 0.3 | $V_{DD2}$ − 0.1 | | V | $I_{ODE}$ = 1.6 mA |
| | $V_{DD2}$ − 0.4 | $V_{DD2}$ − 0.2 | | V | $I_{ODE}$ = 4 mA |
| Output Low Voltage | | | 0.1 | V | $I_{ODE}$ = −20 μA |
| | | 0.1 | 0.3 | V | $I_{ODE}$ = −1.6 mA |
| | | 0.2 | 0.4 | V | $I_{ODE}$ = −4 mA |
| Logic Inputs | | | | | |
| Input High Voltage | 0.7 $V_{DD1}$ | | | V | TxD, RTS, $\overline{RE}$, PV |
| Input Low Voltage | | | 0.25 $V_{DD1}$ | V | TxD, RTS, $\overline{RE}$, PV |
| CMOS Logic Input Current (TxD, RTS, $\overline{RE}$, PV) | −10 | +0.01 | +10 | μA | TxD, RTS, $\overline{RE}$, PV = $V_{DD1}$ or 0 V |
| RECEIVER | | | | | |
| Differential Inputs | | | | | |
| Differential Input Threshold Voltage, $V_{TH}$ | −200 | | +200 | mV | −7 V ≤ $V_{CM}$ ≤ +12 V |
| Input Hysteresis | | 70 | | mV | −7 V ≤ $V_{CM}$ ≤ +12 V |
| Input Resistance (A, B) | 20 | 30 | | kΩ | −7 V ≤ $V_{CM}$ ≤ +12 V |
| Input Current (A, B) | | | 0.6 | mA | $V_{IN}$ = + 12 V |
| | | | −0.35 | mA | $V_{IN}$ = −7 V |
| RxD Logic Output | | | | | |
| Output High Voltage | $V_{DD1}$ − 0.1 | | | V | $I_{OUT}$ = 20 μA, $V_A$ − $V_B$ = 0.2 V |
| | $V_{DD1}$ − 0.4 | $V_{DD1}$ − 0.2 | | V | $I_{OUT}$ = 4 mA, $V_A$ − $V_B$ = 0.2 V |
| Output Low Voltage | | | 0.1 | V | $I_{OUT}$ = −20 μA, $V_A$ − $V_B$ = −0.2 V |
| | | 0.2 | 0.4 | V | $I_{OUT}$ = −4 mA, $V_A$ − $V_B$ = −0.2 V |
| Output Short-Circuit Current | 7 | | 85 | mA | $V_{OUT}$ = GND or $V_{CC}$ |
| Three-State Output Leakage Current | | | ±1 | μA | 0.4 V ≤ $V_{OUT}$ ≤ 2.4 V |
| POWER SUPPLY CURRENT | | | | | |
| Logic Side | | | 1.3 | mA | RTS = 0 V, $V_{DD1}$ = 5.5 V |
| | | 1.0 | | mA | 2 Mbps, $V_{DD1}$ = 5.5 V, see Figure 5 |
| | | 4.0 | | mA | 20 Mbps, $V_{DD1}$ = 5.5 V, see Figure 5 |
| | | | 0.8 | mA | RTS = 0 V, $V_{DD1}$ = 3 V |
| | | | 1.1 | mA | 2 Mbps, $V_{DD1}$ = 3 V, see Figure 5 |
| | | 2.1 | | mA | 20 Mbps, $V_{DD1}$ = 3 V, see Figure 5 |
| Bus Side | | | 3.0 | mA | RTS = 0 V |
| | | 43.0 | | mA | 2 Mbps, RTS = $V_{DD1}$, see Figure 5 |
| | | 58.0 | | mA | 20 Mbps, RTS = $V_{DD1}$, see Figure 5 |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| COMMON-MODE TRANSIENT IMMUNITY[1] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| HIGH FREQUENCY, COMMON-MODE NOISE IMMUNITY | | 100 | | mV | $V_{HF}$ = +5 V, −2 V < $V_{TEST2}$ < +7 V, 1 MHz < $f_{TEST}$ < 50 MHz, see Figure 6 |

[1] Common-mode transient immunity is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. $V_{CM}$ is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

# TIMING SPECIFICATIONS

2.7 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.75 V ≤ $V_{DD2}$ ≤ 5.25 V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DRIVER | | | | | |
| Maximum Data Rate | 20 | | | Mbps | |
| Propagation Delay, $t_{PLH}$, $t_{PHL}$ | 25 | 45 | 55 | ns | $R_{LDIFF}$ = 54 Ω, $C_{L1}$ = $C_{L2}$ = 100 pF, see Figure 7 |
| RTS-to-DE Propagation Delay | 20 | 35 | 55 | ns | See Figure 8 |
| Pulse Width Distortion, $t_{PWD}$ | | | 5 | ns | $R_{LDIFF}$ = 54 Ω, $C_{L1}$ = $C_{L2}$ = 100 pF, see Figure 7 and Figure 12 |
| Switching Skew, $t_{SKEW}$ | | 2 | 5 | ns | $R_{LDIFF}$ = 54 Ω, $C_{L1}$ = $C_{L2}$ = 100 pF, see Figure 7 and Figure 12 |
| Rise/Fall Time, $t_R$, $t_F$ | | 5 | 15 | ns | $R_{LDIFF}$ = 54 Ω, $C_{L1}$ = $C_{L2}$ = 100 pF, see Figure 7 and Figure 12 |
| Enable Time | | 43 | 53 | ns | See Figure 9 and Figure 14 |
| Disable Time | | 43 | 55 | ns | See Figure 9 and Figure 14 |
| Enable Skew, $\lvert t_{AZH} - t_{BZL} \rvert$, $\lvert t_{AZL} - t_{BZH} \rvert$ | | 1 | 3 | ns | See Figure 9 and Figure 14 |
| Disable Skew, $\lvert t_{AHZ} - t_{BLZ} \rvert$, $\lvert t_{ALZ} - t_{BHZ} \rvert$ | | 2 | 5 | ns | See Figure 9 and Figure 14 |
| RECEIVER | | | | | |
| Propagation Delay, $t_{PLH}$, $t_{PHL}$ | 25 | 45 | 55 | ns | $C_L$ = 15 pF, see Figure 10 and Figure 13 |
| Differential Skew, $t_{SKEW}$ | | | 5 | ns | $C_L$ = 15 pF, see Figure 10 and Figure 13 |
| Enable Time | | 3 | 13 | ns | $R_L$ = 1 kΩ, $C_L$ = 15 pF, see Figure 11 and Figure 15 |
| Disable Time | | 3 | 13 | ns | $R_L$ = 1 kΩ, $C_L$ = 15 pF, see Figure 11 and Figure 15 |
| POWER_VALID INPUT | | | | | |
| Enable Time | | 1 | 2 | µs | |
| Disable Time | | 3 | 5 | µs | |

# ADM2486 CHARACTERISTICS

## PACKAGE CHARACTERISTICS

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resistance (Input-to-Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input-to-Output)[1] | $C_{I-O}$ | | 3 | | pF | f = 1 MHz |
| Input Capacitance[2] | $C_I$ | | 4 | | pF | |
| Input IC Junction-to-Case Thermal Resistance | $\theta_{JCI}$ | | 33 | | °C/W | Thermocouple located at center of package underside |
| Output IC Junction-to-Case Thermal Resistance | $\theta_{JCO}$ | | 28 | | °C/W | |

[1] Device considered a 2-terminal device: Pin 1 through Pin 8 shorted together, and Pin 9 through Pin 16 shorted together.
[2] Input capacitance is from any input data pin to ground

## REGULATORY INFORMATION

The ADM2486 has been approved by the following organizations:

**Table 4.**

| Organization | Approval Type | Notes |
|---|---|---|
| UL | Recognized under 1577 component recognition program. File E214100. | In accordance with UL1577, each ADM2486 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA). |
| CSA | Approved under CSA Component Acceptance Notice #5A. File 205078. | |
| VDE | Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01.<br>Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000<br>File 2471900-4880-0001. | In accordance with VDE 0884, each ADM2486 is proof tested by applying an insulation test voltage ≥1050 $V_{PEAK}$ for 1 sec (partial discharge detection limit = 5 pC). |

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 5.**

| Parameter | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1-minute duration. |
| Minimum External Air Gap (Clearance) | L(I01) | 7.45 minimum | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(I02) | 8.1 minimum | mm | Measured from input terminals to output terminals, shortest distance along body. |
| Minimum Internal Gap (Internal Clearance) | | 0.017 minimum | mm | Insulation distance through insulation. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1. |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1). |

## VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on the physical package denotes VDE 0884 approval for 560 V peak working voltage.

**Table 6.**

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| Installation Classification per DIN VDE 0110 for Rated Mains Voltage | | | |
| ≤150 V rms | | I-IV | |
| ≤300 V rms | | I-II | |
| ≤400 V rms | | I-II | |
| Climatic Classification | | 40/85/21 | |
| Pollution Degree (DIN VDE 0110, Table 1) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 560 | $V_{PEAK}$ |
| Input-to-Output Test Voltage, Method b1 | $V_{PR}$ | 1050 | $V_{PEAK}$ |
| $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Tested, $t_m$ = 1 sec, Partial Discharge < 5 pC | | | |
| Input-to-Output Test Voltage, Method a | | | |
| After Environmental Tests, Subgroup 1 | | | |
| $V_{IORM} \times 1.6 = V_{PR}$, $t_m$ = 60 sec, Partial Discharge < 5 pC | | 896 | $V_{PEAK}$ |
| After Input and/or Safety Test, Subgroup 2/3 | | | |
| $V_{IORM} \times 1.2 = V_{PR}$, $t_m$ = 60 sec, Partial Discharge < 5 pC | $V_{PR}$ | 672 | $V_{PEAK}$ |
| Highest Allowable Overvoltage (Transient Overvoltage, $t_{tr}$ = 10 sec) | $V_{TR}$ | 4000 | $V_{PEAK}$ |
| Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure, see Figure 21). | | | |
| Case Temperature | $T_S$ | 150 | °C |
| Input Current | $I_{S, INPUT}$ | 265 | mA |
| Output Current | $I_{S, OUTPUT}$ | 335 | mA |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

**Table 7.**

| Parameter | Rating |
|---|---|
| $V_{DD1}$ | −0.5 V to +7 V |
| $V_{DD2}$ | −0.5 V to +6 V |
| Digital Input Voltage (RTS, $\overline{RE}$, TxD) | −0.5 V to $V_{DD1}$ + 0.5 V |
| Digital Output Voltage | |
| RxD | −0.5 V to $V_{DD1}$ + 0.5 V |
| DE | −0.5 V to $V_{DD2}$ + 0.5 V |
| Driver Output/Receiver Input Voltage | −9 V to +14 V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −55°C to +150°C |
| Average Output Current per Pin | −35 mA to +35 mA |
| $\theta_{JA}$ Thermal Impedance | 73°C/W |
| Lead Temperature | |
| Soldering (10 sec) | 260°C |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

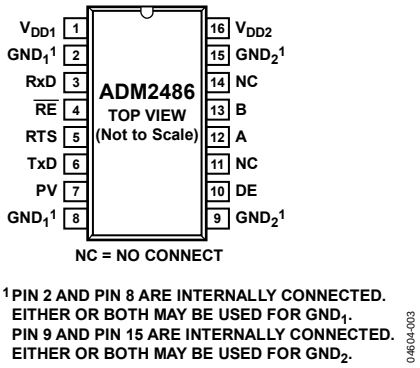



*Figure 2. Pin Configuration*

**Table 8. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Power Supply (Logic Side), 3 V or 5 V Supply. Decoupling capacitor to $GND_1$ required, capacitor value should be between 0.01 µF and 0.1 µF. |
| 2, 8 | $GND_1$ | Ground (Logic Side). |
| 3 | RxD | Receiver Output Data. This output is high when (A – B) > 200 mV and low when (A – B) < –200 mV. The output is three-stated when the receiver is disabled, that is, when $\overline{RE}$ is driven high. |
| 4 | $\overline{RE}$ | Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver, and driving it high disables the receiver. |
| 5 | RTS | Request to Send Input. Driving this input high enables the driver, and driving it low disables the driver. |
| 6 | TxD | Transmit Data Input. Data to be transmitted by the driver is applied to this input. |
| 7 | PV | Power_Valid. Used during power-up and power-down, needs to be tied high when the ADM2486 is operational, see the Applications Information section. |
| 9, 15 | $GND_2$ | Ground (Bus Side). |
| 10 | DE | Driver Enable Status Output. This output signals the driver enable or disable status to other devices on the bus. DE is high when the driver is enabled and low when the driver is disabled. |
| 11, 14 | NC | No Connect. |
| 12 | A | Noninverting Driver Output/Receiver Input. When the driver is disabled, or when $V_{DD1}$ or $V_{DD2}$ is powered down, Pin A is put into a high impedance state to avoid overloading the bus. |
| 13 | B | Inverting Driver Output/Receiver Input. When the driver is disabled, or when $V_{DD1}$ or $V_{DD2}$ is powered down, Pin B is put into a high impedance state to avoid overloading the bus. |
| 16 | $V_{DD2}$ | Power Supply (Bus Side), 5 V Isolated Supply. Decoupling capacitor to $GND_2$ required, capacitor value should be between 0.01 µF and 0.1 µF. |

# TEST CIRCUITS

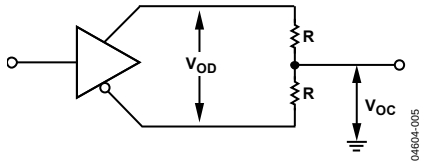



*Figure 3. Driver Voltage Measurement*

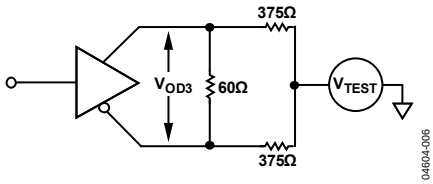



*Figure 4. Driver Voltage Measurement*

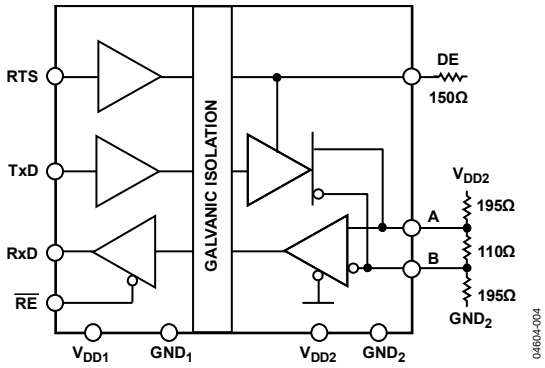



*Figure 5. Supply-Current Measurement Test Circuit*

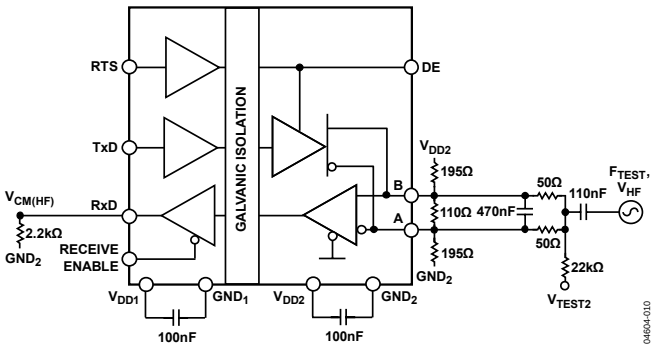



*Figure 6. High Frequency Common-Mode Noise Test Circuit*

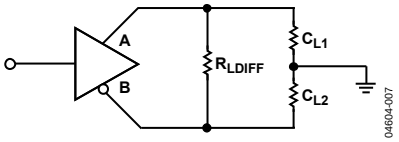



*Figure 7. Driver Propagation Delay*

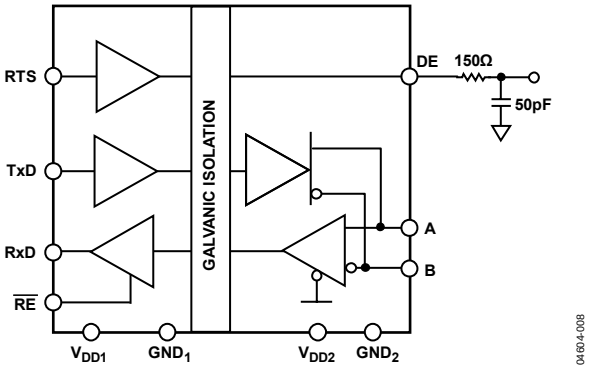



*Figure 8. RTS-to-DE Propagation Delay*

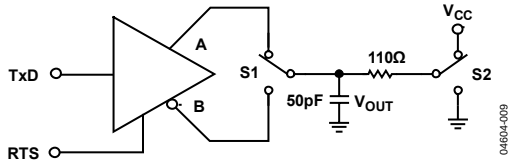



*Figure 9. Driver Enable/Disable*

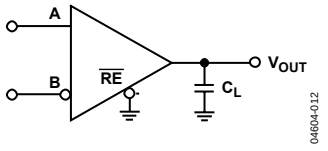



*Figure 10. Receiver Propagation Delay*

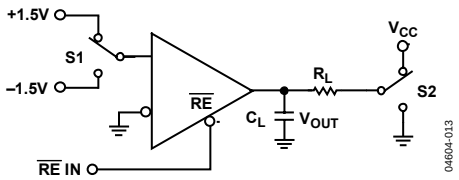



*Figure 11. Receiver Enable/Disable*

# SWITCHING CHARACTERISTICS

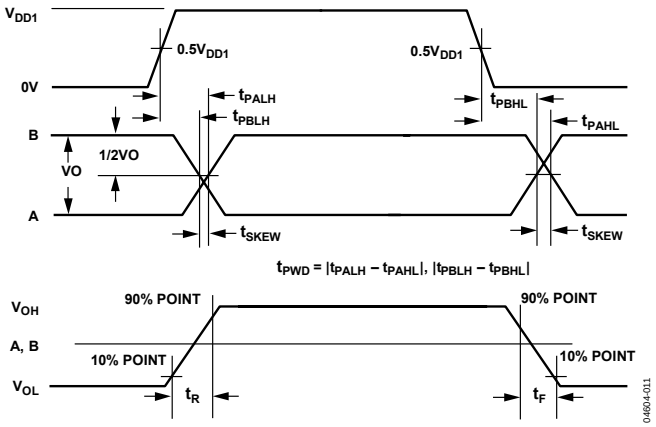



*Figure 12. Driver Propagation Delay, Rise/Fall Timing*

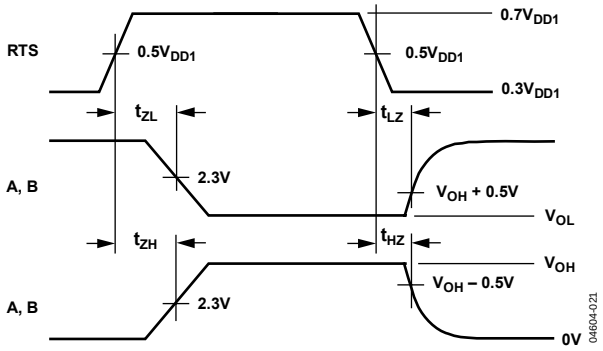



*Figure 14. Driver Enable/Disable Timing*

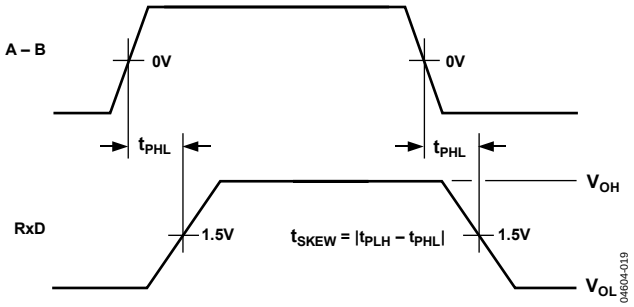



*Figure 13. Receiver Propagation Delay*

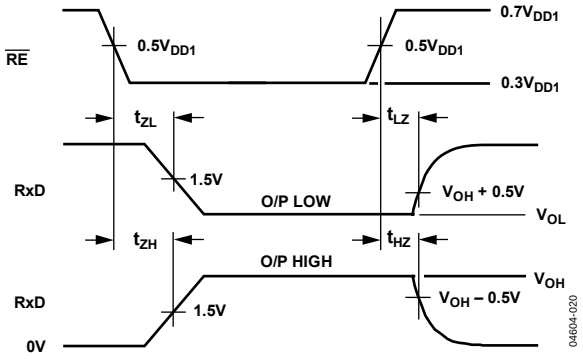



*Figure 15. Receiver Enable/Disable Timing*

# TYPICAL PERFORMANCE CHARACTERISTICS

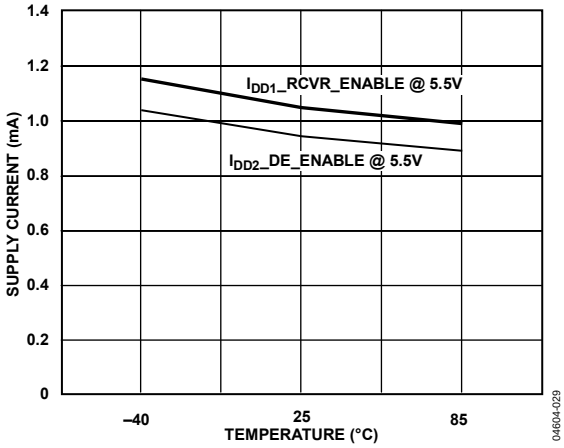



Figure 16. Unloaded Supply Current vs. Temperature

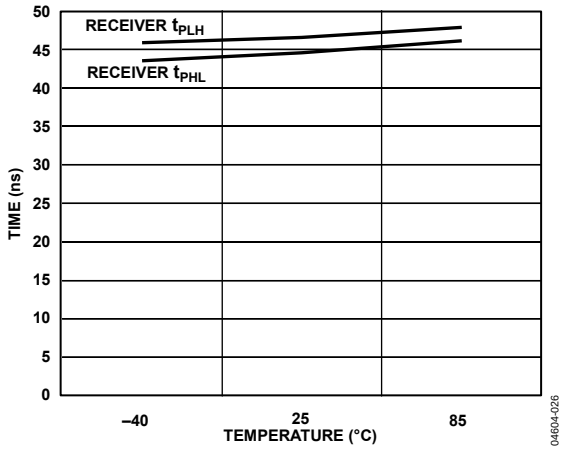



Figure 17. Driver Propagation Delay vs. Temperature

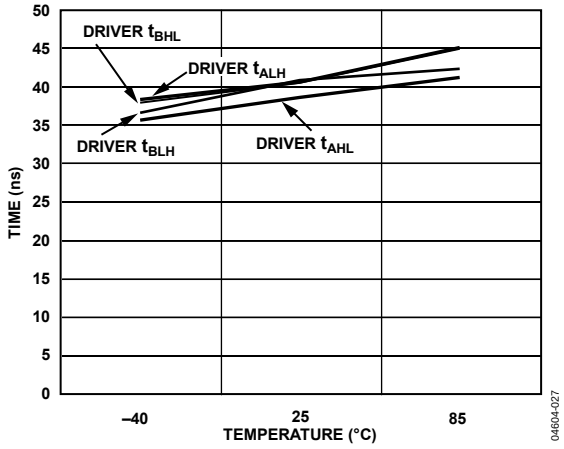



Figure 18. Receiver Propagation Delay vs. Temperature

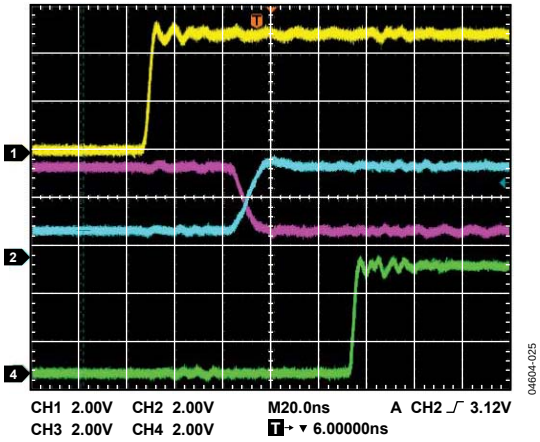



Figure 19. Driver/Receiver Propagation Delay, Low to High ($R_{LDiff}$ = 54 Ω, $C_{L1}$ = $C_{L2}$ = 100 pF)

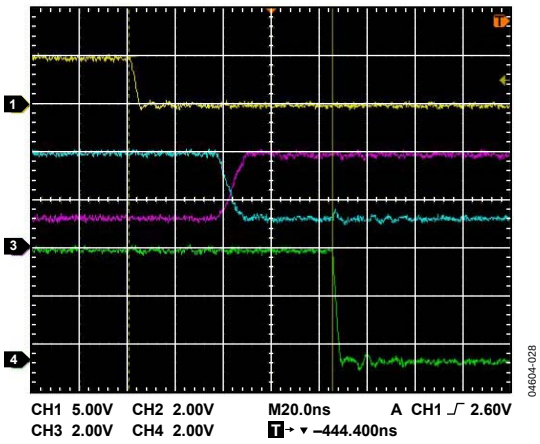



Figure 20. Driver/Receiver Propagation Delay, High to Low ($R_{LDiff}$ = 54 Ω, $C_{L1}$ = $C_{L2}$ = 100 pF)

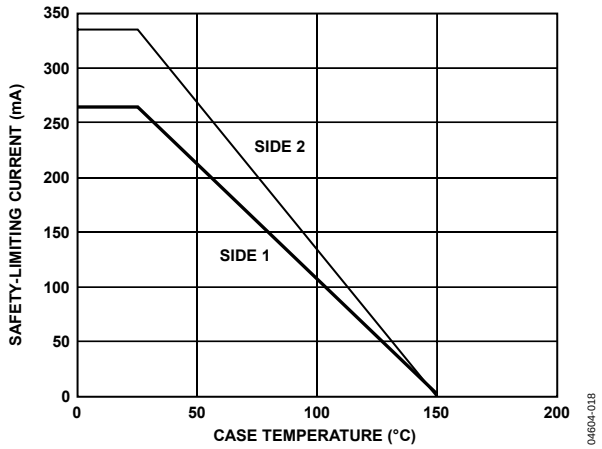



Figure 21. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

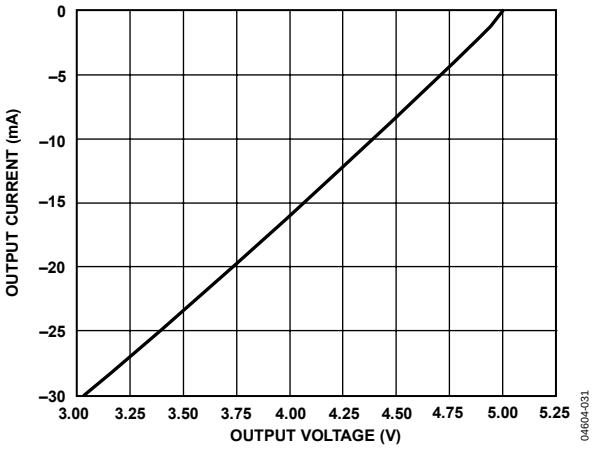



*Figure 22. Output Current vs. Receiver Output High Voltage*

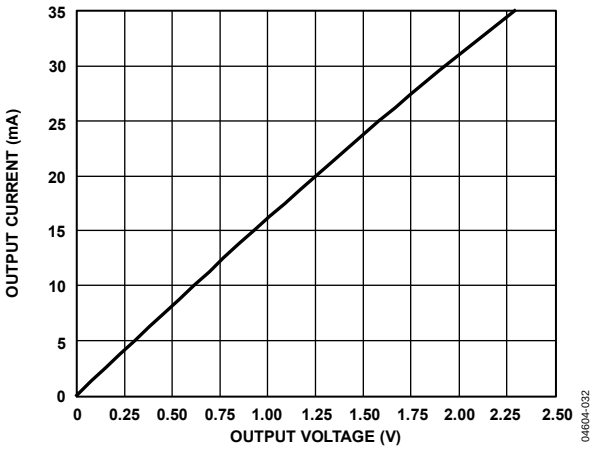



*Figure 23. Output Current vs. Receiver Output Low Voltage*

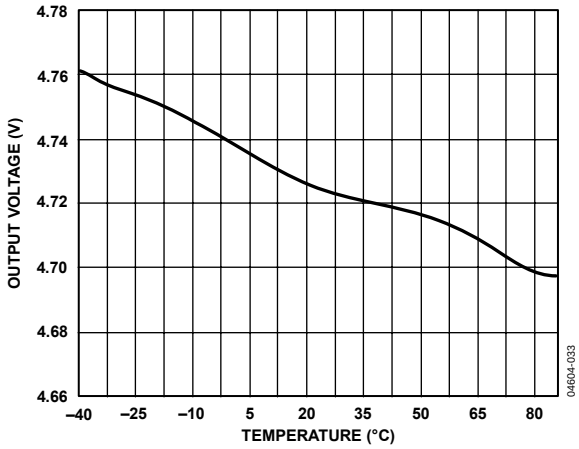



*Figure 24. Receiver Output High Voltage vs. Temperature*
*$I_{RxD}$= –4 mA*

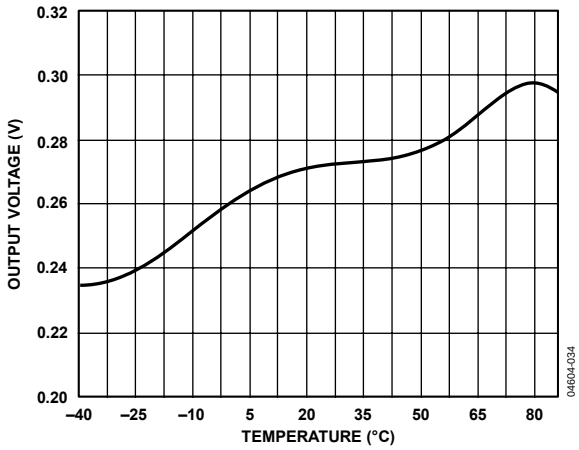



*Figure 25. Receiver Output Low Voltage vs. Temperature*
*$I_{RxD}$ = –4 mA*

# CIRCUIT DESCRIPTION

## ELECTRICAL ISOLATION

In the ADM2486, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 26). Driver input and request-to-send signals, applied to the TxD and RTS pins, respectively, and referenced to logic ground ($GND_1$), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground ($GND_2$). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

### *iCoupler Technology*

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. This technique uses chip-scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

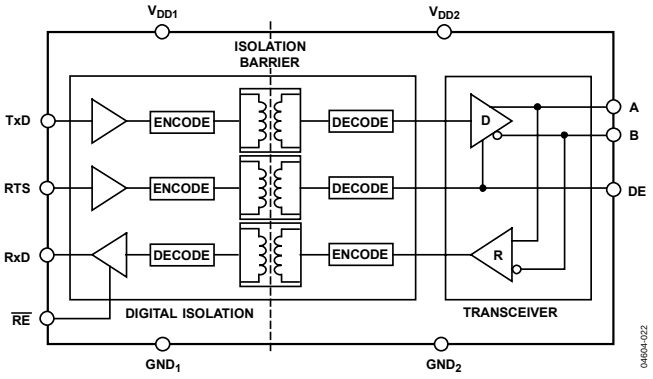



*Figure 26. ADM2486 Digital Isolation and Transceiver Sections*

## TRUTH TABLES

The truth tables in this section use these abbreviations:

| Letter | Description |
|---|---|
| H | High level |
| I | Indeterminate |
| L | Low level |
| X | Irrelevant |
| Z | High impedance (off) |
| NC | Disconnected |

**Table 9. Transmitting**

| Supply Status | | Inputs | | Outputs[1] | | |
|---|---|---|---|---|---|---|
| $V_{DD1}$ | $V_{DD2}$ | RTS | TxD | A | B | DE |
| On | On | H | H | H | L | H |
| On | On | H | L | L | H | H |
| On | On | L | X | Z | Z | L |
| On | Off | X | X | Z | Z | L |
| Off | On | X | X | Z | Z | L |
| Off | Off | X | X | Z | Z | L |

[1] The PV pin is tied high.

**Table 10. Receiving**

| Supply Status | | Inputs | | Output[1] |
|---|---|---|---|---|
| $V_{DD1}$ | $V_{DD2}$ | A – B (V) | $\overline{RE}$ | RxD |
| On | On | >0.2 | L or NC | H |
| On | On | <−0.2 | L or NC | L |
| On | On | −0.2 < A – B < 0.2 | L or NC | I |
| On | On | Inputs open | L or NC | H |
| On | On | X | H | Z |
| On | Off | X | L or NC | H |
| Off | On | X | L or NC | H |
| Off | Off | X | L or NC | L |

[1] The PV pin is tied high.

## POWER-UP/POWER-DOWN THRESHOLDS

The power-up/power-down characteristics of the ADM2486 are in accordance with the supply thresholds shown in Table 11. Upon power-up, the ADM2486 output signals (A, B, RxD, and DE) reach their correct state once both supplies have exceeded their thresholds. Upon power-down, the ADM2486 output signals retain their correct state until at least one of the supplies drops below its power-down threshold. When the $V_{DD1}$ power-down threshold is crossed, the ADM2486 output signals reach their unpowered states within 4 µs.

**Table 11. Power-Up/Power-Down Thresholds**

| Supply | Transition | Threshold (V) |
|---|---|---|
| $V_{DD1}$ | Power-up | 2.0 |
| $V_{DD1}$ | Power-down | 1.0 |
| $V_{DD2}$ | Power-up | 3.3 |
| $V_{DD2}$ | Power-down | 2.4 |

## THERMAL SHUTDOWN

The ADM2486 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

## RECEIVER FAIL-SAFE INPUTS

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating or open-circuited.

## MAGNETIC FIELD IMMUNITY

Because *i*Couplers use coreless technology, no magnetic components are present, and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The following analysis defines the conditions under which this can occur. The ADM2486's 3 V operating condition is examined because it represents the most susceptible mode of operation.

The limitation on the iCoupler's ac magnetic field immunity is set by the condition in which the induced error voltage in the receiving coil (the bottom coil in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2 \; ; \; n = 1, 2, \ldots, N$$

where if the pulses at the transformer output are greater than 1.0 V in amplitude:

$\beta$ = magnetic flux density (gauss).

$N$ = number of turns in receiving coil.

$r_n$ = radius of nth turn in receiving coil (cm).

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 27.

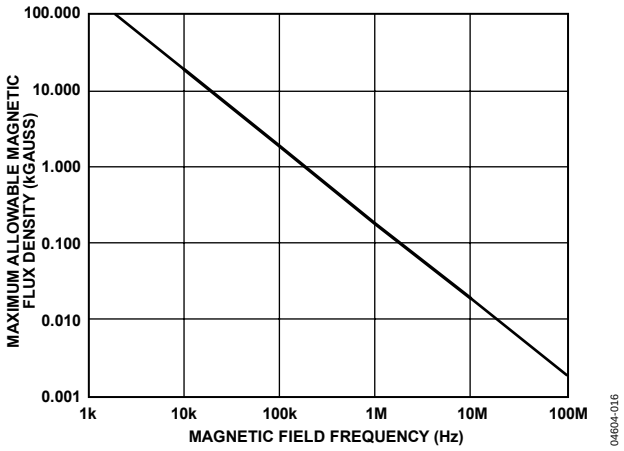



*Figure 27. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V. This is well above the 0.5 V sensing threshold of the decoder.

Figure 28 shows the magnetic flux density values in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2486 transformers.

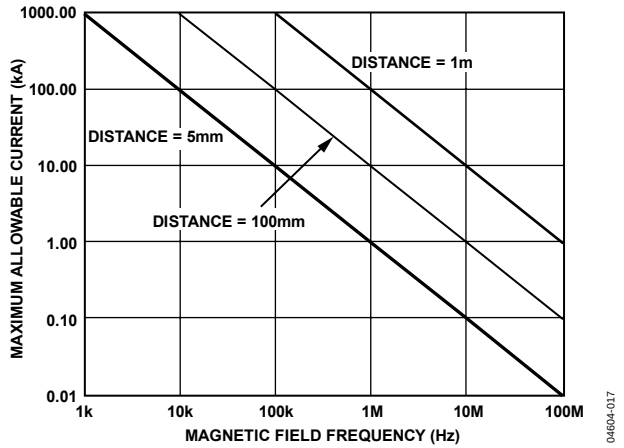



*Figure 28. Maximum Allowable Current for Various Current-to-ADM2486 Spacings*

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

# APPLICATIONS INFORMATION

## PC BOARD LAYOUT

The ADM2486 isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 29). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for $V_{DD1}$ and between Pin 15 and Pin 16 for $V_{DD2}$. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

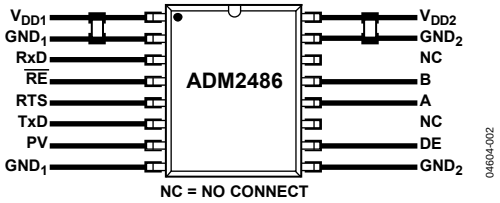



*Figure 29. Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

## POWER_VALID INPUT

To avoid chatter on the A and B outputs caused by slow power-up and power-down transients on $V_{DD1}$ (>100 µs/V), the device features a power_valid (PV) digital input. This pin should be driven low until $V_{DD1}$ exceeds 2.0 V. When $V_{DD1}$ is greater than 2.0 V, this pin should be driven high. Conversely, upon power-down, PV should be driven low before $V_{DD1}$ reaches 2.0 V (see Figure 30).

If the PV pin is driven with an open-drain output, the recommended value for the pull-up resistor is a 10 kΩ resistor, bypassed with a 100 pF capacitor to $GND_1$ (see Figure 31).

The power_valid input can be driven, for example, by the output of a system reset circuit, such as the ADM809Z, which has a threshold voltage of 2.32 V.

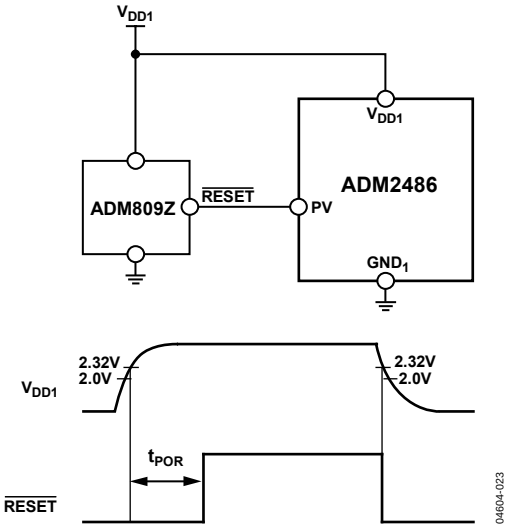



*Figure 30. Driving PV with ADM809Z*

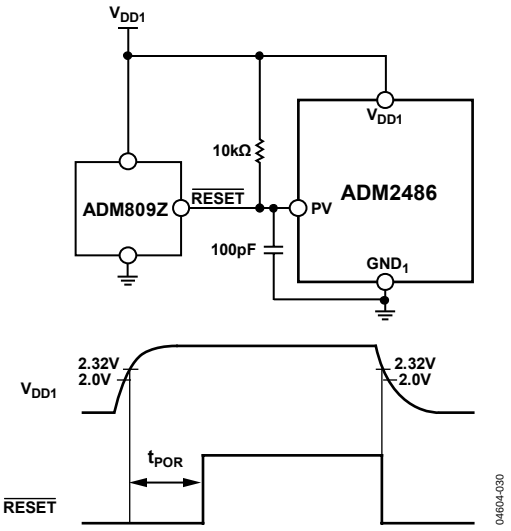



*Figure 31. Driving PV with an Open-Drain Output*

## ISOLATED POWER SUPPLY CIRCUIT

The ADM2486 requires isolated power capable of 5 V at up to approximately 75 mA (this current is dependant on the data rate and termination resistors used) to be supplied between the $V_{DD2}$ and the $GND_2$ pins.

A transformer driver circuit with a center-tapped transformer and LDO can be used to generate the isolated 5 V supply, as shown in Figure 32. The center-tapped transformer provides electrical isolation of the 5 V isolated power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated 5 V power supply to the ADM2486's bus-side circuitry ($V_{DD2}$).

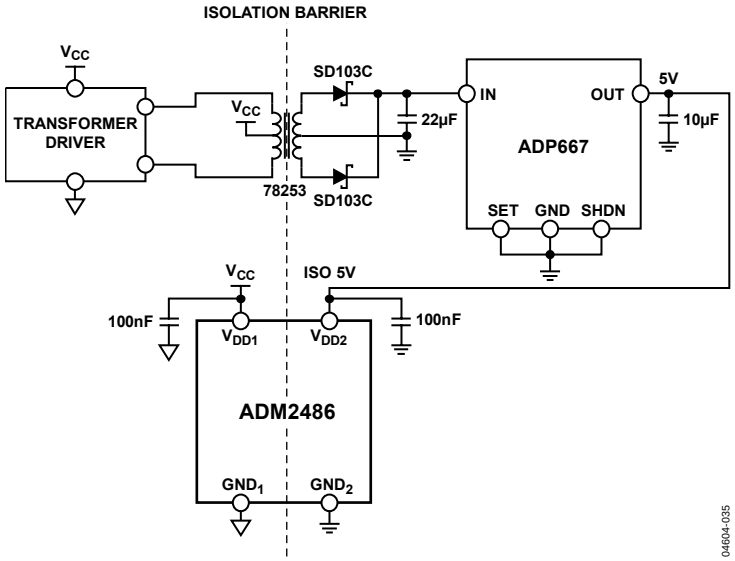
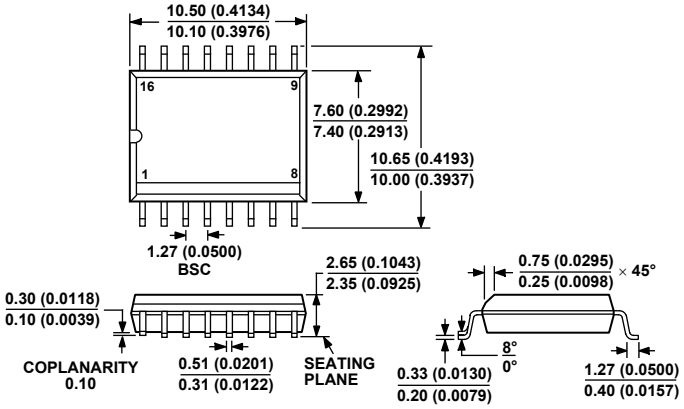



*Figure 32. Isolated Power Supply Circuit*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 33. 16-Lead Standard Small Outline Package [SOIC_W]*
*Wide Body (RW-16)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model | Data Rate (Mbps) | Temperature Range | Package Description | Ordering Quantity | Package Option |
|---|---|---|---|---|---|
| ADM2486BRW | 20 | −40°C to +85°C | 16-Lead SOIC_W | 47 | RW-16 |
| ADM2486BRW-REEL | 20 | −40°C to +85°C | 16-Lead SOIC_W | 1,000 | RW-16 |
| ADM2486BRWZ[1] | 20 | −40°C to +85°C | 16-Lead SOIC_W | 47 | RW-16 |
| ADM2486BRWZ-REEL[1] | 20 | −40°C to +85°C | 16-Lead SOIC_W | 1,000 | RW-16 |

[1] Z = Pb-free part.

## NOTES

## NOTES


D04604-0-2/06(D)