



# $\pm 15$ kV ESD-Protected, 3.3 V, 12 Mbps, EIA RS-485/RS-422 Transceiver

## ADM3485E

### FEATURES

- TIA/EIA RS-485/RS-422 compliant
- $\pm 15$  kV ESD protection on RS-485 input/output pins
- 12 Mbps data rate
- Half-duplex transceiver
- Up to 32 nodes on the bus
- Receiver open-circuit, fail-safe design
- Low power shutdown current
- Outputs high-Z when disabled or powered off
- Common-mode input range:  $-7$  V to  $+12$  V
- Thermal shutdown and short-circuit protection
- Industry-standard 75176 pinout
- 8-lead narrow SOIC package

### APPLICATIONS

- Power/energy metering
- Telecommunications
- EMI-sensitive systems
- Industrial control
- Local area networks

### GENERAL DESCRIPTION

The ADM3485E is a 3.3 V, low power data transceiver with  $\pm 15$  kV ESD protection, suitable for half-duplex communication on multipoint bus transmission lines. The ADM3485E is designed for balanced data transmission and complies with TIA/EIA standards RS-485 and RS-422. The ADM3485E is a half-duplex transceiver that shares differential lines and has separate enable inputs for the driver and the receiver.

The devices have a  $12\text{ k}\Omega$  receiver input impedance, which allows up to 32 transceivers on a bus. Because only one driver should be enabled at any time, the output of a

### FUNCTIONAL BLOCK DIAGRAM

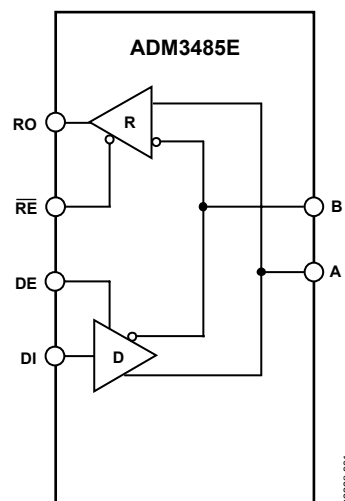


Figure 1.

disabled or powered-down driver is tristated to avoid overloading the bus.

The receiver has a fail-safe feature that ensures a logic high output when the inputs are floating. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit.

The part is fully specified over the industrial temperature range and is available in an 8-lead narrow SOIC package.

#### Rev. C

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## TABLE OF CONTENTS

|                                                      |   |                                                  |    |
|------------------------------------------------------|---|--------------------------------------------------|----|
| Features .....                                       | 1 | Test Circuits and Switching Characteristics..... | 7  |
| Applications.....                                    | 1 | Typical Performance Characteristics .....        | 9  |
| Functional Block Diagram .....                       | 1 | Standards and Testing.....                       | 11 |
| General Description .....                            | 1 | ESD Testing .....                                | 11 |
| Revision History .....                               | 2 | Applications Information .....                   | 12 |
| Specifications.....                                  | 3 | Differential Data Transmission .....             | 12 |
| Timing Specifications.....                           | 4 | Cable and Data Rate.....                         | 12 |
| Absolute Maximum Ratings.....                        | 5 | Receiver Open-Circuit Fail-Safe.....             | 12 |
| Thermal Resistance .....                             | 5 | Outline Dimensions .....                         | 13 |
| ESD Caution.....                                     | 5 | Ordering Guide .....                             | 13 |
| Pin Configuration and Pin Function Descriptions..... | 6 |                                                  |    |

## REVISION HISTORY

### 12/06—Rev. B to Rev. C

|                                                                         |           |
|-------------------------------------------------------------------------|-----------|
| Updated Format.....                                                     | Universal |
| Removed PDIP Model .....                                                | Universal |
| Changes to Features, Applications, and General Description ....         | 1         |
| Changes to Specifications .....                                         | 3         |
| Changes to Timing Specifications .....                                  | 4         |
| Changes to Absolute Maximum Ratings .....                               | 5         |
| Reorganized Test Circuits and Switching<br>Characteristics Section..... | 7         |
| Replaced Figure 3 to Figure 11 .....                                    | 7         |
| Deleted Figure 12 to Figure 14.....                                     | 8         |
| Changes to Figure 15 to Figure 20.....                                  | 9         |
| Changes to Figure 21 and Figure 22.....                                 | 10        |
| Changes to Table 9.....                                                 | 11        |
| Deleted Figure 24.....                                                  | 11        |
| Removed Fast Transient Burst Immunity<br>(IEC1000-4-4) Section .....    | 12        |
| Updated Outline Dimensions .....                                        | 13        |
| Changes to Ordering Guide .....                                         | 13        |

### 10/04—Rev. A to Rev. B

|                                                |           |
|------------------------------------------------|-----------|
| Updated Format.....                            | Universal |
| Changes to Power-Supply Current, Table 1 ..... | 3         |
| Updated Outline Dimensions .....               | 14        |
| Changes to Ordering Guide .....                | 14        |

### 5/00—Rev. 0 to Rev. A

## SPECIFICATIONS

$V_{CC} = +3.3 \text{ V} \pm 0.3 \text{ V}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

| Parameter                                                     | Symbol          | Min                      | Typ      | Max      | Unit          | Test Conditions/Comments                                                                  |
|---------------------------------------------------------------|-----------------|--------------------------|----------|----------|---------------|-------------------------------------------------------------------------------------------|
| <b>DRIVER</b>                                                 |                 |                          |          |          |               |                                                                                           |
| Differential Outputs                                          |                 |                          |          |          |               |                                                                                           |
| Differential Output Voltage                                   | $V_{OD}$        | 2.0                      |          |          | V             | $R_L = 100 \Omega$ (RS-422) (see Figure 3)                                                |
|                                                               |                 | 1.5                      |          |          | V             | $R_L = 54 \Omega$ (RS-485) (see Figure 3)                                                 |
|                                                               |                 | 1.5                      |          |          | V             | $R_L = 60 \Omega$ (RS-485) (see Figure 4)                                                 |
| $\Delta V_{OD} $ for Complementary Output States <sup>1</sup> | $\Delta V_{OD}$ |                          |          | 0.2      | V             | $R_L = 54 \Omega$ or $100 \Omega$ (see Figure 3)                                          |
| Common-Mode Output Voltage                                    | $V_{OC}$        |                          |          | 3        | V             | $R_L = 54 \Omega$ or $100 \Omega$ (see Figure 3)                                          |
| $\Delta V_{OC} $ for Complementary Output States <sup>1</sup> | $\Delta V_{OC}$ |                          |          | 0.2      | V             | $R_L = 54 \Omega$ or $100 \Omega$ (see Figure 3)                                          |
| Short-Circuit Output Current                                  | $I_{OSD}$       | -250                     |          |          | mA            | $V_{OUT} = -7 \text{ V}$                                                                  |
|                                                               |                 |                          |          | 250      | mA            | $V_{OUT} = 12 \text{ V}$                                                                  |
| Logic Inputs                                                  |                 |                          |          |          |               |                                                                                           |
| Input High Voltage                                            | $V_{IH}$        |                          |          | 0.8      | V             | DE, DI, $\overline{RE}$                                                                   |
| Input Low Voltage                                             | $V_{IL}$        | 2.0                      |          |          | V             | DE, DI, $\overline{RE}$                                                                   |
| Logic Input Current                                           | $I_{IN1}$       |                          |          | $\pm 2$  | $\mu\text{A}$ | DE, DI, $\overline{RE}$                                                                   |
| <b>RECEIVER</b>                                               |                 |                          |          |          |               |                                                                                           |
| Differential Inputs                                           |                 |                          |          |          |               |                                                                                           |
| Differential Input Threshold Voltage                          | $V_{TH}$        | -0.2                     |          | +0.2     | V             | $-7 \text{ V} < V_{CM} < +12 \text{ V}$                                                   |
| Input Voltage Hysteresis                                      | $\Delta V_{TH}$ |                          | 50       |          | mV            | $V_{CM} = 0 \text{ V}$                                                                    |
| Input Resistance (A, B)                                       | $R_{IN}$        | 12                       |          |          | k $\Omega$    | $-7 \text{ V} < V_{CM} < +12 \text{ V}$                                                   |
| Input Current (A, B)                                          | $I_{IN2}$       |                          |          | 1.0      | mA            | DE = 0 V, $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{IN} = 12 \text{ V}$             |
|                                                               |                 | -0.8                     |          |          | mA            | DE = 0 V, $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{IN} = -7 \text{ V}$             |
| RO Logic Output                                               |                 |                          |          |          |               |                                                                                           |
| Output Voltage High                                           | $V_{OH}$        | $V_{CC} - 0.4 \text{ V}$ |          |          | V             | $I_{OUT} = -1.5 \text{ mA}$ , $V_{ID} = 200 \text{ mV}$ (see Figure 5)                    |
| Output Voltage Low                                            | $V_{OL}$        |                          |          | 0.4      | V             | $I_{OUT} = 2.5 \text{ mA}$ , $V_{ID} = 200 \text{ mV}$ (see Figure 5)                     |
| Short-Circuit Output Current                                  | $I_{OSR}$       | $\pm 8$                  |          | $\pm 60$ | mA            | $0 \text{ V} < V_{RO} < V_{CC}$                                                           |
| Tristate Output Leakage Current                               | $I_{OZR}$       |                          |          | $\pm 1$  | $\mu\text{A}$ | $V_{CC} = 3.6 \text{ V}$ , $0 \text{ V} < V_{OUT} < V_{CC}$                               |
| <b>POWER SUPPLY CURRENT</b>                                   |                 |                          |          |          |               |                                                                                           |
| Voltage Range                                                 | $V_{CC}$        | 3.0                      |          | 3.6      | V             |                                                                                           |
| Supply Current                                                | $I_{CC}$        |                          | 1.1      | 2.2      | mA            | No load, DI = 0 V or $V_{CC}$ , DE = $V_{CC}$ , $\overline{RE} = 0 \text{ V}$ or $V_{CC}$ |
|                                                               |                 |                          | 0.95     | 1.9      | mA            | No load, DI = 0 V or $V_{CC}$ , DE = 0 V, $\overline{RE} = 0 \text{ V}$                   |
| Shutdown Current                                              | $I_{SHDN}$      |                          | 0.002    | 1        | $\mu\text{A}$ | DE = 0 V, $\overline{RE} = V_{CC}$ , DI = 0 V or $V_{CC}$                                 |
| <b>ESD PROTECTION</b>                                         |                 |                          |          |          |               |                                                                                           |
| A, B Pins                                                     |                 |                          | $\pm 15$ |          | kV            | Human body model                                                                          |
| All Pins Except A, B                                          |                 |                          | $\pm 4$  |          | kV            | Human body model                                                                          |

<sup>1</sup>  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in  $V_{OD}$  and  $V_{OC}$ , respectively, when DI input changes state.

## TIMING SPECIFICATIONS

$V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

Table 2.

| Parameter                                      | Symbol     | Min | Typ  | Max      | Unit | Test Conditions/Comments                                                         |
|------------------------------------------------|------------|-----|------|----------|------|----------------------------------------------------------------------------------|
| <b>DRIVER</b>                                  |            |     |      |          |      |                                                                                  |
| Maximum Data Rate                              |            | 12  | 15   |          |      |                                                                                  |
| Differential Output Delay                      | $t_{DD}$   | 1   | 22   | 35       | ns   | $R_L = 60 \Omega$ , $C_{L1} = C_{L2} = 15 \text{ pF}$ (see Figure 6)             |
| Differential Output Transition Time            | $t_{TD}$   | 3   | 11   | 25       | ns   | $R_L = 60 \Omega$ , $C_{L1} = C_{L2} = 15 \text{ pF}$ (see Figure 6)             |
| Propagation Delay                              |            |     |      |          |      |                                                                                  |
| From Low to High Level                         | $t_{PLH}$  | 7   | 23   | 35       | ns   | $R_L = 27 \Omega$ (see Figure 7)                                                 |
| From High to Low Level                         | $t_{PHL}$  | 7   | 23   | 35       | ns   | $R_L = 27 \Omega$ (see Figure 7)                                                 |
| $ t_{PLH} - t_{PHL} $ Propagation Delay Skew   | $t_{PDS}$  |     | -1.4 | $\pm 8$  | ns   | $R_L = 27 \Omega$ (see Figure 7)                                                 |
| Enable/Disable Timing                          |            |     |      |          |      |                                                                                  |
| Enable Time to Low Level                       | $t_{PZL}$  |     | 42   | 90       | ns   | $R_L = 110 \Omega$ (see Figure 9)                                                |
| Enable Time to High Level                      | $t_{PZH}$  |     | 42   | 90       | ns   | $R_L = 110 \Omega$ (see Figure 8)                                                |
| Disable Time from Low Level                    | $t_{PLZ}$  |     | 35   | 80       | ns   | $R_L = 110 \Omega$ (see Figure 9)                                                |
| Disable Time from High Level                   | $t_{PHZ}$  |     | 35   | 80       | ns   | $R_L = 110 \Omega$ (see Figure 8)                                                |
| Enable Time from Shutdown to Low Level         | $t_{PSL}$  |     | 650  | 900      | ns   | $R_L = 110 \Omega$ (see Figure 9)                                                |
| Enable Time from Shutdown to High Level        | $t_{PSH}$  |     | 650  | 900      | ns   | $R_L = 110 \Omega$ (see Figure 8)                                                |
| <b>RECEIVER</b>                                |            |     |      |          |      |                                                                                  |
| Propagation Delay                              |            |     |      |          |      |                                                                                  |
| From Low to High Level                         | $t_{RPLH}$ | 25  | 62   | 90       | ns   | $V_{ID} = 0 \text{ V to } 3.0 \text{ V}$ , $C_L = 15 \text{ pF}$ (see Figure 10) |
| From High to Low Level                         | $t_{RPHL}$ | 25  | 62   | 90       | ns   | $V_{ID} = 0 \text{ V to } 3.0 \text{ V}$ , $C_L = 15 \text{ pF}$ (see Figure 10) |
| $ t_{RPLH} - t_{RPHL} $ Propagation Delay Skew | $t_{RPDS}$ |     | 6    | $\pm 10$ | ns   | $V_{ID} = 0 \text{ V to } 3.0 \text{ V}$ , $C_L = 15 \text{ pF}$ (see Figure 10) |
| Enable/Disable Timing                          |            |     |      |          |      |                                                                                  |
| Enable Time to Low Level                       | $t_{RPZL}$ |     | 25   | 50       | ns   | $C_L = 15 \text{ pF}$ (see Figure 11)                                            |
| Enable Time to High Level                      | $t_{RPZH}$ |     | 25   | 50       | ns   | $C_L = 15 \text{ pF}$ (see Figure 11)                                            |
| Disable Time from Low Level                    | $t_{RPLZ}$ |     | 25   | 45       | ns   | $C_L = 15 \text{ pF}$ (see Figure 11)                                            |
| Disable Time from High Level                   | $t_{RPHZ}$ |     | 25   | 45       | ns   | $C_L = 15 \text{ pF}$ (see Figure 11)                                            |
| Enable Time from Shutdown to Low Level         | $t_{RPSL}$ |     | 720  | 1400     | ns   | $C_L = 15 \text{ pF}$ (see Figure 11)                                            |
| Enable Time from Shutdown to High Level        | $t_{RPSH}$ |     | 720  | 1400     | ns   | $C_L = 15 \text{ pF}$ (see Figure 11)                                            |
| Time to Shutdown <sup>1</sup>                  | $t_{SHDN}$ | 80  | 190  | 300      | ns   |                                                                                  |

<sup>1</sup> The transceivers are put into shutdown mode by bringing the  $\overline{RE}$  high and the DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the parts are in this state for 300 ns or more, the parts are guaranteed to enter shutdown.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter                                               | Values                        |
|---------------------------------------------------------|-------------------------------|
| $V_{CC}$ to GND                                         | –0.3 V to +6 V                |
| Digital Input/Output Voltage (DE, $\overline{RE}$ , DI) | –0.3 V to +6 V                |
| Receiver Output Voltage (RO)                            | –0.3 V to ( $V_{CC} + 0.3$ V) |
| Driver Output (A, B)/<br>Receiver Input (A, B) Voltage  | –8 V to +13 V                 |
| Driver Output Current                                   | ±250 mA                       |
| Power Dissipation (8-Lead SOIC_N)                       | 650 mW                        |
| Operating Temperature Range                             | –40°C to +85°C                |
| Storage Temperature Range                               | –65°C to +150°C               |
| Lead Temperature, Soldering (10 sec)                    | 300°C                         |
| Vapor Phase (60 sec)                                    | 215°C                         |
| Infrared (15 sec)                                       | 220°C                         |
| ESD Rating                                              |                               |
| Human Body Model (A, B)                                 | ±15 kV                        |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

| Package Type  | $\theta_{JA}$ | Unit |
|---------------|---------------|------|
| 8-Lead SOIC_N | 158           | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADM3485E

## PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

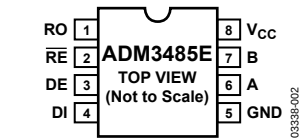


Figure 2. SOIC\_N Pin Configuration (R-8)

Table 5. Pin Function Descriptions

| Mnemonic        | Pin Number | Description                                                                                                                                                                                                                                    |
|-----------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RO              | 1          | Receiver Output. When enabled, if $A > B$ by 200 mV, then $RO = \text{high}$ . If $A < B$ by 200 mV, then $RO = \text{low}$ .                                                                                                                  |
| $\overline{RE}$ | 2          | Receiver Output Enable. With $\overline{RE}$ low, the receiver output (RO) is enabled. With $\overline{RE}$ high, the output goes into a high impedance state. If $\overline{RE}$ is high and DE is low, the ADM3485E enters a shutdown state. |
| DE              | 3          | Driver Output Enable. A high level enables the driver differential outputs A and B. A low level places it in a high impedance state.                                                                                                           |
| DI              | 4          | Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, while a logic high on DI forces A high and B low.                                                                                                         |
| GND             | 5          | Ground Connection, 0 V.                                                                                                                                                                                                                        |
| A               | 6          | Noninverting Receiver Input A/Driver Output A.                                                                                                                                                                                                 |
| B               | 7          | Inverting Receiver Input B/Driver Output B.                                                                                                                                                                                                    |
| V <sub>CC</sub> | 8          | Power Supply, 3.3 V $\pm$ 0.3 V.                                                                                                                                                                                                               |

## TEST CIRCUITS AND SWITCHING CHARACTERISTICS

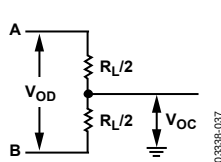


Figure 3. Driver Differential Output Voltage and Common-Mode Output Voltage

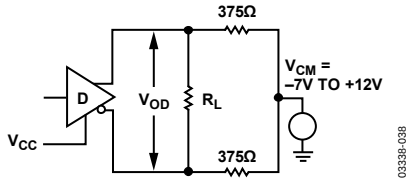


Figure 4. Driver Differential Output Voltage with Varying Common-Mode Voltage

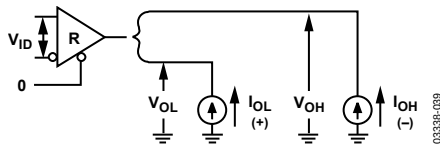
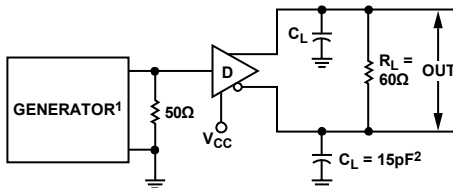


Figure 5. Receiver Output Voltage High and Output Voltage Low



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

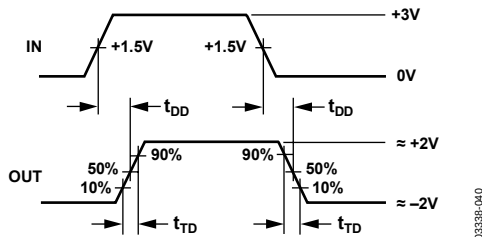
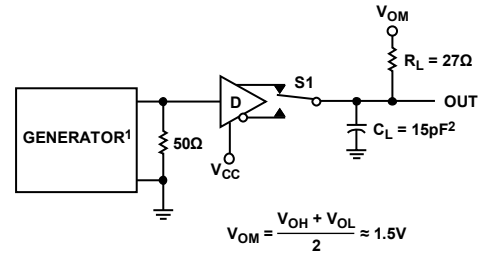


Figure 6. Driver Differential Output Delay and Transition Times



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

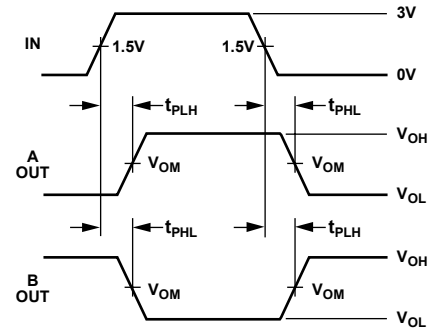
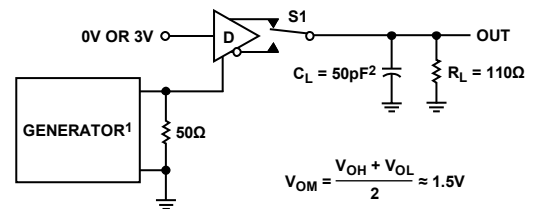


Figure 7. Driver Propagation Delays



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

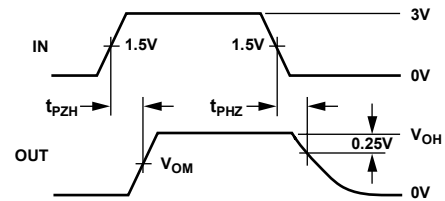
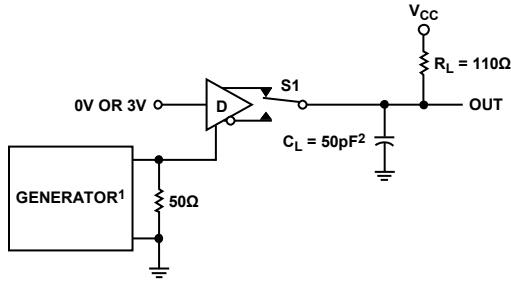


Figure 8. Driver Enable and Disable Times ( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

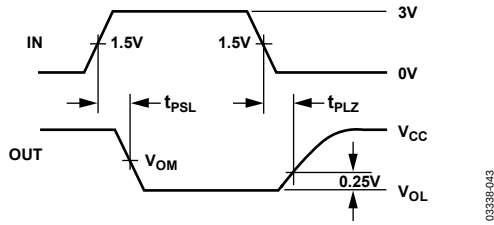
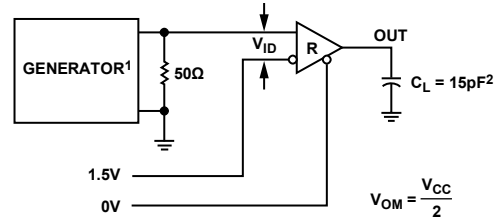


Figure 9. Driver Enable and Disable Times ( $t_{PLZ}$ ,  $t_{PSL}$ ,  $t_{PLZ}$ )



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

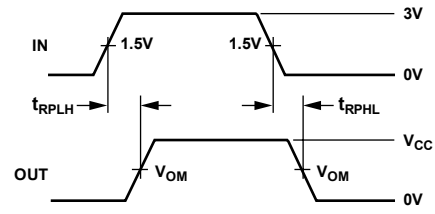
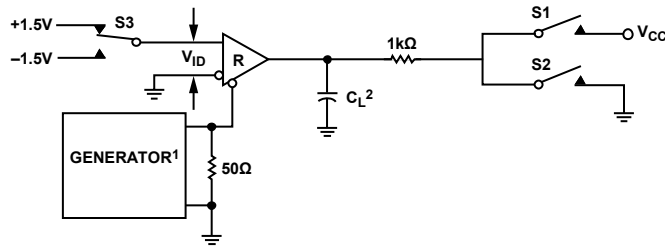


Figure 10. Receiver Propagation Delays



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_R \leq 6.0\text{ns}$ ,  $Z_O = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

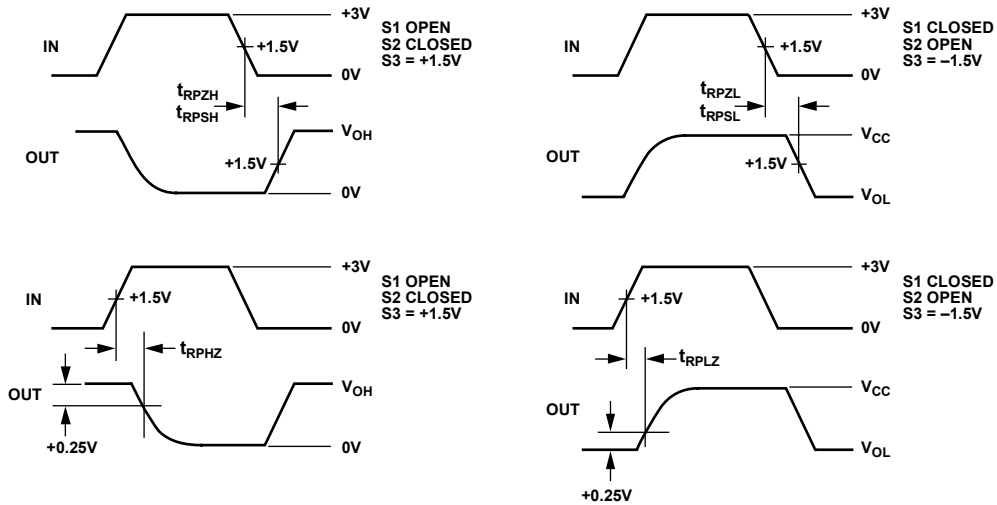


Figure 11. Receiver Enable and Disable Times

# TYPICAL PERFORMANCE CHARACTERISTICS

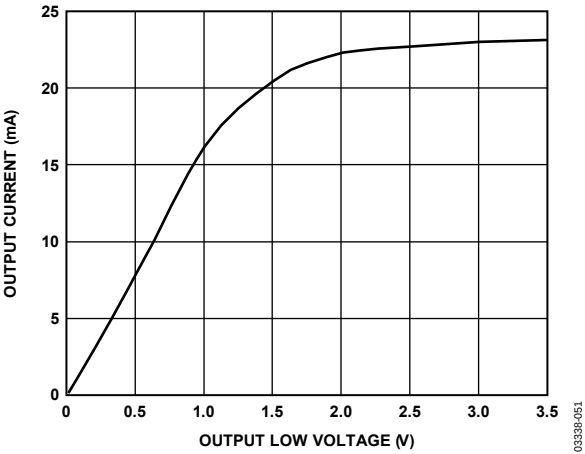


Figure 12. Output Current vs. Receiver Output Low Voltage

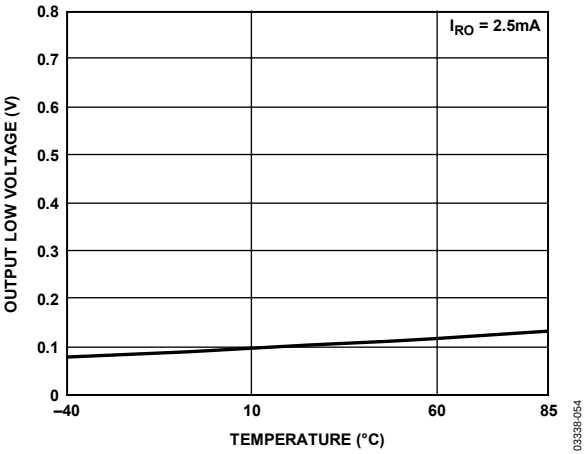


Figure 15. Receiver Output Low Voltage vs. Temperature

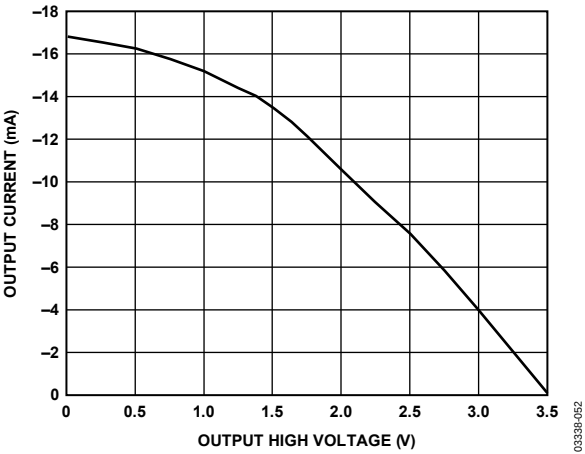


Figure 13. Output Current vs. Receiver Output High Voltage

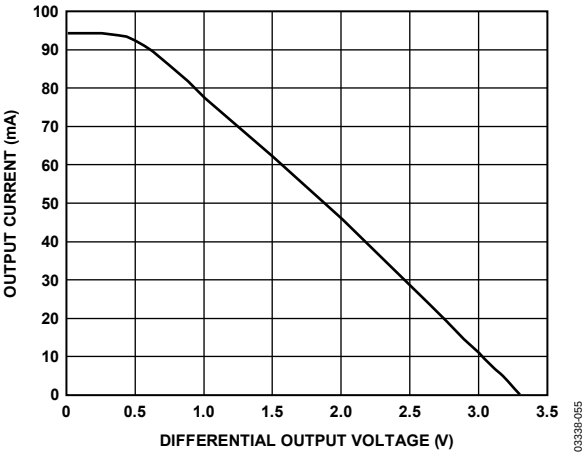


Figure 16. Driver Output Current vs. Differential Output Voltage

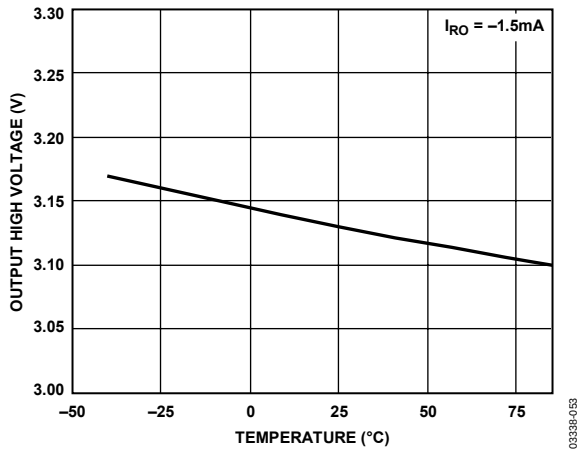


Figure 14. Receiver Output High Voltage vs. Temperature

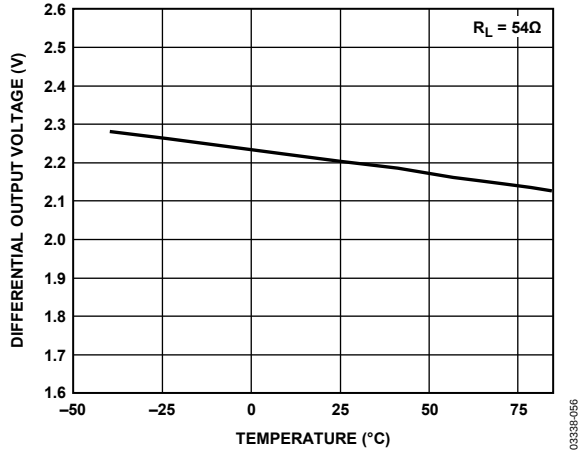


Figure 17. Driver Differential Output Voltage vs. Temperature

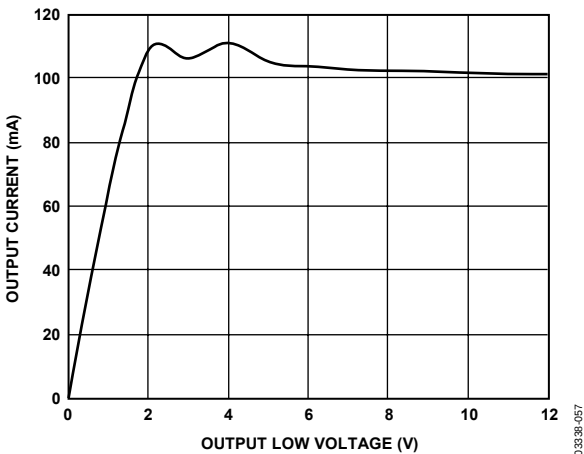


Figure 18. Output Current vs. Driver Output Low Voltage

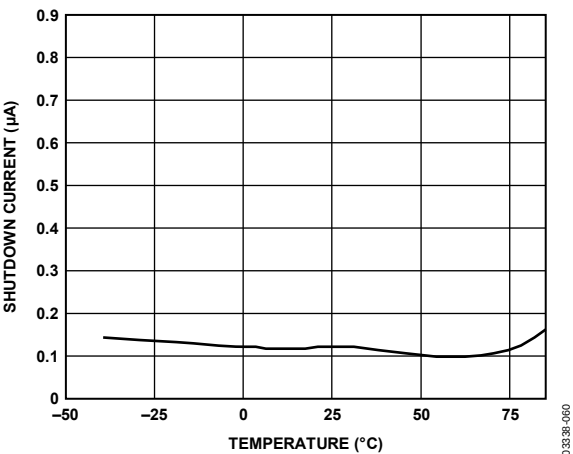


Figure 21. Shutdown Current vs. Temperature

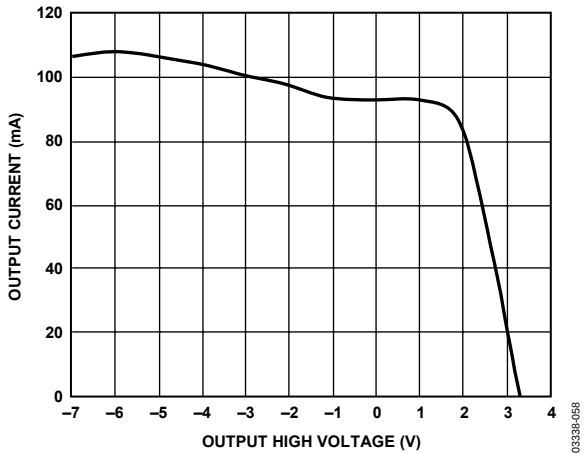


Figure 19. Output Current vs. Driver Output High Voltage

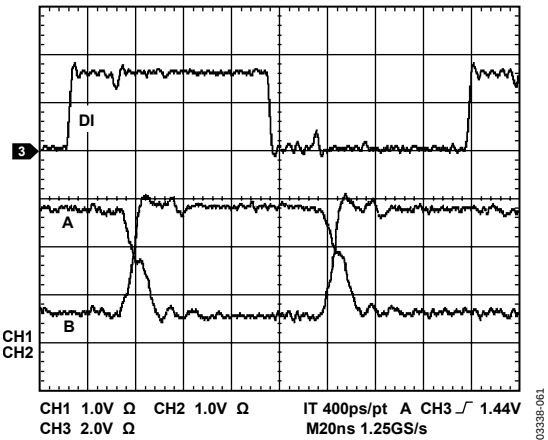


Figure 22. Driver Propagation Delay

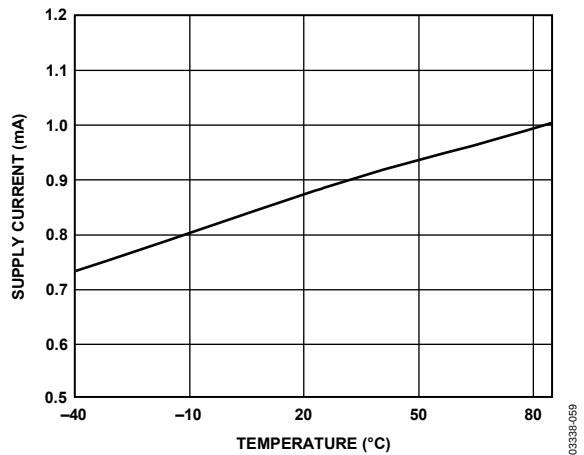


Figure 20. Supply Current vs. Temperature

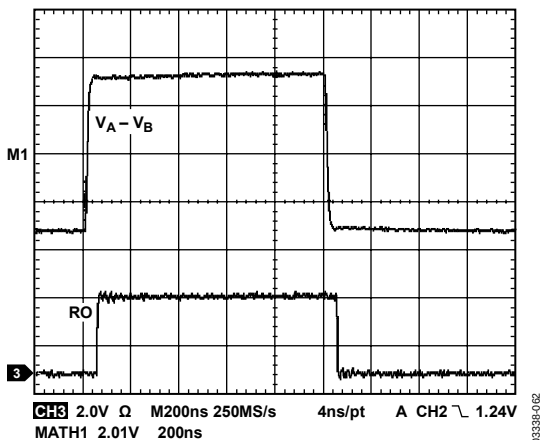


Figure 23. Receiver Propagation Delay,  
Driven by External RS-485 Device

## STANDARDS AND TESTING

Table 6 compares RS-422 and RS-485 interface standards, and Table 7 and Table 8 show transmitting and receiving truth tables.

**Table 6.**

| Specification                        | RS-422           | RS-485            |
|--------------------------------------|------------------|-------------------|
| Transmission Type                    | Differential     | Differential      |
| Maximum Data Rate                    | 10 Mbps          | 10 Mbps           |
| Maximum Cable Length                 | 4000 ft          | 4000 ft           |
| Minimum Driver Output Voltage        | $\pm 2$ V        | $\pm 1.5$ V       |
| Driver Load Impedance                | 100 $\Omega$     | 54 $\Omega$       |
| Receiver Input Resistance            | 4 k $\Omega$ min | 12 k $\Omega$ min |
| Receiver Input Sensitivity           | $\pm 200$ mV     | $\pm 200$ mV      |
| Receiver Input Voltage Range         | -7 V to +7 V     | -7 V to +12 V     |
| Number of Drivers/Receivers per Line | 1/10             | 32/32             |

**Table 7. Transmitting Truth Table**

| Transmitting Inputs    |    |                | Transmitting Outputs |                     |
|------------------------|----|----------------|----------------------|---------------------|
| $\overline{\text{RE}}$ | DE | DI             | B                    | A                   |
| X <sup>1</sup>         | 1  | 1              | 0                    | 1                   |
| X <sup>1</sup>         | 1  | 0              | 1                    | 0                   |
| 0                      | 0  | X <sup>1</sup> | High-Z <sup>2</sup>  | High-Z <sup>2</sup> |
| 1                      | 0  | X <sup>1</sup> | High-Z <sup>2</sup>  | High-Z <sup>2</sup> |

<sup>1</sup> X = don't care.

<sup>2</sup> High-Z = high impedance.

**Table 8. Receiving Truth Table**

| Receiving Inputs       |                | Receiving Outputs |                     |
|------------------------|----------------|-------------------|---------------------|
| $\overline{\text{RE}}$ | DE             | A – B             | RO                  |
| 0                      | X <sup>1</sup> | > +0.2 V          | 1                   |
| 0                      | X <sup>1</sup> | < -0.2 V          | 0                   |
| 0                      | X <sup>1</sup> | Inputs open       | 1                   |
| 1                      | X <sup>1</sup> | X <sup>1</sup>    | High-Z <sup>2</sup> |

<sup>1</sup> X = don't care.

<sup>2</sup> High-Z = high impedance.

## ESD TESTING

Two coupling methods are used for ESD testing, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air-gap discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air-gap discharge. This method is

influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. The contact discharge method, while less realistic, is more repeatable and is gaining acceptance and preference over the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device can suffer from parametric degradation, which can result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I/O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I/O port. It is extremely important, therefore, to have high levels of ESD protection on the I/O lines.

The ESD discharge could induce latch-up in the device under test, so it is important that ESD testing on the I/O pins be carried out while device power is applied. This type of testing is more representative of a real-world I/O discharge, where the equipment is operating normally when the discharge occurs.

**Table 9. ESD Test Results**

| ESD Test Method  | I/O Pins    |
|------------------|-------------|
| Human Body Model | $\pm 15$ kV |

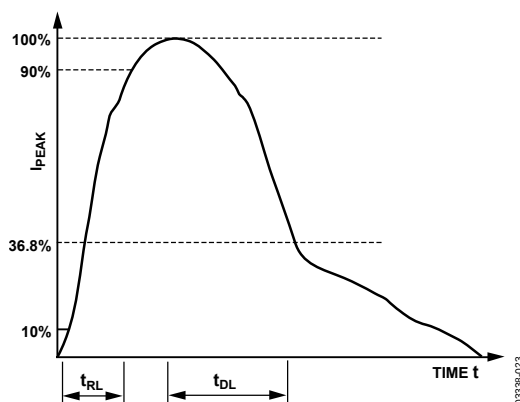


Figure 24. Human Body Model Current Waveform

APPLICATIONS INFORMATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line.

Two main standards that specify the electrical characteristics of transceivers used in differential data transmission are approved by the Electronics Industries Association (EIA). The RS-422 standard specifies data rates up to 10 Mbps and line lengths up to 4000 feet. A single driver can drive a transmission line with up to 10 receivers. The RS-485 standard was defined to cater to true multipoint communications. This standard meets or exceeds all the requirements of RS-422 but also allows multiple drivers and receivers to be connected to a single bus. An extended common-mode range of -7 V to +12 V is defined.

The most significant difference between RS-422 and RS-485 is the fact that under the RS-485 standard the drivers may be disabled, thereby allowing more than one to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted-pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM3485E is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 25. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths off the main line must also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

RECEIVER OPEN-CIRCUIT FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

Table 10. RS-422 and RS-485 Interface Standards

| Specification                 | RS-422       | RS-485        |
|-------------------------------|--------------|---------------|
| Transmission Type             | Differential | Differential  |
| Maximum Cable Length          | 4000 ft      | 4000 ft       |
| Minimum Driver Output Voltage | ±2 V         | ±1.5 V        |
| Driver Load Impedance         | 100 Ω        | 54 Ω          |
| Receiver Input Resistance     | 4 kΩ min     | 12 kΩ min     |
| Receiver Input Sensitivity    | ±200 mV      | ±200 mV       |
| Receiver Input Voltage Range  | -7 V to +7 V | -7 V to +12 V |

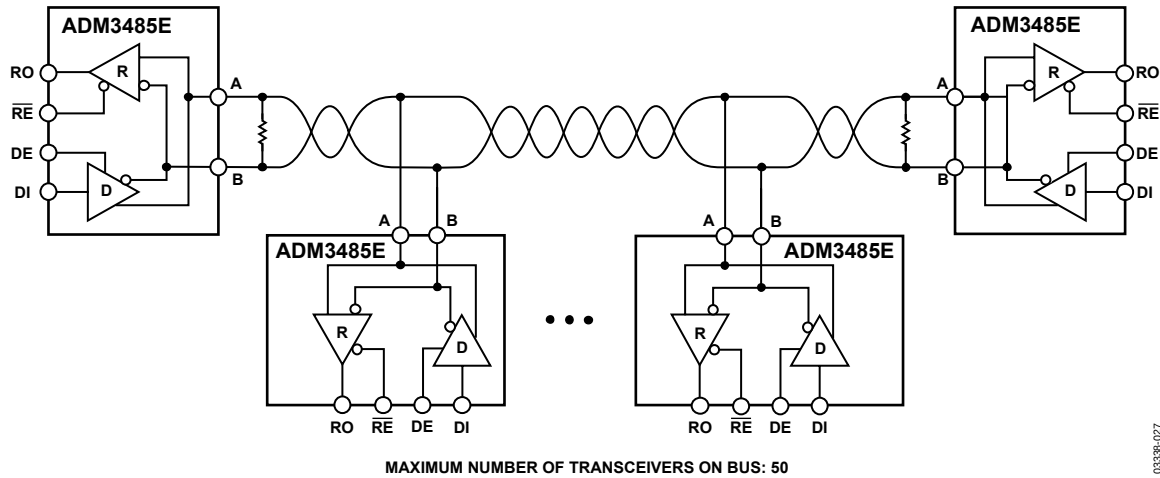
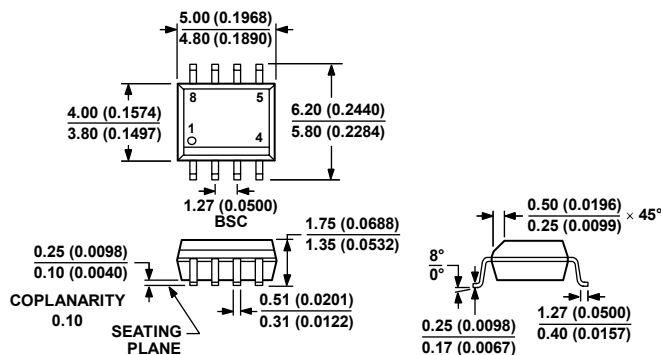


Figure 25. Multipoint Transmission Network

03336-027

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 8-Lead Standard Small Outline Package [SOIC\_N]

Narrow Body

(R-8)

Dimensions shown in millimeters and (inches)

06050E-A

## ORDERING GUIDE

| Model                          | Temperature Range | Package Description                            | Package Option |
|--------------------------------|-------------------|------------------------------------------------|----------------|
| ADM3485EAR                     | −40°C to +85°C    | 8-Lead Standard Small Outline Package [SOIC_N] | R-8            |
| ADM3485EAR-REEL7               | −40°C to +85°C    | 8-Lead Standard Small Outline Package [SOIC_N] | R-8            |
| ADM3485EAR-REEL                | −40°C to +85°C    | 8-Lead Standard Small Outline Package [SOIC_N] | R-8            |
| ADM3485EARZ <sup>1</sup>       | −40°C to +85°C    | 8-Lead Standard Small Outline Package [SOIC_N] | R-8            |
| ADM3485EARZ-REEL7 <sup>1</sup> | −40°C to +85°C    | 8-Lead Standard Small Outline Package [SOIC_N] | R-8            |
| ADM3485EARZ-REEL <sup>1</sup>  | −40°C to +85°C    | 8-Lead Standard Small Outline Package [SOIC_N] | R-8            |

<sup>1</sup> Z = Pb-free part.

**NOTES**

NOTES

**ADM3485E**

## **NOTES**