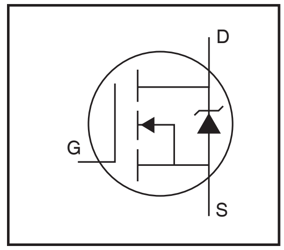
PD - 96385

International
IOR Rectifier

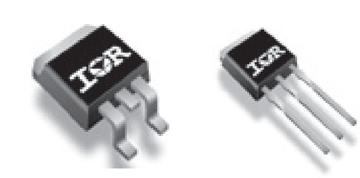
AUTOMOTIVE GRADE

AUIRL1404S
AUIRL1404L
HEXFET® Power MOSFET

Features
- Advanced Planar Technology
- Logic-Level Gate Drive
- Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



$V_{(BR)DSS}$	**40V**
$R_{DS(on)}$ **max.**	**4mΩ**
I_D	**160A⑥**



D²Pak AUIRL1404S   TO-262 AUIRL1404L

G	D	S
Gate	Drain	Source

Description
Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Absolute Maximum Ratings
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	160 ⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	110 ⑥	
I_{DM}	Pulsed Drain Current ①	640	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	200	
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	520	mJ
I_{AR}	Avalanche Current ①	95	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient (PCB mounted)⑦	–––	40	

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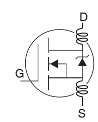
*Qualification standards can be found at http://www.irf.com/

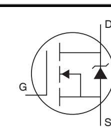
Static Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	–––	–––	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.038	–––	V/°C	Reference to 25°C, $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	4.0	mΩ	$V_{GS} = 10V$, $I_D = 95A$ ④
		–––	–––	5.9		$V_{GS} = 4.3V$, $I_D = 40A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–––	3.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
gfs	Forward Transconductance	93	–––	–––	S	$V_{DS} = 25V$, $I_D = 95A$
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	μA	$V_{DS} = 40V$, $V_{GS} = 0V$
		–––	–––	250		$V_{DS} = 32V$, $V_{GS} = 0V$, $T_J = 150°C$
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	–––	–––	-200		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

Q_g	Total Gate Charge	–––	–––	140	nC	$I_D = 95A$
Q_{gs}	Gate-to-Source Charge	–––	–––	48		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	60		$V_{GS} = 5.0V$,See Fig 6 ④
$t_{d(on)}$	Turn-On Delay Time	–––	18	–––	ns	$V_{DD} = 20V$
t_r	Rise Time	–––	270	–––		$I_D = 95A$
$t_{d(off)}$	Turn-Off Delay Time	–––	38	–––		$R_G = 2.5\Omega$,$V_{GS} = 4.5V$
t_f	Fall Time	–––	130	–––		$R_D = 0.25\Omega$ ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	–––	7.5	–––		Between lead, and center of die contact
C_{iss}	Input Capacitance	–––	6600	–––	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	–––	1700	–––		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	–––	350	–––		ƒ = 1.0MHz, See Fig.5
C_{oss}	Output Capacitance	–––	6700	–––		$V_{GS} = 0V$, $V_{DS} = 1.0V$, ƒ =1.0MHz
C_{oss}	Output Capacitance	–––	1500	–––		$V_{GS} = 0V$, $V_{DS} = 32V$, ƒ =1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance⑤	–––	1500	–––		$V_{GS} = 0V$, $V_{DS} = 0V$ to 32V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	160⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	640		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	$T_J = 25°C$, $I_S = 95A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	–––	63	94	ns	$T_J = 25°C$, $I_F = 95A$
Q_{rr}	Reverse Recovery Charge	–––	170	250	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, $L = 0.35mH$, $R_G = 25\Omega$, $I_{AS} = 95A$. (See Figure 12)

③ $I_{SD} \leq 95A$, $di/dt \leq 160A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handing of the package refer to Design Tip # 93-4.

⑦ This is applied to D^2Pak, When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994.

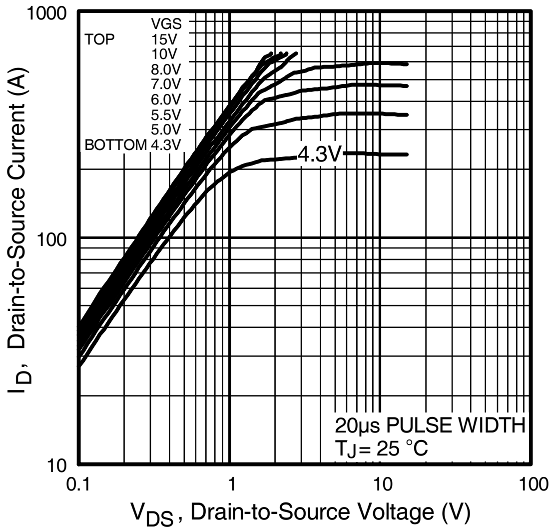


Fig 1. Typical Output Characteristics

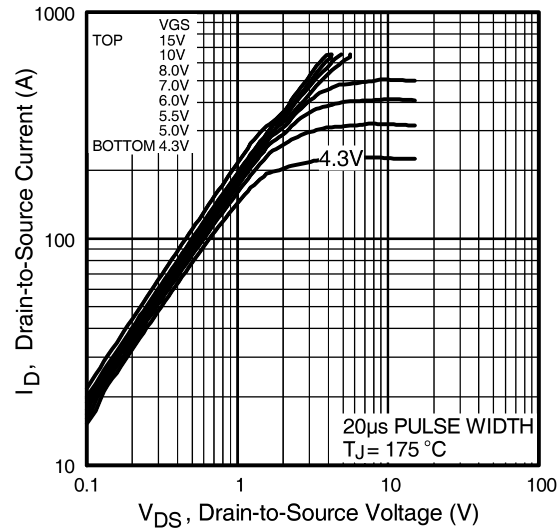


Fig 2. Typical Output Characteristics

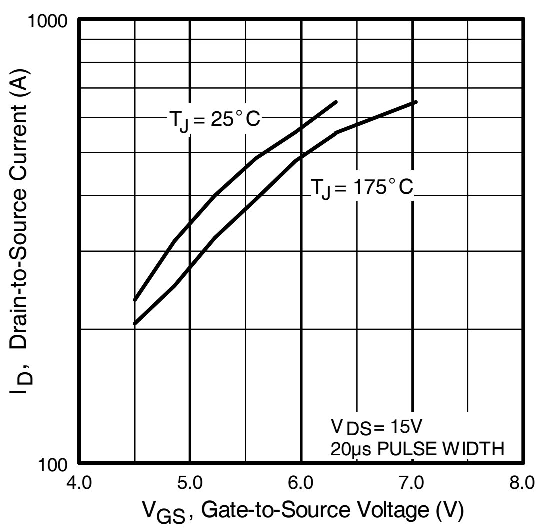


Fig 3. Typical Transfer Characteristics

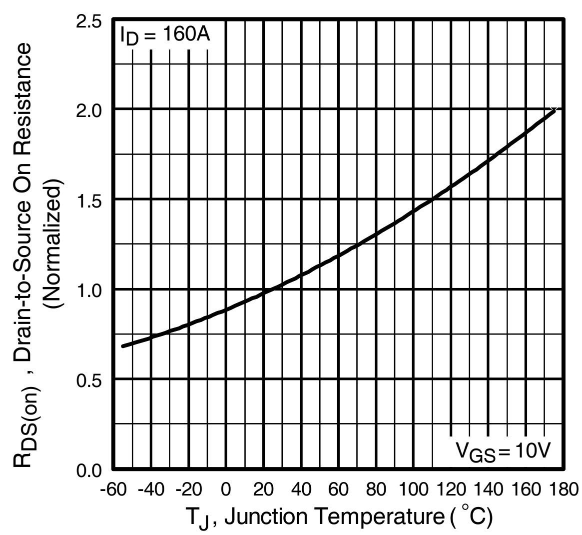


Fig 4. Normalized On-Resistance Vs. Temperature

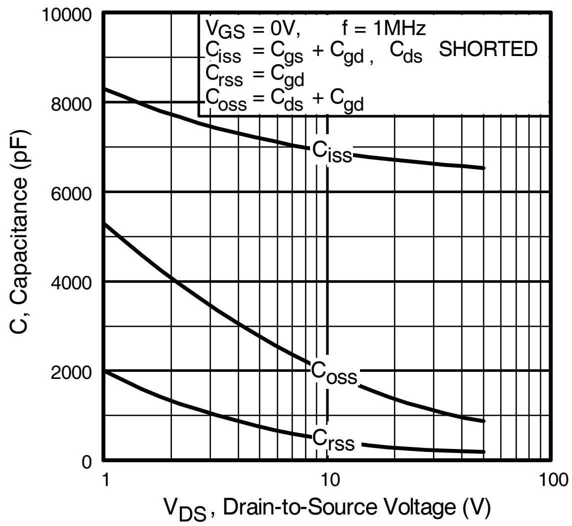


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

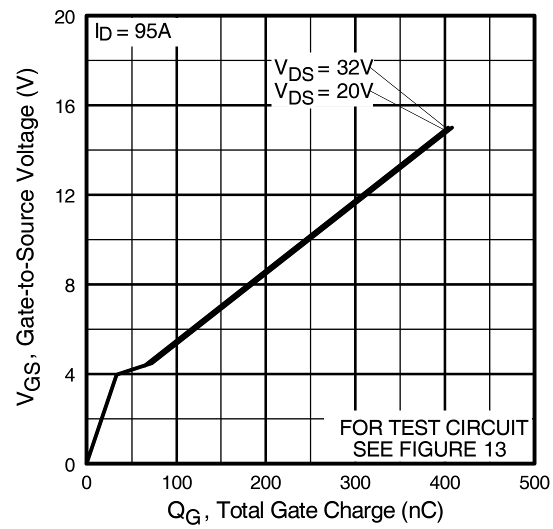


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

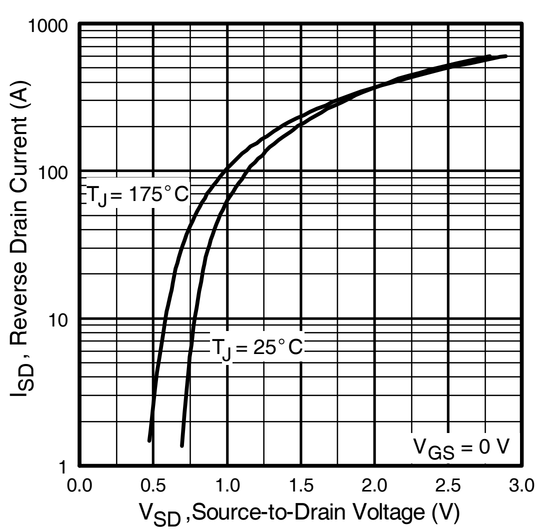


Fig 7. Typical Source-Drain Diode Forward Voltage

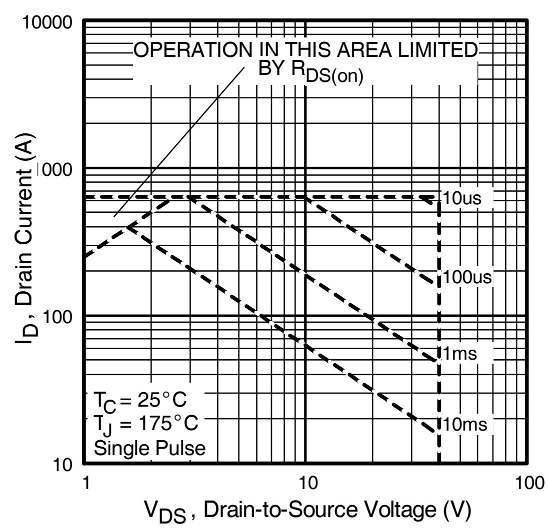


Fig 8. Maximum Safe Operating Area

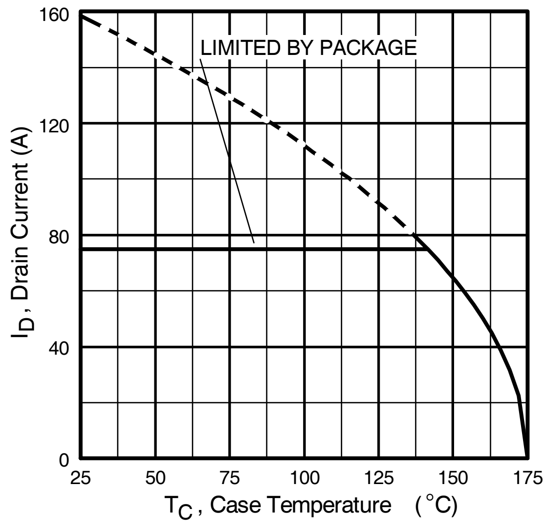
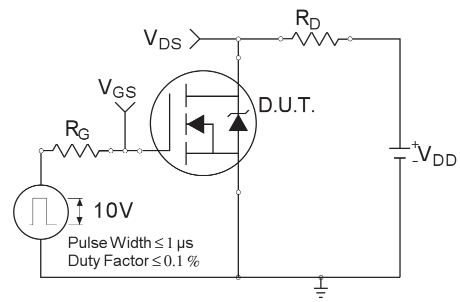
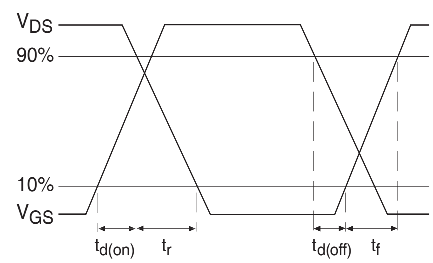


Fig 9. Maximum Drain Current Vs. Case Temperature





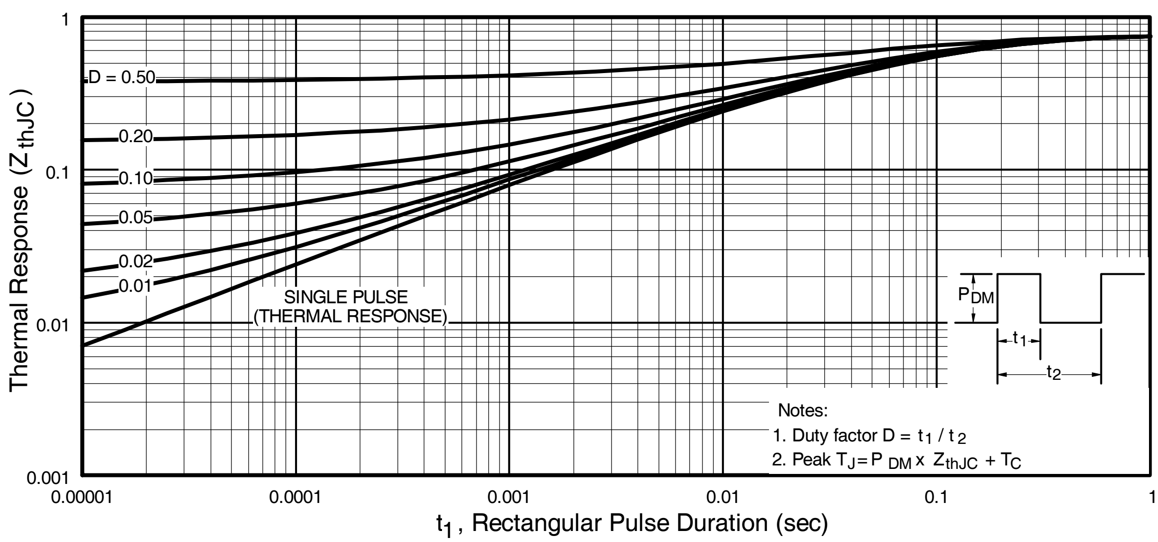


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

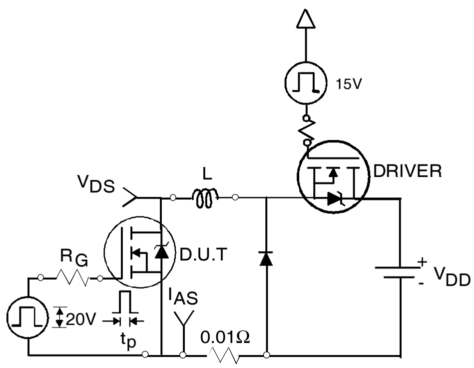


Fig 12a. Unclamped Inductive Test Circuit

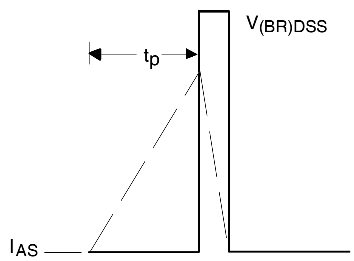


Fig 12b. Unclamped Inductive Waveforms

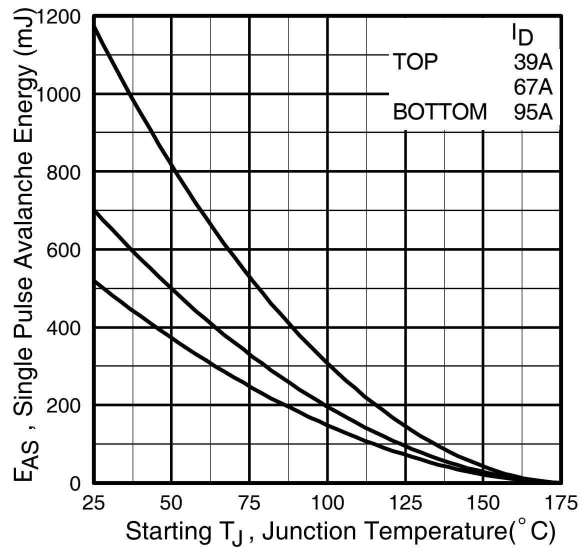


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

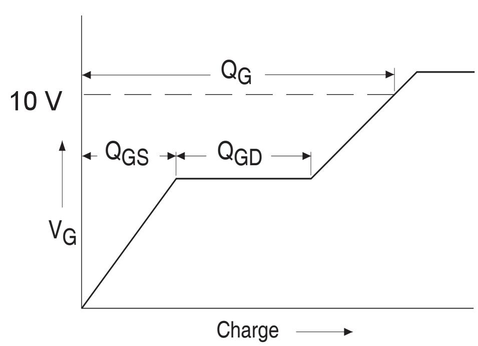


Fig 13a. Basic Gate Charge Waveform

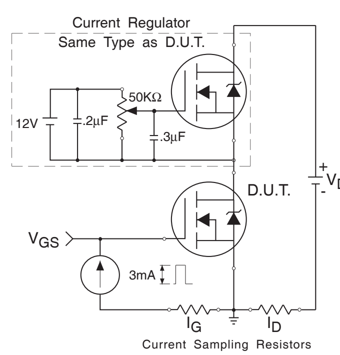
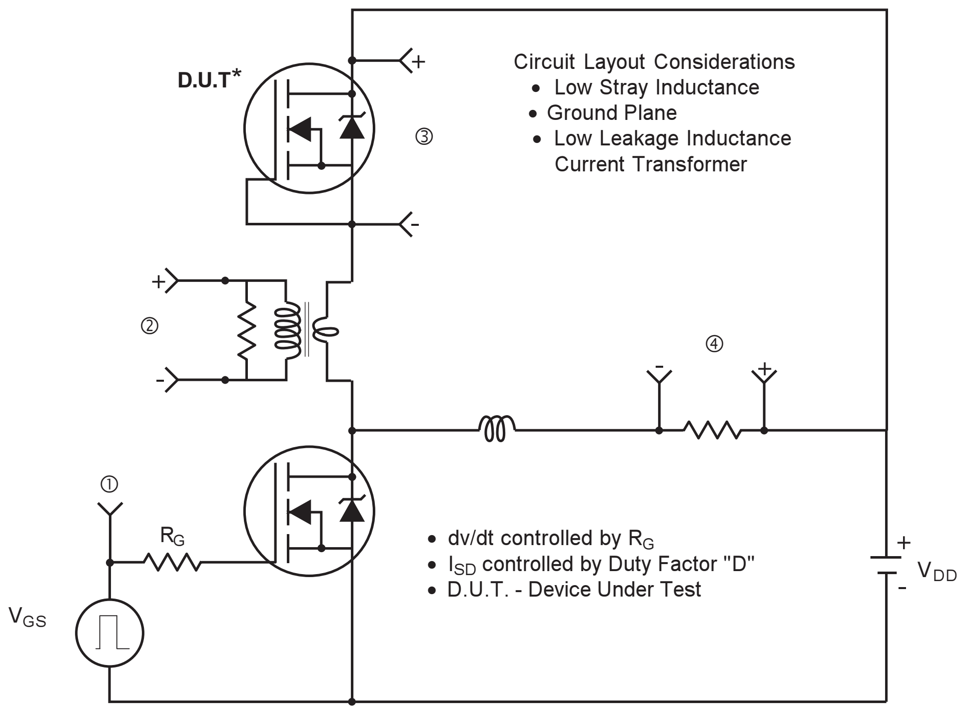
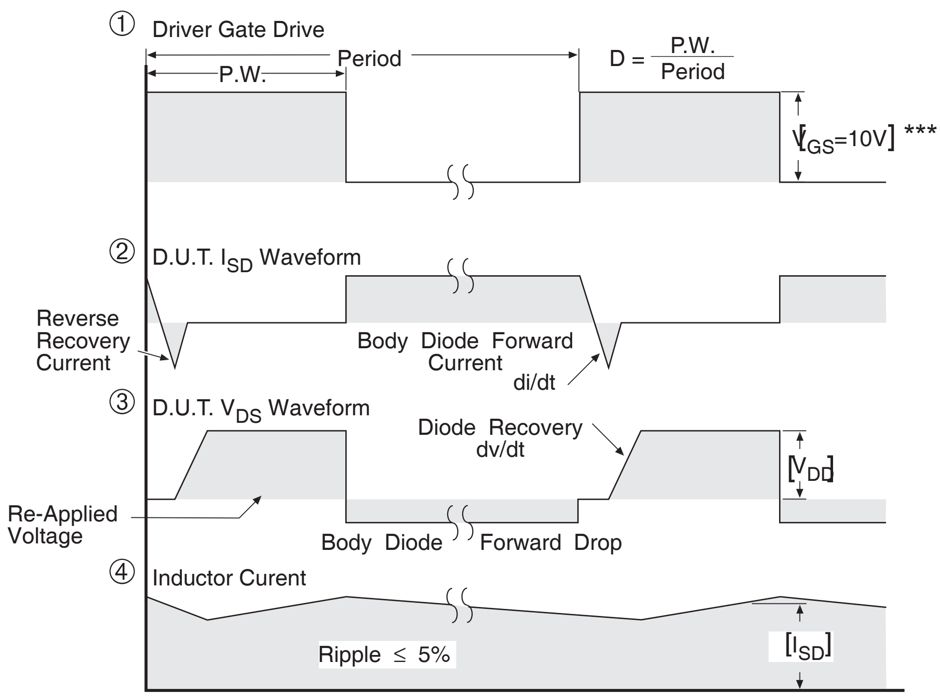


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



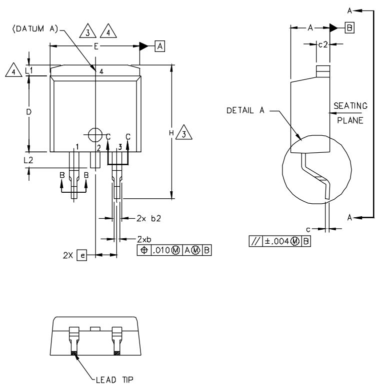
* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

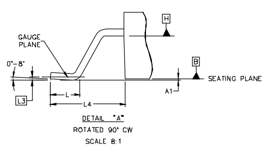
Fig 14. For N-channel HEXFET® power MOSFETs

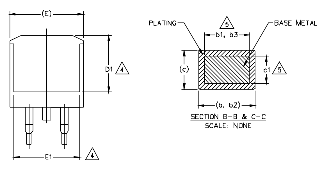
D^2Pak Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.





SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

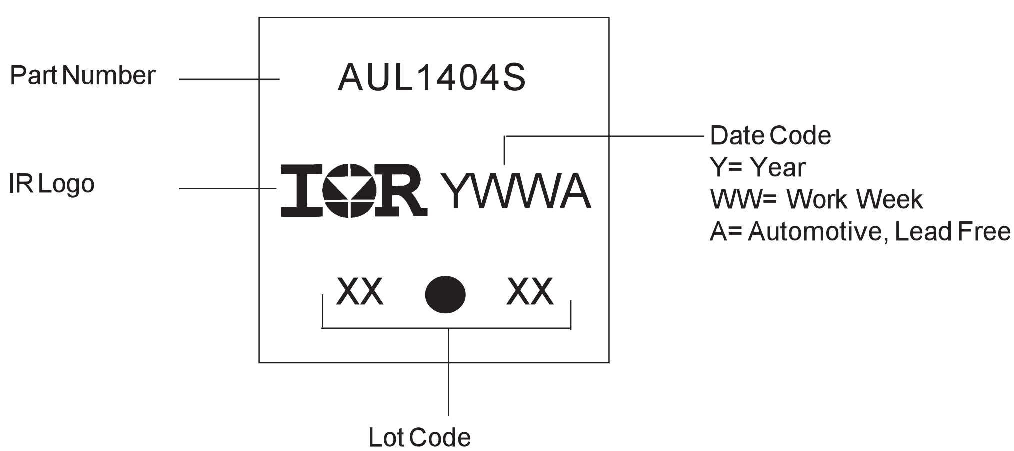
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE *
2, 4.– CATHODE
3.– ANODE

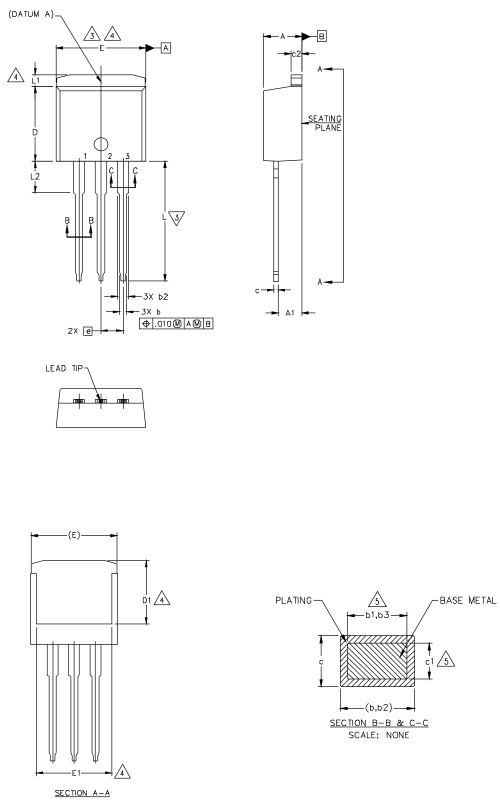
* PART DEPENDENT.

D^2Pak Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

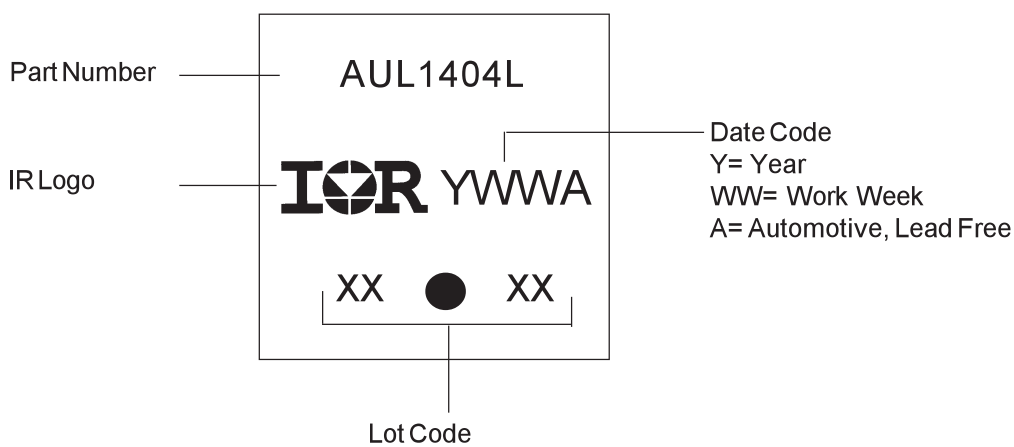
HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

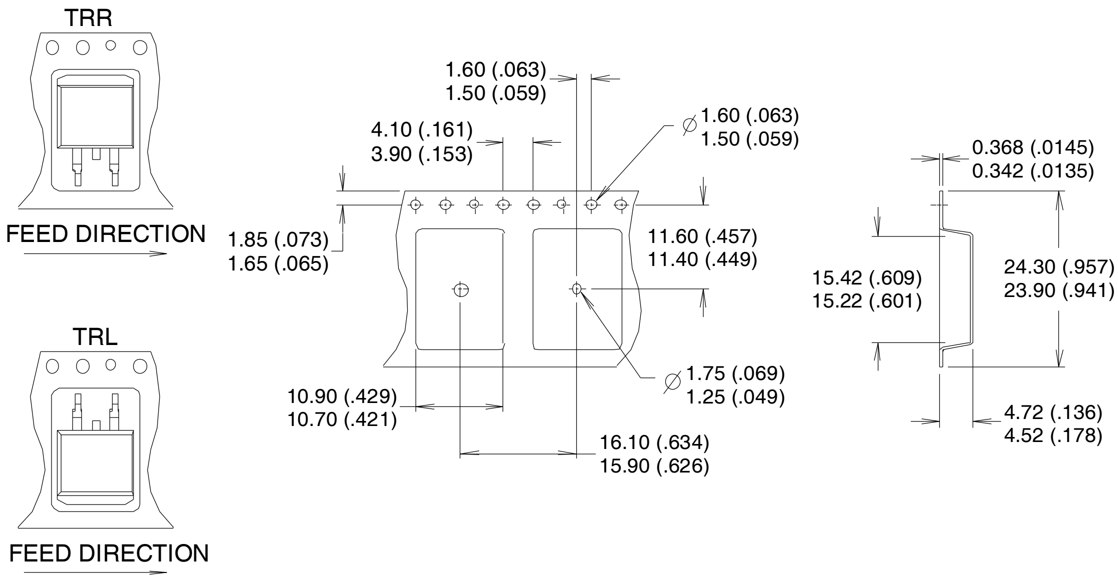
TO-262 Part Marking Information

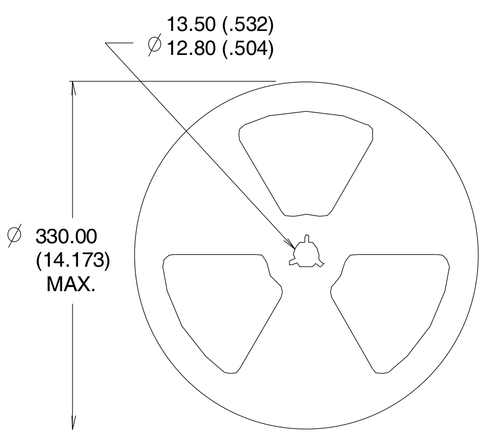


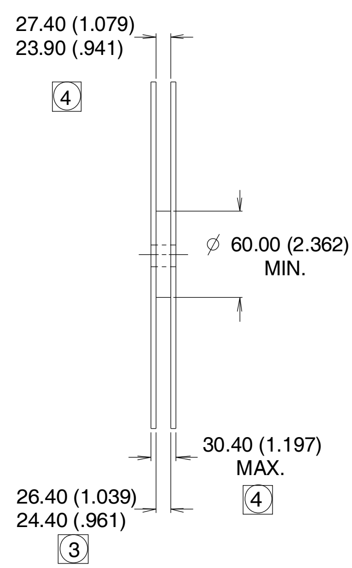
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D^2Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Ordering Information

Base part	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRL1404L	TO-262	Tube	50	AUIRL1404L
AUIRL1404S	D2Pak	Tube	50	AUIRL1404S
		Tape and Reel Left	800	AUIRL1404STRL
		Tape and Reel Right	800	AUIRL1404STRR

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