

SYNC separator IC with AFC

BA7046 / BA7046F

The BA7046 and BA7046F separate the synchronization signals from a video signal and output the horizontal and vertical synchronization signals (H_D and V_D), and the composite synchronization signal (Sync-out). The H_D and V_D pulse phase difference is guaranteed.

●Applications

TVs and VCRs

●Features

- 1) Built-in AFC circuit.
- 2) H_D and V_D phase difference guaranteed.
- 3) Low power dissipation. (approx. 21mW)
- 4) Low external parts count.
- 5) 8-pin DIP / SOP package.
- 6) Horizontal free-run frequency does not require adjustment.

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

BA7046 (DIP)

Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{CC \text{ Max.}}$	8.0	V
Power dissipation	P_d	500*	mW
Operating temperature	T_{opr}	- 20 ~ + 75	$^\circ\text{C}$
Storage temperature	T_{stg}	- 55 ~ + 125	$^\circ\text{C}$

* Reduced by 5mW for each increase in T_a of 1°C over 25°C .

BA7046F (SOP)

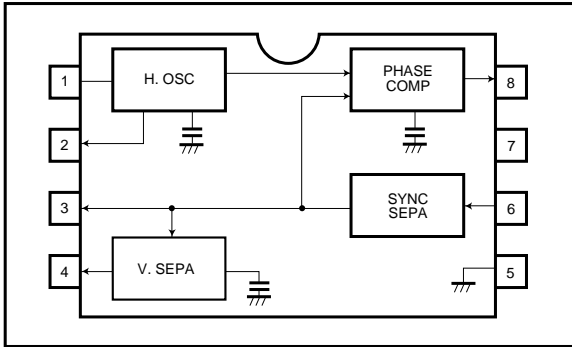
Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{CC \text{ Max.}}$	8.0	V
Power dissipation	P_d	350*	mW
Operating temperature	T_{opr}	- 20 ~ + 75	$^\circ\text{C}$
Storage temperature	T_{stg}	- 55 ~ + 125	$^\circ\text{C}$

* When mounted on a 50mm × 50mm PCB board, reduced by 3.5mW for each increase in T_a of 1°C over 25°C .

●Recommended operating conditions ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{CC}	4.5	—	5.5	V

●Block diagrams



●Pin descriptions

Pin No.	Function
1	Horizontal oscillator resistor
2	H _D output
3	SYNC output (open collector)
4	V _D output
5	GND
6	Video input
7	Power supply
8	Phase comparator output

●Input / output circuits

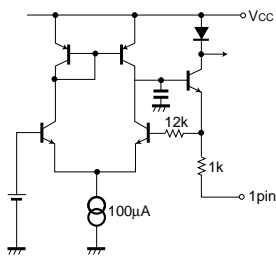


Fig. 1

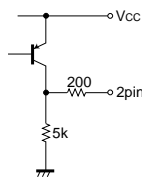


Fig. 2

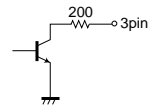


Fig. 3

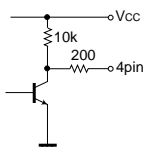


Fig. 4

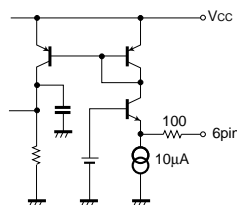


Fig. 5

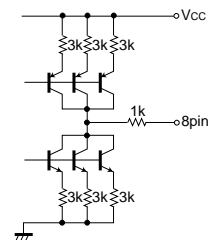


Fig. 6

●Electrical characteristics (unless otherwise noted Ta = 25°C and Vcc = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I _Q	2.0	4.1	6.2	mA	pin 3 open
Minimum synchronization separation level	V _{syn-Min.}	—	0.08	0.15	V _{P-P}	pin 6 terminated with 75Ω resistor
Pulse voltage, LOW	V _{P-L}	—	0.1	0.3	V	pins 2, 4
Pulse voltage, HIGH	V _{P-H}	4.7	4.9	—	V	pins 2, 4
(Horizontal) free-running frequency	f _{H-O}	13.9	15.7	17.5	kHz	No input signal, I ₁ = open
Capture range	Δf _{CAP}	± 2.1	± 2.9	—	kHz	
Lock-in phase difference	T _{HPPH}	- 1.0	0	+ 1.0	μs	pin2 ↙ pin- 6 ↘
H _D , V _D phase difference	T _{HVD}	17.0	23.5	30.0	μs	pin4 ↙ pin- 2 ↗
H _D pulse width	T _{HD}	4.6	5.1	5.6	μs	pin2 ↙ ↗
V _D pulse width	T _{VD}	190	230	270	μs	pin4 ↙ ↗

○ Not designed for radiation resistance.

●Measurement circuit

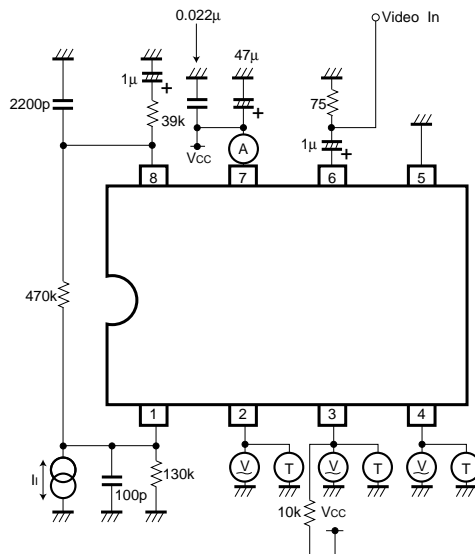


Fig. 7

●Circuit operation

(1) Synchronization separation circuit

Detects the charging current to an externally-connected capacitor, and performs synchronization separation.

(2) Horizontal oscillation circuit

When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency

is determined by external resistor R1.

$$f_{H-O} = \frac{2.05E6}{R_1} \text{ [kHz]}$$

(3) Vertical synchronization separation circuit

When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

● V_{IN} , H_D and V_D timing charts

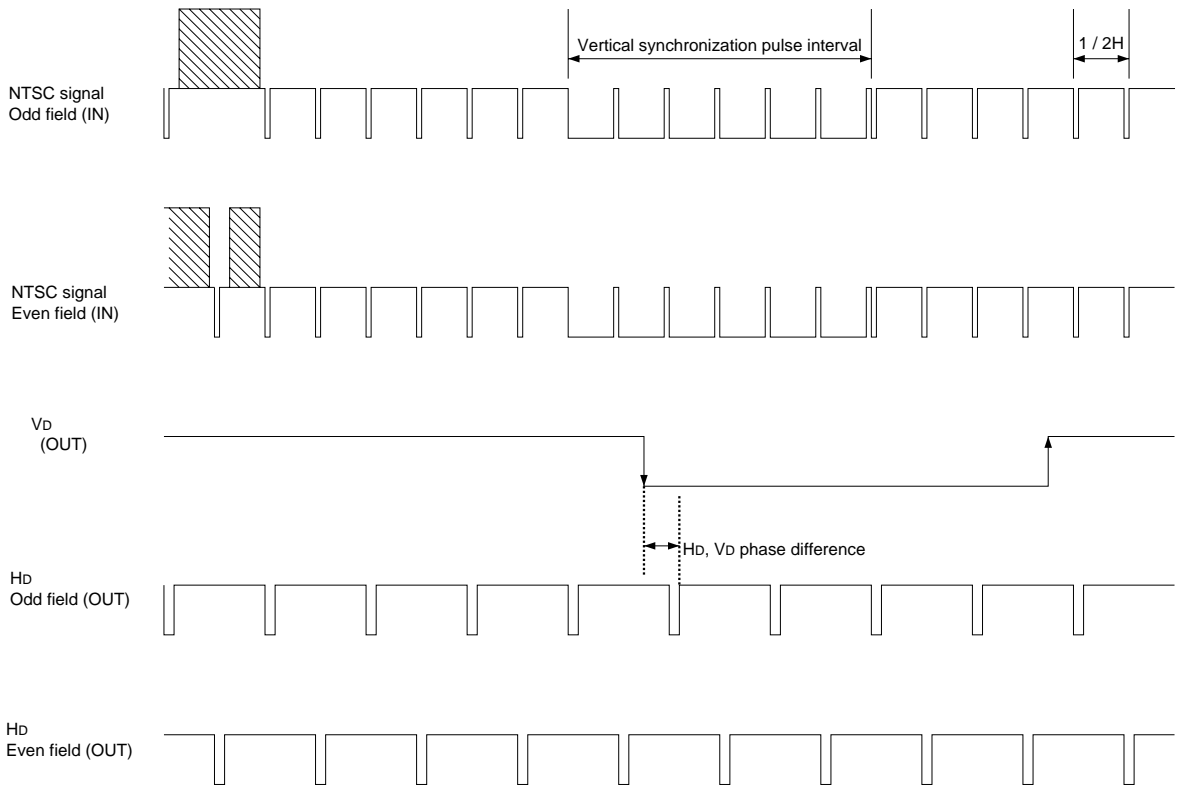
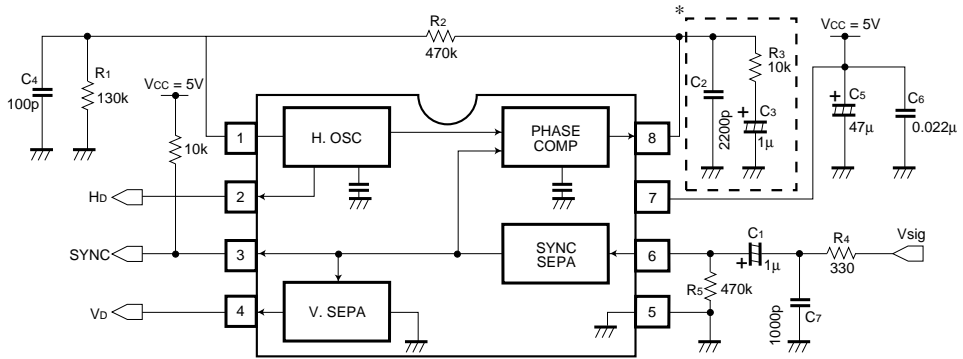


Fig. 8

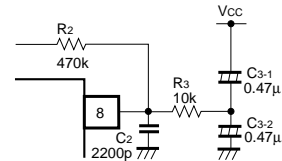
- (1) The rise and fall positions for V_D are basically the same for both odd and even fields.
- (2) H_D shifts by $1 / 2H$ during the odd and even field interval.
- (3) Only the odd field is given for the specification.

●Application example



* By configuring the circuit enclosed in the dotted line to that in the diagram on the right, you can decrease the lock-in time and increase the capture range.

Fig.9



- When SYNC SEPA output only is used. H_b and V_b unused.

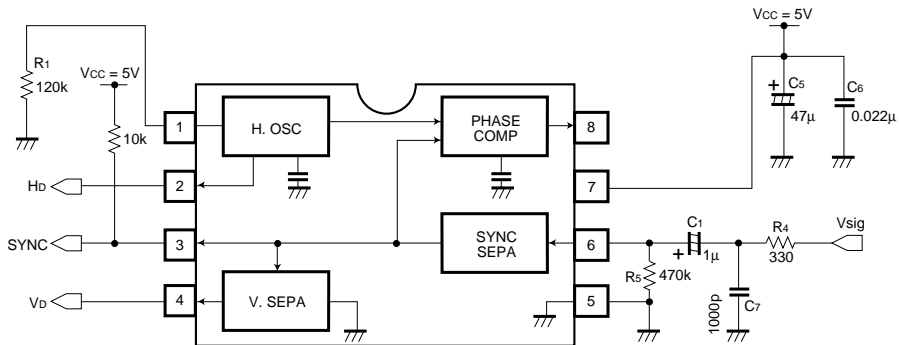


Fig. 10

- (1) Connect pin 1 to GND via a 120kΩ (approx.) resistor. Leave pins 2, 4 and 8 open.
- (2) SYNC output polarity (pin 3) is positive.
- (3) The delay time for rising edge of the SYNC output (pin 3) with respect to the falling edge of Sync for the V_{sig} input signal (pin 6) is 850ns (reference value).
- (4) The delay time for falling edge of the SYNC output (pin 3) with respect to the rising edge of Sync for the V_{sig} input signal (pin 6) is 450ns (reference value).

●Attached components

Resistor R₁ should have a tolerance of ± 2%, and a temperature coefficient of 100ppm or lower.

●Electrical characteristic curves

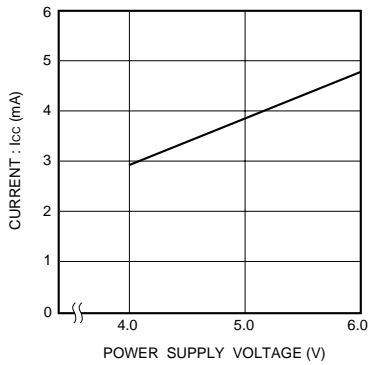


Fig. 11 Quiescent current vs. power supply voltage

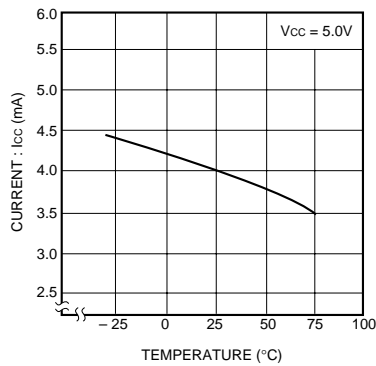


Fig. 12 Quiescent current vs. temperature

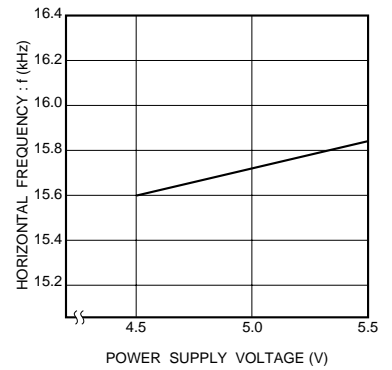


Fig. 13 Horizontal free-running frequency vs. power supply voltage

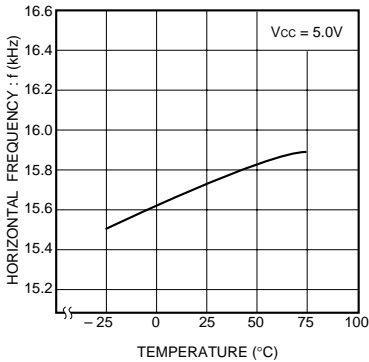


Fig. 14 Horizontal free-running frequency vs. temperature

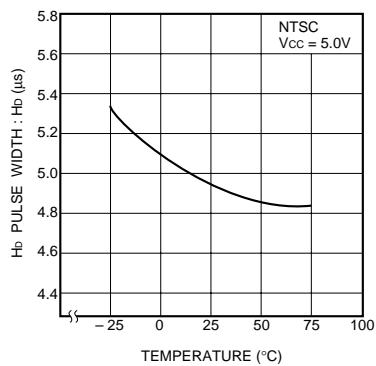


Fig. 15 Hd pulse width vs. temperature

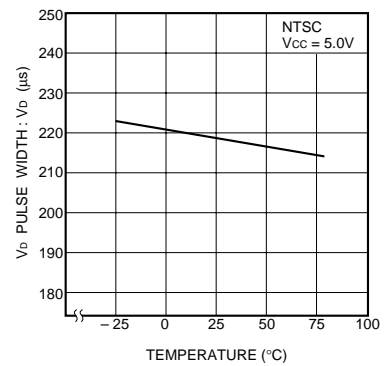


Fig. 16 Vd pulse width vs. temperature

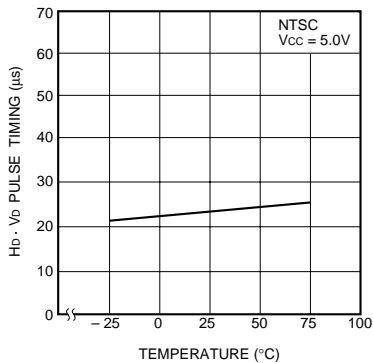


Fig. 17 Hd, Vd phase difference vs. temperature

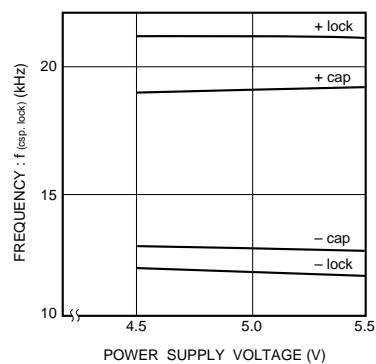


Fig. 18 Capture range / lock range vs. power supply voltage

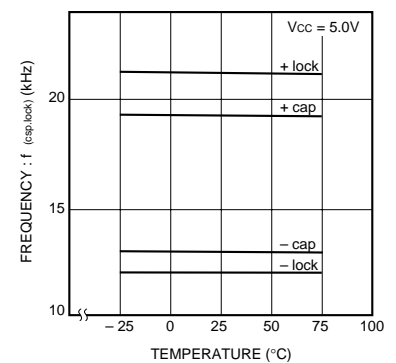


Fig. 19 Capture range charging / lock range vs. temperature

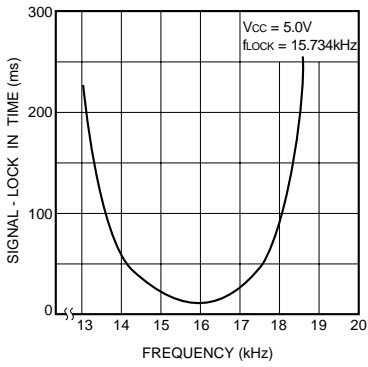


Fig. 20 Time from no signal to pull in

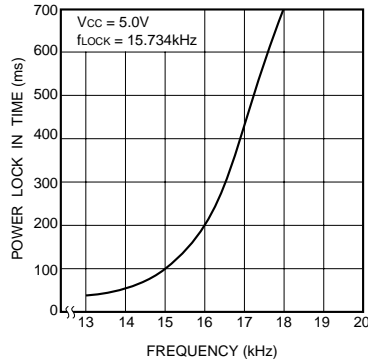


Fig. 21 Time from power on to pull in

●Operation notes

- Make the ground line as thick as possible.
- Keep power supply noise to a minimum.

●External dimensions (Units: mm)

