

LED DISPLAY SPECIFICATION

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VERSION: 1.0

● COMMODITY: .56"(14.20mm) DRIVER IC THREE DIGIT LED DISPLAY

● DEVICE NUMBER: BT-M512RD-DR1

SHEET DATE	1	2	3	4	5	6	7		CONTENTS
2002.08.21	-	1.2	1.0	1.0	1.0	1.0	1.0		Original Release
2003.04.03	1.0	1.3	1.0	1.0	1.0	1.0	1.0		Add page 1 & Edit pin connection

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APPROVED	DRAWER
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LED DISPLAY SPECIFICATION

●COMMODITY: 0.56"(14.20mm) THREE DIGIT LED DISPLAY

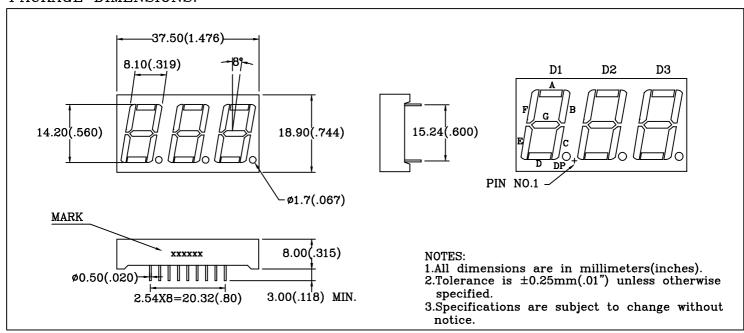
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ELECTRICAL AND OPTICAL CHARACTERISTICS (Ta=25°C)

Chij	p	Absolute Maximum Electro-optical								
	Peak		Rat	ing		Da	ıta (At 10)mA)	Surface	Segment
Emitted Color	Wave Length	Δλ	Pd	If	Peak	Vf	(V)	Іч Тур.	Color	Color
	λP(nm)	(nm)	(mW)	(mA)	If(mA)	Тур.	Max.	(mcd)		
Green	568	30	80	30	150	2.1	2.5	3.0	Black	White

lacktriangle ABSOLUTE MAXIMUM RATINGS (Ta=25 $^{\circ}$ C)



PIN CONNECTION

PIN NO.	Description	PIN NO.	Description
1	VSS	10	Bit 31 Output
2	V led	11	Bit 32 Output
3	V led	12	Bit 33 Output
4	Bit 25 Output	13	Bit 34 Output
5	Bit 26 Output	14	Data Enable
6	Bit 27 Output	15	Data Input
7	Bit 28 Output	16	Clock Input
8	Bit 29 Output	17	Vdd
9	Bit 30 Output	18	BRT Control

Note: Pin no.2 &3 are internally connected

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Table I Serial Data Input Sequence

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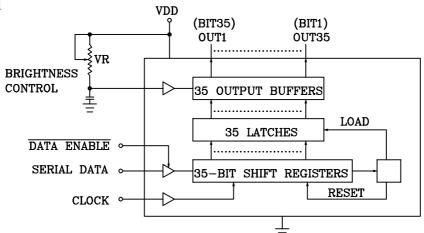
Bit	Digit	Segment	Bit	Digit	Segment
1	1	A	18	3	В
2	1	В	19	3	С
3	1	С	20	3	D
4	1	D	21	3	E
5	1	Е	22	3	F
6	1	F	23	3	G
7	1	G	24	3	D.P.
8	1	D.P.	25		Pin4
9	2	A	26		Pin5
10	2	В	27		Pin6
11	2	С	28		Pin7
12	2	D	29		Pin8
13	2	Е	30		Pin9
14	2	F	31		Pin10
15	2	G	32		Pin11
16	2	D.P.	33		Pin12
17	3	A	34		Pin13

FEATURES

- * CMOS TECHNOLOGY
- * CONTINUOUS BRIGHTNESS CONTROL
- * SERIAL DATA INPUT
- * NO LOAD SIGNAL REQUIRED
- * OPTIONAL EXTERNAL DATA ENABLE AND RESET
- * WIDE POWER SUPPLY OPERATION (3.5V TO 10V)
- * TTL COMPATIBILITY
- * 34 OR 35 OUTPUTS, 20mA SINK CAPABILITY
- *ALPHANUMERIC CAPABILITY

PAD NAME	TYPE	DESCRIPTION
VDD	POWER	POWER
VSS	GROUND	GROUND
RESET	INPUT	RESET SIGNAL INPUT, (NORMALLY LO; ACTIVE HI)
B.C.	INPUT	DC CURRENT INPUT FOR LED BRIGHTNESS CONTROL
CLK	INPUT	CLOCK INPUT
DATA IN	INPUT	SERIAL DATA INPUT
ENB	INPUT	DATA INPUT ENABLES, (NORMALLY LO; ACTIVE LO)
OUT1~OUT35	OUTPUT	NMOS OUTPUT DRIVERS

BLOCK DIAGRAM



35-BIT LED DISPLAY DRIVER

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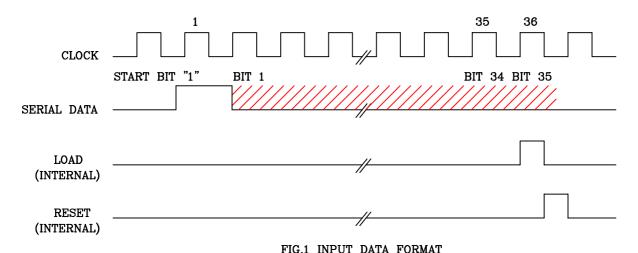
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FUNCTIONAL DESCRIPTION

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1.DATA IS TRANSFERRED SERIALLY VIA 2 SIGNALS: CLOCK AND SERIAL DATA.DATA TRANSFER WITHOUT THE ADDED INCONVENIENCE OF AN EXTERNAL LOAD SIGNAL IS ACCOMPLISHED BY USING A FORMAT OF ALEADING "1" FOLLOWED BY THE ALLOWED 35 DATA BITS.THESE 35 DATA BITS ARE LATCHED AFTER THE 36TH HAS BEEN TRANSFERRED.THIS SCHEME PROVIDES NON-MULTIPLEXED, DIRECT DRIVE TO THE LED DISPLAY.CHARACT3ERS CURRENTLY DISPLAYED (THUS, DATA OUTPUT) CHANGES ONLY IF THE SERIAL DATA BITS DIFFER FROM THOSE PREVIOUSLY TRANSFERREN.

- 2.DISPLAY BRIGHTNESS IS DETERMINED BY CONTROL OF THE OUTPUT CURRENT FOR LED
 DISPLAYS.THIS CONTROL FUNCTION CAN BE ACHIEVED BY VARYING THE CURRENT INTO
 B.C.TERMINAL. A SIMPLE WAY IS TO SET AN EXTERNAL VARIABLE RESIJSTOR ILLUSTRATED IN THE
 BLOCK DIAGRAM. TYPICALLY, THE OUTPUT CURRENT IS 36 TIMES GREATER THAT CURRENT INTO B.C.
 TERMINAL.
- 3.FIGURE 1 SHOWS THE INPUT DATA FORMAT. A LEADING "1" IS FOLLOWED BY 35 BITS OF DATA. AFTER THE 36TH HAD BEEN TRANSFERRED, A LOAD SIGNAL IS GENERATED SYNCHRONOUSLY WITH THE CLOCK HIGH STATE. THIS LOADS THE 35 BITS OF DATA INTO THE LATCHES. [A RESET SIGNAL IS GENERATED CONSECUTIVELY WITH THE CLOCK LOW WHICH CLEARS ALL SHIFT REGISTERS FOR THE NEXT SEDT OF DATA] ALL SHIFT REGISTERS ARE STATIC MASTER-SLAVE, WITH NO CLEAR FOR THE MASTER PORTION OF THE FIRST REGISTER, ALL OWING CONTINUOUS OPERATION [THERE MUST BE A COMPLETE OF 36 CLOCKS OR THE SHIFT REGISTERS WILL NOT CLEAR.]
- 4.WHEN THE CHIP FIRST POWERS ON AN INTERNAL POWER ON RESET SIGNAL IS GENERATED WHICH RESETS ALL SHIFT REGISTERS AND ALL LATCHES. THE START BIT AND THE FIRST CLOCK RETURN THE CHIP TO ITS NORMAL OPERATION.



35-BIT LED DISPLAY DRIVER

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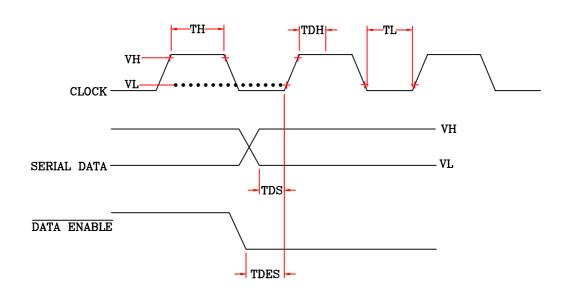
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ABSOLUTE MAXIMUM RATINGS, Ta=25°C (UNLESS OTHERWISE SPECIFIED)

CHARACTERISTICS	SYMBOL	RATING	UNIT
SUPPLY VOLTAGE	VDD	+3.5~+10	V
CLOCK FREQUENCY	Fosc	500K	Hz
INPUT VOLTAGE	$V_{ m IN}$	-0.3~VDD+0.3	V
INPUT B.C. CURRENT	I_{BC}	550	μΑ
OUTPUT SUSTAINING VOLTAGE	$ m V_{DS}$	12	V
OUT CONTINUOUS CURRENT	IOUT	20	mA

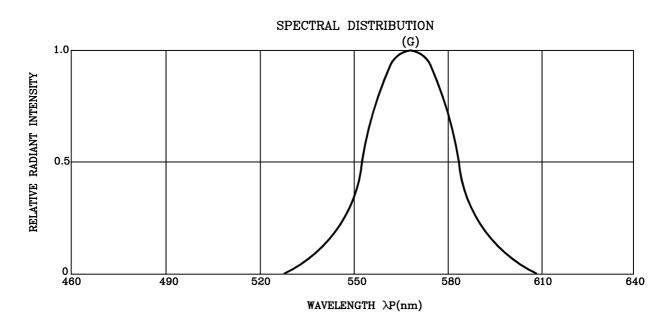
• TIMING CHART & TIMING CONDITIONS

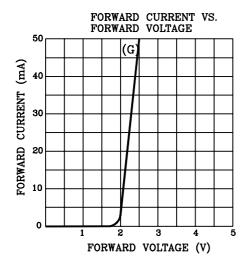


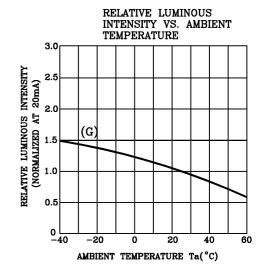
VDD=+5V, Ta=25°C, UNLESS OTHERWISE SPECIFIED						
ITEM	DESCRIPTION	MIN	TYP	MAX	UNTI	
TH	CLOCK INPUT HIGH TIME	950	-	-	nS	
TL	CLOCK INPUT LOW TIME	950	-	-	nS	
TDS	SERIAL DATA SET-UP TIME	300	-	-	nS	
TDH	SERIAL DATA HOLD TIME	300	-	-	nS	
TDES	DATA ENABLE SET-UP TIME	100	-	-	nS	

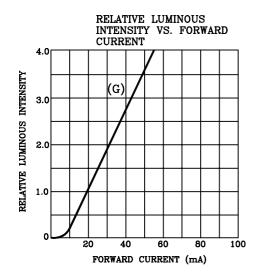
TYPICAL CHARACTERISTICS

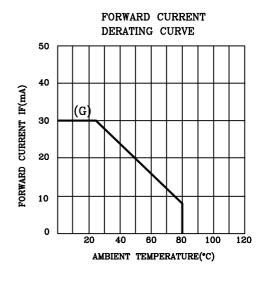
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RELIABILITY TEST

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DEVICE NO.: BT-M512RD-DR1

Classification	Test Item	Reference Standard	Test Conditions	Result
	Operation Life	MIL-STD-750:1026 MIL-STD-883:1005 JIS C 7021 :B-1	Connect with a power If=30mA Ta=Under room temperature Test time=1,000hrs(-24hrs,+72hrs)	0/10
Endurance	High Temperature High Humidity Storage	MIL-STD-202:103B JIS C 7021 :B-11	Ta=65°C ±5°C RH=90%-95% Test time=240hrs±2hrs	0/10
Test	High Temperature Storage	MIL-STD-883:1008 JIS C 7021 :B-10	High Ta=85°C ±5°C Test time=1,000hrs(-24hrs,+72hrs)	0/10
	Low Temperature Storage	JIS-C-7021 :B-12	Low Ta= -35°C ±5°C Test time=1,000hrs(-24hrs,+72hrs)	0/10
	Temperature Cycling	MIL-STD-202:107D MIL-STD-750:1051 MIL-STD-883:1010 JIS C 7021 :A-4	-35°C ~25°C ~85°C ~25°C 30min 5min 30min 5min Test Time=10cycle	0/10
Environmental	Thermal Shock	MIL-STD-202:107D MIL-STD-750:1051 MIL-STD-883:1011	85° C $\pm 5^{\circ}$ C $\sim -35^{\circ}$ C $\pm 5^{\circ}$ C 10min 10 min Test Time= 10 cycle	0/10
Test	Solder Resistance	MIL-STD-202:201A MIL-STD-750:2031 JIS C 7021 :A-1	T.sol= 260 ± 5 °C Dwell Time= 10 ± 1 sec.	0/10
	Solderability	MIL-STD-202:208D MIL-STD-750:2026 MIL-STD-883:2003 JIS C 7021 :A-2	T.sol= 230 ± 5 °C Dwell Time= 5 ± 1 sec.	0/10

JUDGMENT CRITERIA OF FAILURE FOR THE RELIABILITY

Measuring items	Symbol	Measuring conditions	Judgement criteria for failure
Forward voltage	VF	IF=10mA	Over Ux1.2
Reverse current	IR	VR=5V	Over Ux2
Luminous intensity	IV	IF=10mA	Below Sx0.5

Note: 1.U means the upper limit of specified characteristics. S means initial value.

2.Measurment shall be taken between 2 hours and after the test pieces have been returned to normal ambient conditions after completion of each test.