

# CAT6500

## 3.0 A Power Selector Switch

### Description

CAT6500 is an automatic power switch designed to select between two power sources and direct that power to a load for battery charging or system power.

CAT6500's power inputs withstand voltages of up to 18 V and protect the downstream load from voltages exceeding 7 V. In the event of a polarity reversal at either input CAT6500's internal power switches will shut off to prevent discharge of the system's internal power source.

Low resistance power switches handle currents in excess of 3 A and when OFF block current flow in both directions. CAT6500 can operate in reverse mode in which internal system power is be directed to either of the power input ports for powering an external device, such as a USB On-The-Go appliance.

### Features

- Autonomous Switching between 2 Power Sources
- Withstands +18 V to -5 V on Either Power Input
- 80 mΩ Switches (typ.) for Low Power Loss
- Reverse-Mode for Powering External Devices
- Over Voltage Protection of Downstream Load
- Compatible with USB-OTG Devices
- 32-Lead WQFN 4.4 mm x 4.4 mm Package
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Typical Applications

- Mobile Phones
- PDAs
- Personal Navigation Devices

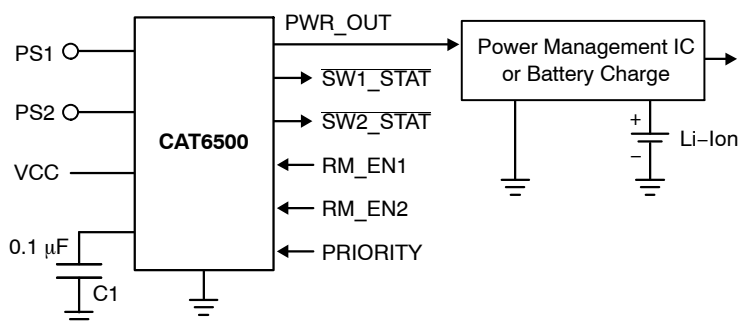
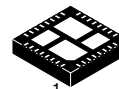


Figure 1. Typical Application Circuit



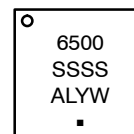
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WQFN-32  
HVA SUFFIX  
CASE 485BN

### MARKING DIAGRAM



- 6500 = Specific Device Code
- SSSS = Last Four Digits of Assembly Lot Number
- A = Assembly Location
- L = Wafer Lot Number (optional)
- Y = Production Year
- W = Production Week
- = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
CAT6500HVA-T2	WQFN-32 (Pb-Free)	2,000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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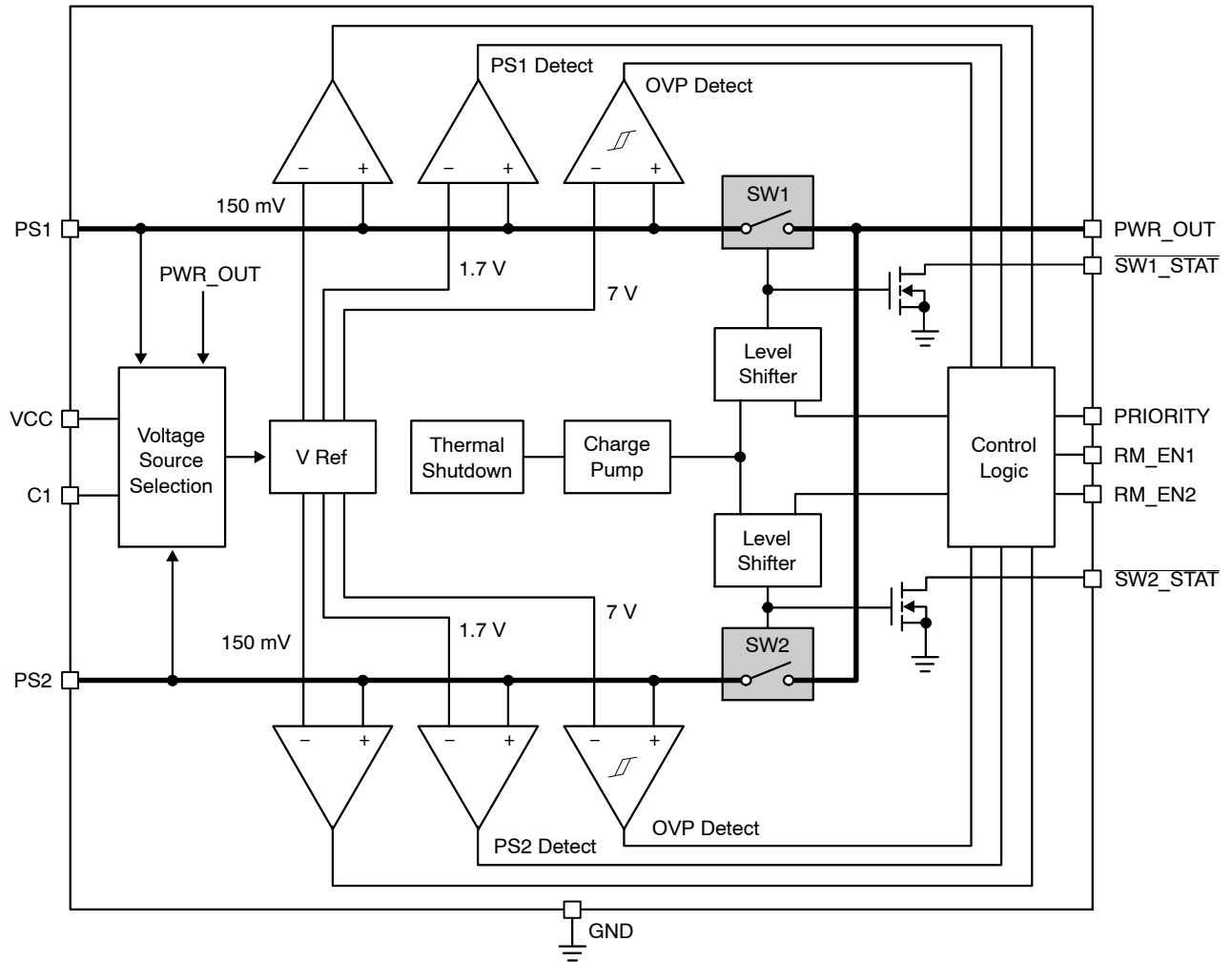


Figure 2. Simplified Block Diagram

## PIN CONNECTIONS

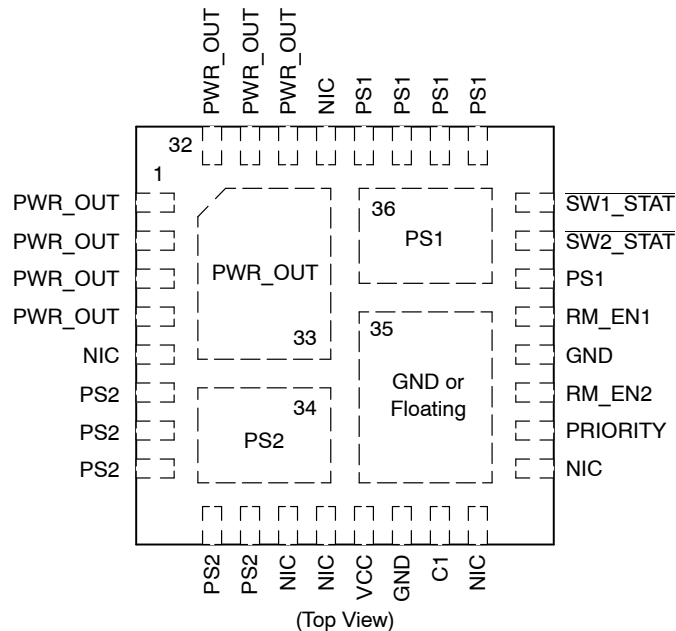


Figure 3. Pin Connections w/Rear Pads Shown

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**Table 1. PIN FUNCTION DESCRIPTION**

Pin No.	Pin Name	Description
1, 2, 3, 4	PWR_OUT	Power Output. Must be tied to PWR_OUT on opposite side of chip. Use all 3 pins each side.
5	NIC	No Internal Connection. A signal or voltage applied to this pin will have no effect on device operation.
6, 7, 8, 9, 10	PS2	Power Source #2. External power input
11, 12	NIC	No Internal Connection. A signal or voltage applied to this pin will have no effect on device operation.
13	VCC	Power input from battery.
14	GND	Ground. Reference point for all voltages.
15	C1	Filter capacitor for CAT6500's internal power bus
16	NIC	No Internal Connection. A signal or voltage applied to this pin will have no effect on device operation.
17	NIC	No Internal Connection. A signal or voltage applied to this pin will have no effect on device operation.
18	PRIORITY	Priority selects preferred power source when both PS1 and PS2 are powered.
19	RM_EN2	Reverse Mode Enable 2. Overrides PRIORITY and turns SW2 ON.
20	GND	Ground. Reference point for all voltages.
21	RM_EN1	Reverse Mode Enable 1. Overrides PRIORITY and turns SW1 ON.
22	PS1	Power Source #1. External power input.
23	SW2_STAT	Power Source 2 Status. An open drain LOW true logic level output indicating that the switch SW2 is turned on.
24	SW1_STAT	Power Source 1 Status. An open drain LOW true logic level output indicating that the switch SW1 is turned on.
25, 26, 27, 28	PS1	Power Source #1. External power input.
29	NIC	No Internal Connection. A signal or voltage applied to this pin will have no effect on device operation.
30, 31, 32	PWR_OUT	Power Output. Must be tied to PWR_OUT on opposite side of chip. Use all 3 pins each side.
33	PWR_OUT	Electrically active thermal pad. Does not need to be connected to other PWR_OUTs. Can be left floating but must not be connected to other signal paths or Ground.
34	PS2	Electrically active thermal pad. Does not need to be connected to other PS2 pins. Can be left floating but must not be connected to other signal paths or Ground.
35	—	Mechanical support for control IC. This chip does not generate any significant heat and does not need a separate heat sinking connection. Electrically this may be left floating or can be grounded. It should NOT be connected to other signals or voltages.
36	PS1	Electrically active thermal pad. Does not need to be connected to other PS1 pins. Can be left floating but must not be connected to other signal paths or Ground.

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**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Pin	Range	Unit
Input Voltage Range (Note 1)	$V_{PS}$	PS1, PS2	-5.0 to 18	V
	$V_{CC}$ , $V_{PWR\_OUT}$	VCC, C1, PWR_OUT	-0.3 to 6.0	
Control Logic Input Range	$V_{L\_IN}$	RM_ENx, PRIORITY	-0.3 to 6.0	V
Control Logic Output Range	$V_{L\_OUT}$	SW1_STAT, SW2_STAT	-0.3 to 6.0	V
Maximum Junction Temperature	$T_{J(max)}$	-	150	°C
Storage Temperature Range	$T_{STG}$	-	-65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD <sub>HBM</sub>	ALL	2	kV
ESD Capability, Machine Model (Note 2)	ESD <sub>MM</sub>	ALL	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)	$T_{SLD}$	ALL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)  
 Latchup Current Maximum Rating:  $\leq 150$  mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

**Table 3. THERMAL CHARACTERISTICS** (Note 4)

Parameter	Symbol	Value	Unit
Thermal Characteristics, TDFN-32 4.4 x 4.4 mm Thermal Resistance, Junction-to-Air, 1 sq. Inch, 1 oz. Copper Clad PCB Thermal Resistance, Junction-to-Air, 1 sq. Inch, 2 oz. Copper Clad PCB	$R_{\theta JA}$	59 54	°C/W

4. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Input Voltage PS1, PS2	$V_{CC}$	1.6	5.5	V
	$V_{PWR\_OUT}$	0	5.5	
	$V_{PS1}$ , $V_{PS2}$	-5	7.7	
Output Current	$I_{PWR\_OUT}$	0	3.3	A
Control Logic; Inputs and Outputs	$V_{L\_IN}$ , $V_{L\_OUT}$	0	5.5	V
Ambient Temperature	$T_A$	-40	+85	°C

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**Table 5. ELECTRICAL OPERATING CHARACTERISTICS**

( $V_{CC} = 3.9\text{ V}$ ,  $C1 = 0.1\ \mu\text{F}$ , unless otherwise noted. Typical values  $T_A = 25^\circ\text{C}$ , Min/Max values  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>INPUT / OUTPUT</b>						
Input Voltage	PS1 or PS2 normal operation mode	$V_{PS}$	1.6	3.9	7.7	V
	PS1 or PS2 overvoltage protection mode	$V_{PS}$	1.6	3.9	12	
	VCC	$V_{CC}$	2.5	3.9	5.5	
Operating Current; SW1 and SW2 ON	Measured at VCC RM_EN1 = 1, RM_EN2 = 1 1.7 V < PS1 < 2.4 V, 1.7 V < PS2 < 2.4 V	$I_{VCC}$	–	85	120	$\mu\text{A}$
Quiescent Current; SW1 and SW2 OFF	Measured at VCC PRIORITY = 1, RM_EN1 = 0, RM_EN2 = 0 PS1 < 1.5 V, PS2 < 1.5 V	$I_{VCC}$	–	35	45	$\mu\text{A}$
Input Voltage Detect	PS1, PS2, voltage rising	$V_{DETR}$	1.6	1.7	1.8	V
	PS1, PS2, voltage falling	$V_{DETF}$	0.1	0.15	0.3	
Over Voltage Detection	PS1, PS2, voltage rising	$V_{OVP}$	6.5	7.0	7.8	V
Over Voltage Hysteresis	PS1, PS2, voltage falling	$V_{HYS}$	100	–	250	mV
Reverse Voltage Detect Threshold	PS1, PS2	$V_{REV}$	–0.7	–	–1.0	V
<b>POWER SWITCHES</b>						
Switch Resistance; SW1, SW2	Measured from PSx to PWR_OUT PS1 or PS2 = 2.5 V, 5°C	$R_{ON}$	–	80	110	m $\Omega$
	PS1 or PS2 = 5 V, 25°C		–	–	–	
	PS1 or PS2 = 5 V, –40°C to +85°C		–	–	135	
<b>LOGIC</b>						
Input Threshold Voltage	Voltage Increasing, Logic High PRIORITY, RM_EN1, RM_EN2	$V_{th\_HIGH}$	1.0	–	1.5	V
	Voltage Decreasing, Logic Low PRIORITY, RM_EN1, RM_EN2	$V_{th\_LOW}$	0.4	–	0.8	
Input Current	PRIORITY, Pull-Up	$I_{IN}$	–	10	20	$\mu\text{A}$
	RM_ENx, Pull-Down		–	10	20	
Output Current HIGH	$V_{OH} = V_{IN} - 0.3\text{ V}$ SW1_STAT, SW2_STAT	$I_{OH}$	–	10	15	$\mu\text{A}$
Output Voltage LOW	$I_{OL} = 3.0\text{ mA}$ SW1_STAT, SW2_STAT	$V_{OL}$	–	0.3	0.4	V
<b>TIMING</b>						
SW Turn-on Delay Time	Measured from rising edge of RM_ENx to 10% of voltage at PSx; PSx = 2.0 V	$t_{ON\_DLY}$	–	100	–	$\mu\text{s}$
SW Rise Time	Measured at PWR_OUT 10% to 90% of voltage applied at PSx PS = 2.0 V	$t_{RISE}$	–	200	300	$\mu\text{s}$
	Measured at PWR_OUT 10% to 90% of voltage applied at PSx PS = 5 V		–	100	250	
SW Turn-off Time	Measured at PWR_OUT 90% to 10% of voltage applied at PSx	$t_{OFF}$	–	–	25	$\mu\text{s}$
Over Voltage Turn-off Time	PS = 0 V → 10 V	$t_{OFF\_OV1}$	–	10	–	$\mu\text{s}$
	PS = 5 V → 10 V	$t_{OFF\_OV2}$	–	10	–	
Break-Before-Make Off Time	Measured at PWR_OUT, OFF time during transition from PS1 → PS2 or PS2 → PS1	$t_{OFF\_BBM}$	–	400	–	$\mu\text{s}$
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown Temperature		$T_{SD}$	–	145	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis		$T_{SH}$	–	10	–	$^\circ\text{C}$

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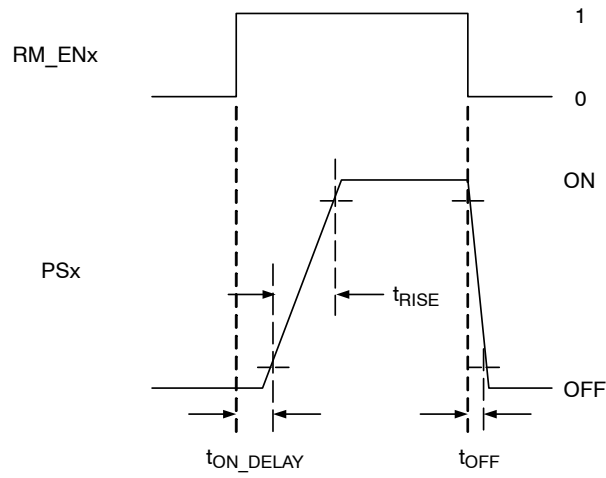


Figure 4. Switch Timing

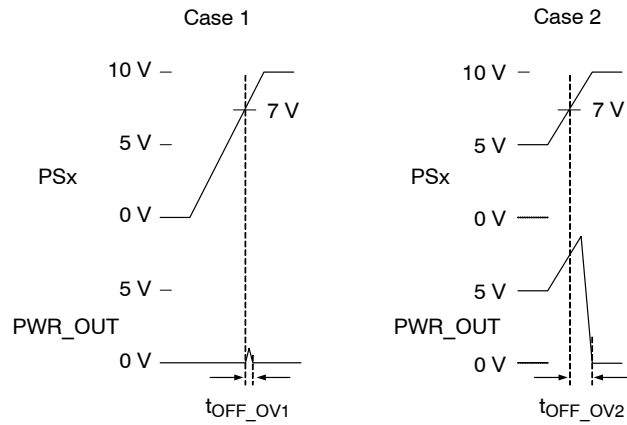


Figure 5. Overvoltage Turn-Off Timing

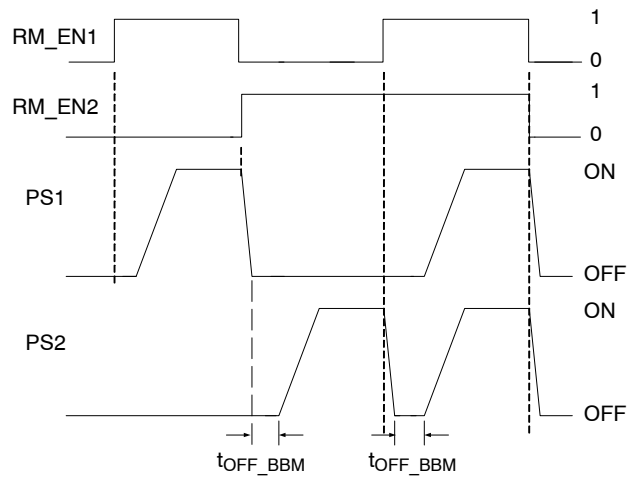


Figure 6. Break-Before-Make Switching

TYPICAL PERFORMANCE CHARACTERISTICS

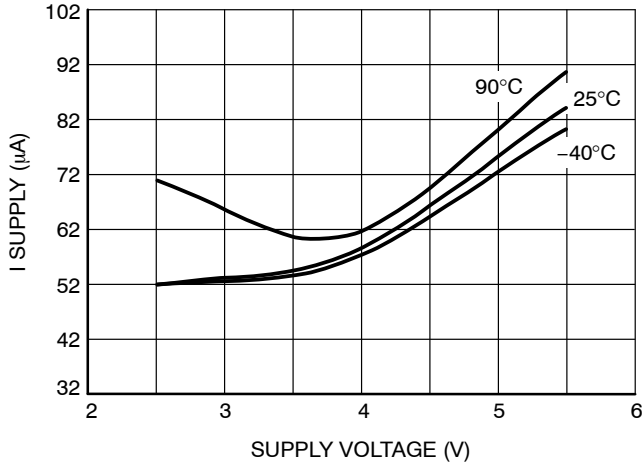


Figure 7. Operating Supply Current vs. VCC

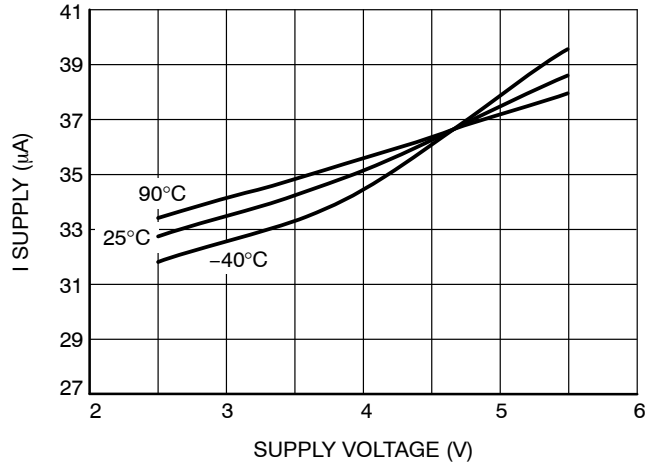


Figure 8. Quiescent Supply Current vs. VCC

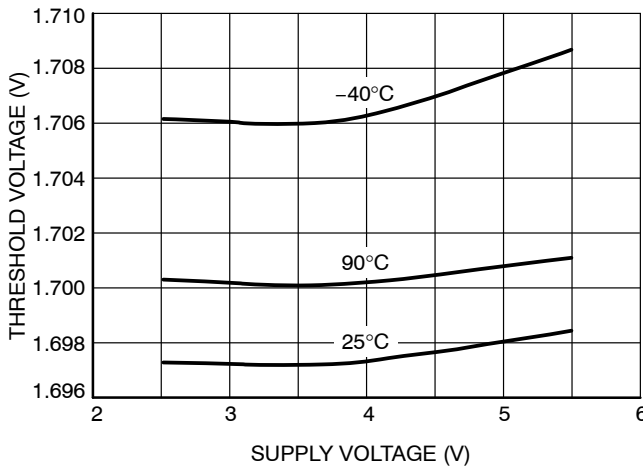


Figure 9. PS\_Detect Threshold vs. VCC

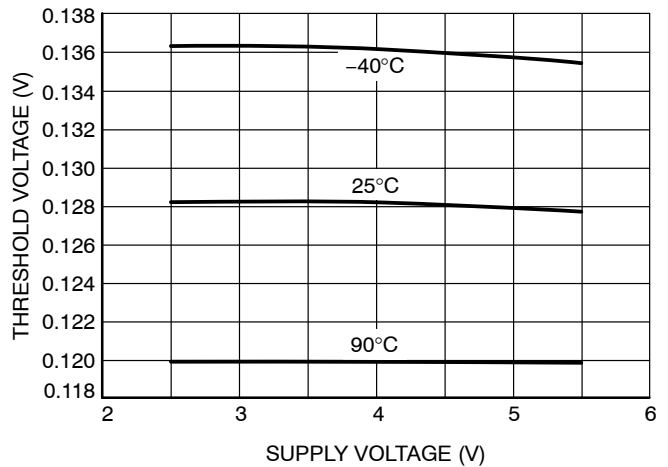


Figure 10. PS\_Release Threshold vs. VCC

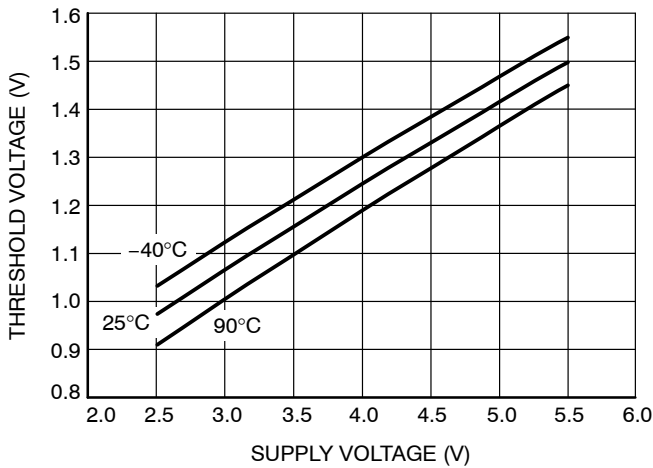


Figure 11. Vth\_HIGH vs. VCC

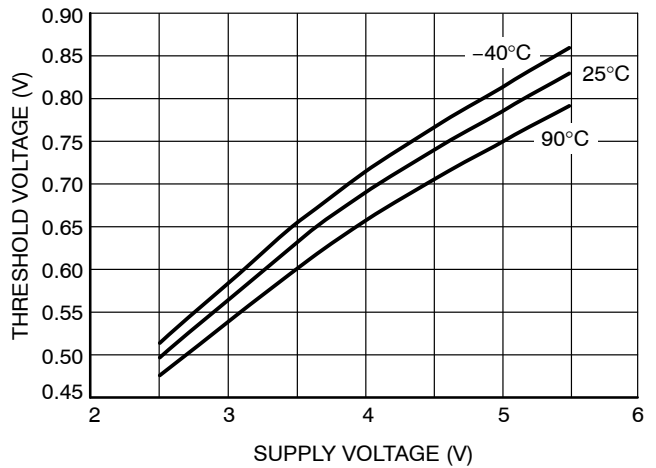


Figure 12. Vth\_LOW vs. VCC

TYPICAL PERFORMANCE CHARACTERISTICS

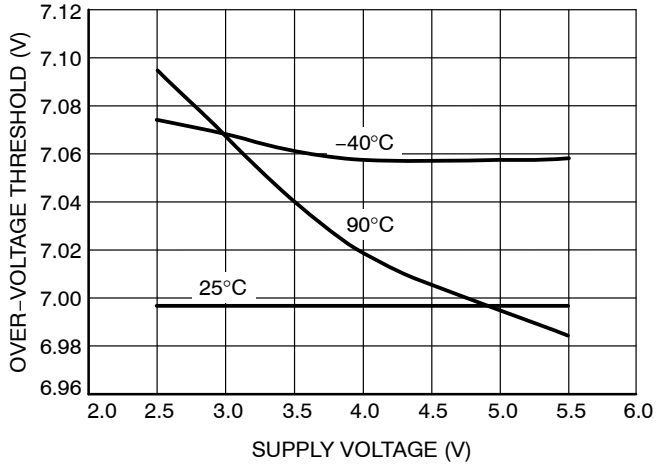


Figure 13. Over-Voltage Threshold vs. VCC

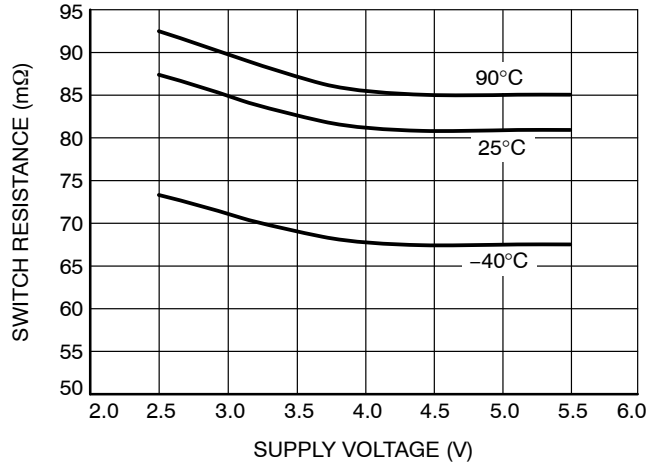


Figure 14. Switch  $R_{ON}$  vs. VCC

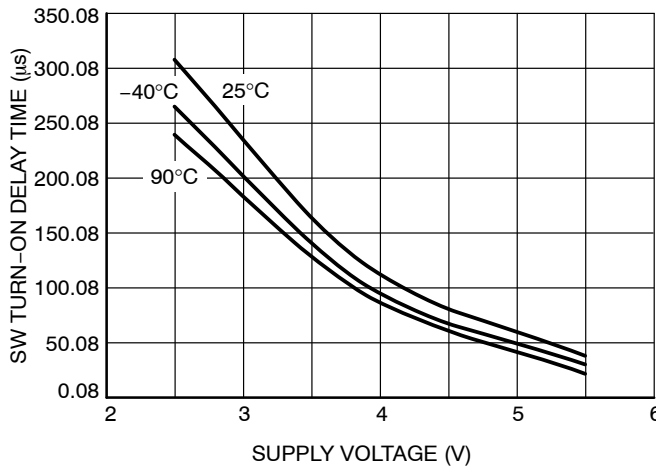


Figure 15.  $t_{ON\_DLY}$  vs. VCC

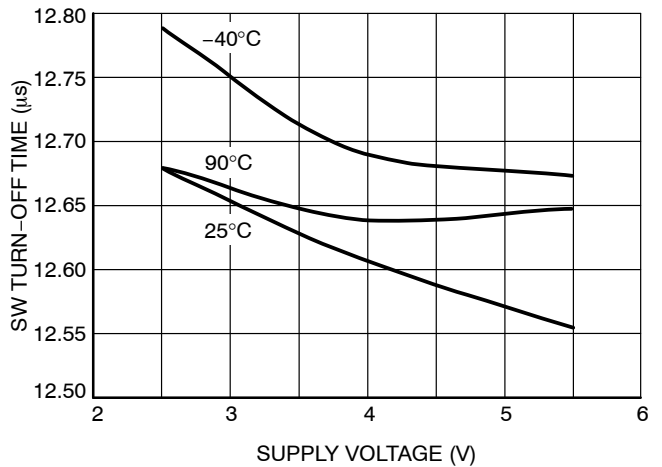


Figure 16.  $t_{OFF}$  vs. VCC

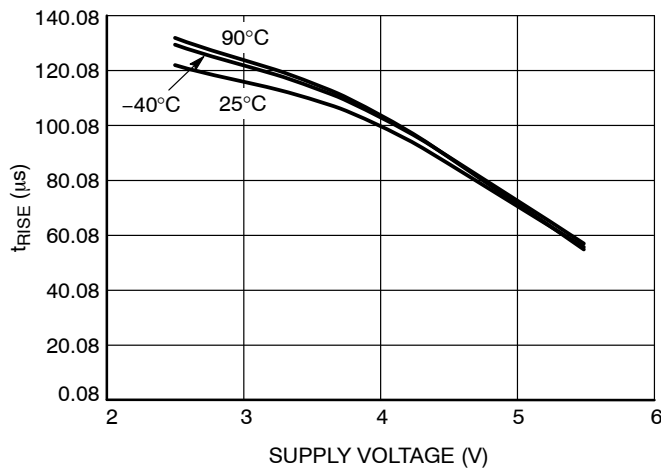


Figure 17.  $t_{RISE}$  vs. VCC



# CAT6500

## PIN FUNCTIONS

### SW1, SW2

SW1 and SW2 are low ON resistance power FET switches within CAT6500 and form the power transfer path between PS1, PS2 and PWR\_OUT. SW1 and SW2 are bidirectional allowing for current to flow in either direction. They are controlled by the digital inputs PRIORITY, RM\_EN1, RM\_EN2. While they are not device pins they are defined here in order to make pin functions more understandable.

### PS1, PS2

These are input pins for two external power sources which supply power for battery charging and system operation. On the basis of a PRIORITY input, CAT6500 will select from PS1 or PS2 and route power to PWR\_OUT. If power on the preferred input is unavailable or the voltage is insufficient and a suitable power source is available on the other power input then CAT6500 will use the alternate source.

PS1 and PS2 can also supply power to external devices if a reverse-mode command is given. In reverse-mode, PWR\_OUT becomes the power source and is connected to either PS1 or PS2 in accord with the reverse-mode command. It is possible for both PS1 and PS2 to be powered simultaneously by PWR\_OUT if commanded by the reverse-mode inputs. This dual command state also allows for power transfer between PS1 and PS2.

### PWR\_OUT

PWR\_OUT is the common point between SW1 and SW2 and conducts power from either of these inputs to the system's power bus.

When used in reverse mode PWR\_OUT can supply power to an external load such as a USB device attached to PS1 or PS2.

### RM\_EN1, RM\_EN2

Reverse mode enable inputs are logic high signals which will override autonomous voltage source selection and force either SW1 or SW2 into an ON state. RM\_EN1 and RM\_EN2 act independently of each other and therefore can both be active at the same time.

### VCC

VCC is an alternative power source for CAT6500 in the event neither PS1 nor PS2 is powered or if CAT6500 is in reverse-mode and is supplying power to an external device. VCC supplies only CAT6500's internal control logic circuitry and is never routed to PS1, PS2 or PWR\_OUT.

### C1

CAT6500 can draw its operating current from several different inputs and will switch between these sources as they change or become available. To keep the chip's internal supply voltage stable during these transitions an external filter capacitor is required. The recommended value for C1 is between 0.1  $\mu$ F and 1.0  $\mu$ F.

### GND

The negative power input pin for CAT6500 and system ground.

### PRIORITY

PRIORITY is a logic signal input that directs power source selection in forward mode if both PS1 & PS2 sources of power are present at the same time. For PRIORITY low, PS1 is selected. If only one source of power is present, CAT6500 will default to that source.

PRIORITY can be overridden by a RM\_ENx command in which case the associated power FET SW1 or SW2 is turned ON by the RM\_EN command.

### SW1\_STAT, SW2\_STAT

$\overline{\text{SW1\_STAT}}$  and  $\overline{\text{SW2\_STAT}}$  are open drain LOW true digital outputs indicating the operating state of Power Switch 1 (SW1) and Power Switch 2 (SW2), where a LOW indicates the switch is ON.  $\overline{\text{SW1\_STAT}}$  and  $\overline{\text{SW2\_STAT}}$  may be pulled up to an external voltage greater than VCC or greater than PSx as long as it does not exceed 5.5 V.

$\overline{\text{SW1\_STAT}}$  and  $\overline{\text{SW2\_STAT}}$  are active in reverse-mode and continue to indicate the operational status of SW1 and SW2.

CIRCUIT DESCRIPTION AND OPERATING CONSIDERATIONS

**Description**

CAT6500 is an autonomous power selector switch designed for portable device applications where either of two power sources may be used for battery charging and device operation. CAT6500 can operate in two distinct modes, forward or reverse, depending on the states of the RM\_ENx inputs.

In forward mode, CAT6500 will automatically select from the available power sources, PS1 or PS2, and direct one to PWR\_OUT.

In reverse mode, a system power rail connected to PWR\_OUT can source power to an external device attached to either PS1 or PS2. This allows charging or powering of other portable devices.

**Power Source Selection**

In forward mode, on-chip voltage detection circuitry senses the presence of a suitable power source at power inputs, PS1 and PS2. If both inputs are powered the PRIORITY pin sets the preferred power source directs that source to PWR\_OUT. If only one of the two inputs is powered then that power source is directed to PWR\_OUT.

CAT6500 provides two status outputs SWx\_STAT to indicate the presence of a voltage at either PS1 or PS2. These status outputs trigger at 1.7 V and are LOW true digital outputs.

PRIORITY has an internal pull-up and defaults to a logic HIGH if the pin is disconnected or left floating. Input selection follows the truth table in Table 6.

CAT6500 draws its operating power from PS1 or PS2 when a voltage of 2.5 V or more is present. If no power is present at PS1 or PS2 or CAT6500 is in reverse mode, power will be drawn from VCC.

CAT6500 provides overvoltage protection to circuitry downstream from the chip by limiting input voltages to 7 V. Should the voltage at PS1 or PS2 rise above 7 V then PWR\_OUT will be disconnected from the power source until the voltage returns to safe levels.

CAT6500 provides similar protection for reverse polarity voltages down to -5 V.

**Reverse Mode Operation**

The RM\_ENx inputs allow CAT6500 to operate the power switches in reverse mode where the PWR\_OUT becomes the supply powering PS1 and/or PS2. When RM\_EN1 is logic high, SW1 switch is turned on and PWR\_OUT is connected to PS1. When RM\_EN2 is logic high, SW2 switch is turned on and PWR\_OUT is connected to PS2. The switch connection remains on until the PWR\_OUT voltage decreases all the way to 0 V (below 0.1 V typical) regardless of the state of the associated RM\_ENx input.

RM\_EN is not affected by the voltage levels seen at PS1 or PS2 as PRIORITY and will not switch OFF automatically

if the voltage drops below 1.7 V as would CAT6500 otherwise do. This allows the power connection to be used for signaling purposes as in USB On-The-Go where power line signaling is used to request a transfer of bus Master status between devices. When operating in reverse mode, the SW1\_STAT and SW2\_STAT outputs are still active and will reflect the switch conditions.

RM\_EN1 and RM\_EN2 are independent controls and can be activated simultaneously, meaning both SW1 and SW2 can be conducting at the same time. This presents both opportunities and hazards.

Having both switches ON allows for simultaneous charging or powering of two devices from a single source; a USB power source can charge and operate the device as well as power an additional unit connected to the other PS input. Or the device can power two external units attached to PS1 and PS2.

The downside of this capability becomes apparent when two operating power sources are present at the same time. If both switches are ON the power sources will compete with the stronger driving the weaker. For example; if a wall charger is attached to PS1 and an active USB port to PS2, with both SW1 and SW2 ON, the wall charger will likely dominate and push power backwards into the USB port, possibly elevating the USB bus voltage above allowable limits.

Note: SW1 and SW2 are not current limited and can conduct very high currents if short circuited. Current limiting circuitry is advisable if short circuits are possible in the intended application.

**Entering and Exiting Reverse Mode**

When entering or exiting Reverse Mode, it is recommended that power applied to PWR\_OUT be sequenced with the enabling/disabling signal. It is best to enter Reverse Mode with PWR\_OUT at 0 V and apply power after the logic control. Similarly on exiting Reverse Mode, power should be taken to 0 V and then the switch disabled.

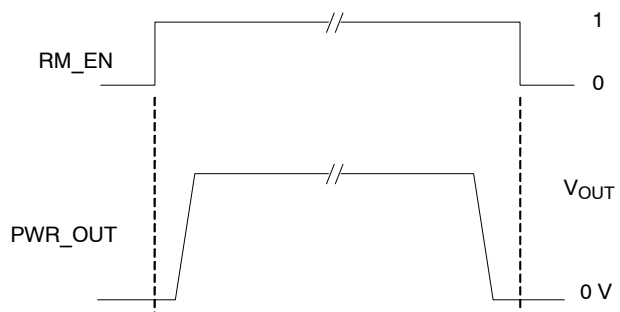


Figure 18. Entering and Exiting Reverse Mode

**Over-Voltage**

CAT6500 is designed to withstand input voltages of up to 18 V on the PS1 or PS2 inputs. In the event of such a fault condition, SW1 or SW2, whichever is exposed to the fault will shut OFF. This fault protection is voltage sensitive, activating at 7 V typically and overrides control inputs PRIORITY, RM\_EN1 and RM\_EN2.

The response time of the over voltage detection circuit is constant and independent of the rise time of the overvoltage event, however the voltage transient seen at PWR\_OUT will vary depending upon the operating conditions at the time of the event. Case 1 and Case 2 of Figure 5 illustrates this. In Case 1, an overvoltage is applied to a PS input as would happen if a malfunctioning or improper charger were used to recharge a handheld appliance. The internal FET switch is initially off and the application of voltage at the PS input

initiates turning it ON, but the delay associated with turning ON the switch is very long compared to the overvoltage comparator’s response time. The resulting voltage transient at PWR\_OUT is very small to non-existent because the FET switch never gets the chance to turn fully ON.

Case 2 assumes voltage is applied to a PS input and the internal FET switch is ON. If for some reason the applied voltage surges above the overvoltage threshold the FET will be turned OFF but a transient will be seen at PWR\_OUT. The degree to which the voltage at PWR\_OUT exceeds the overvoltage threshold depends upon the rate of voltage rise at PS compared to the comparator’s response time.

CAT6500 is tolerant to negative voltages as well and shuts OFF SW1 and SW2 when either PS1 or PS2 goes negative by more than 0.7 V.

**Table 6. POWER SWITCH CONTROL AND SELECTION**

Inputs					Connections		Outputs		
PS1	PS2	RM_EN1	RM_EN2	PRIORITY	SW1	SW2	PWR_OUT	SW1_STAT	SW2_STAT
L	L	0	0	X	0	0	0	1	1
H	L	0	0	0	1	0	PS1	0	1
L	H	0	0		0	1	PS2	1	0
H	H	0	0		1	0	PS1	0	1
H	L	0	0	1	1	0	PS1	0	1
L	H	0	0		0	1	PS2	1	0
H	H	0	0		0	1	PS2	1	0
PWR_OUT	Hi-Z	1	0	X	1	0	X	0	1
Hi-Z	PWR_OUT	0	1		0	1	X	1	0
PWR_OUT	PWR_OUT	1	1		1	1	X	0	0

L ≤ 1.7 V for voltage rising at PS	H ≥ 1.7 V	Default = 0 if left floating	Default = 1 if left floating	0 = Open    1 = Closed
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**Break-Before-Make Switching**

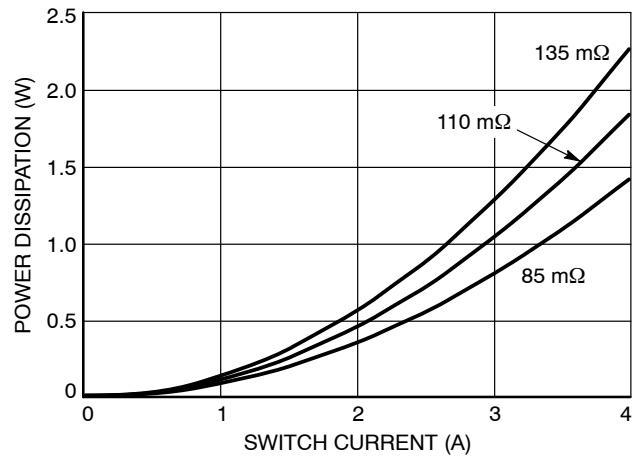
When switching between power sources either under automatic control (PRIORITY) or in override (RM\_EN), CAT6500 disables the active switch before the new connection is made. This ensures there will be no unintended cross conduction between PS1 and PS2. Even when SW1 and SW2 are commanded to be ON simultaneously there is a brief interval when both SW1 and SW2 are OFF. Figure 6 illustrates this.

**Thermal Considerations**

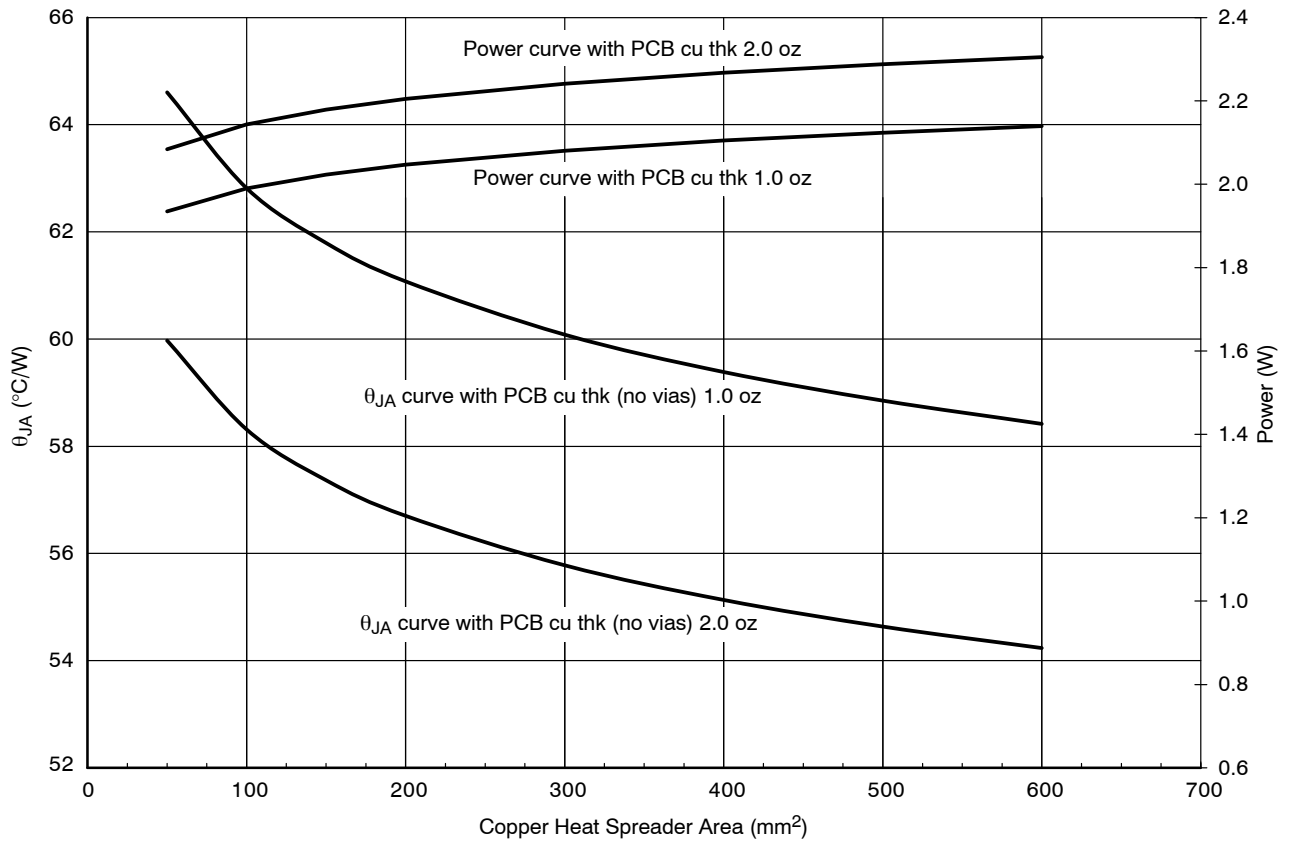
Under normal operating conditions SW1 and SW2 will dissipate some amount of heat which is a function of the current through the switch and RON. Typical heating curves are shown in Figure 19.

CAT6500 is protected against overheating by an internal temperature sensor. Should the chip’s temperature reach 145°C CAT6500 will shut off both power switches until the die temperature drops to below approximately 135°C, at which time the power switches will be returned to their original operating state. If the temperature again exceeds the thermal shutdown limit both switches will be disabled and this cycling will continue until current flowing through the switch is reduced, the load is removed or the switch is turned off under system control.

# CAT6500



**Figure 19. Power Dissipation vs. Switch Current and Resistance**

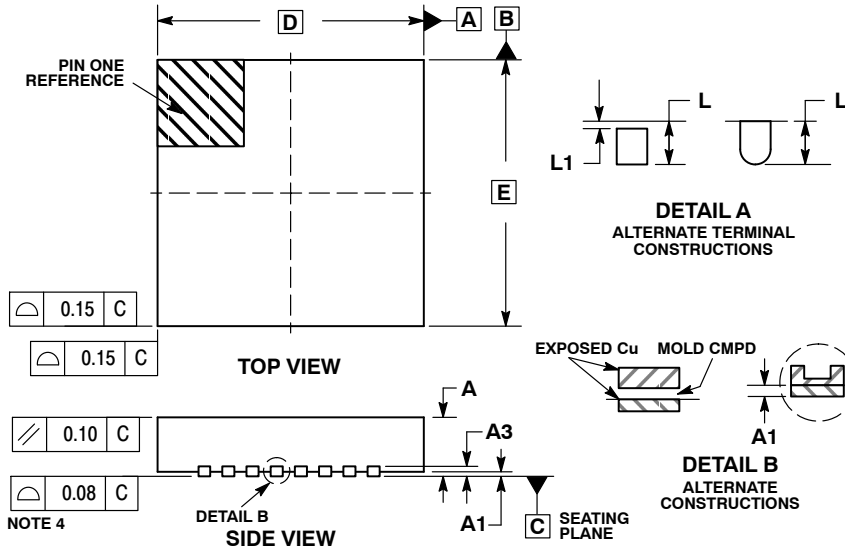


**Figure 20.  $\theta_{JA}$  vs. Copper Heat Spreader Area**

# CAT6500

## PACKAGE DIMENSIONS

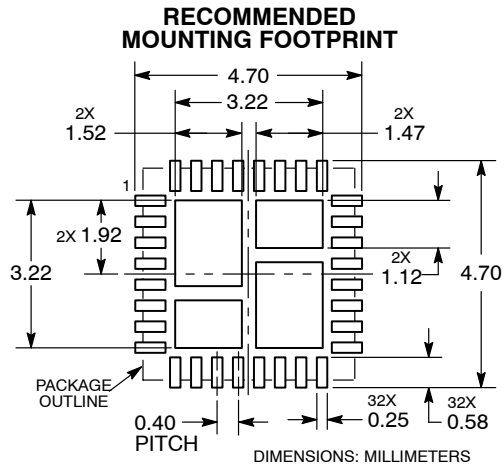
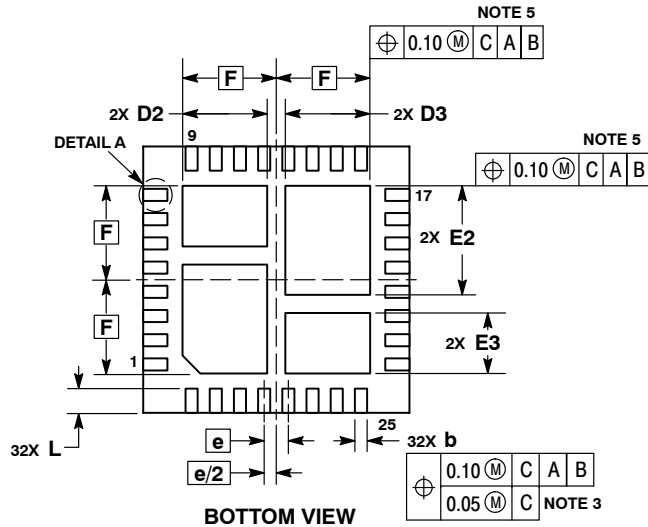
WQFN32 4.4x4.4, 0.4P  
CASE 485BN-01  
ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE EXPOSED PADS.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20	REF
b	0.15	0.25
D	4.40	BSC
D2	1.30	1.50
D3	1.25	1.45
E	4.40	BSC
E2	1.70	1.90
E3	0.90	1.10
e	0.40	BSC
F	1.55	BSC
L	0.30	0.50
L1	0.05	0.15



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