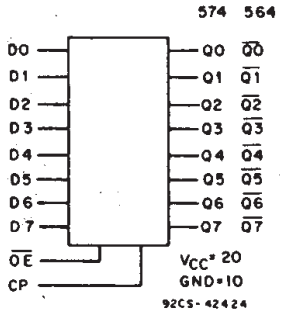
CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS292



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State
Positive-Edge-Triggered

CD54/74AC/ACT564 - Inverting
CD54/74AC/ACT574 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  6.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA-CD54/74AC564 and CD54/74AC574 and the CD54/74ACT564 and CD54/74ACT574 octal D-type, 3-state, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT564 and CD54/74AC/ACT574 share the same pin configurations; the CD54/74AC/ACT564, however, has inverted outputs and the CD54/74AC/ACT574 has non-inverted outputs.

The CD74AC/ACT564 and CD74AC/ACT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT564 and CD54AC/ACT574, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			564	574
$\overline{OE}$	CP	Dn	$\overline{Qn}$	Qn
L	↑	H	L	H
L	↑	L	H	L
L	L	X	$\overline{QO}$	QO
H	X	X	Z	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care
↑ = Transition from low to high level
QO = The level of Q before the indicated steady-state input conditions were established
$\overline{QO}$ = The level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Z = High impedance

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This data sheet is applicable to the CD54/74AC574 and CD54/74ACT574. The CD54/74AC564 and CD54/74ACT564 were not acquired from Harris Semiconductor.

File Number **1948**

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

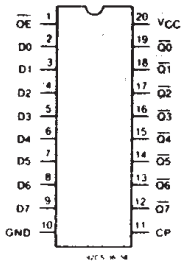
*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

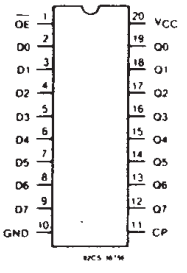
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT564



CD54/74AC/ACT574

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	±0.1	—	±.1	—	±.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
D, $\overline{OE}$	0.7
CP	1.17

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to Clock	t_{SU}	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Maximum Clock Frequency	f_{MAX}	1.5	11	—	10	—	MHz
		3.3	101	—	89	—	
		5	143	—	125	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q AC574	t_{PLH} t_{PHL}	1.5	—	123	—	135	ns
		3.3*	4	13.7	3.8	15.1	
		5†	2.9	9.8	2.7	10.8	
Clock to $\overline{Q}$ AC564	t_{PLH} t_{PHL}	1.5	—	128	—	141	ns
		3.3	4.1	14.4	4	15.8	
		5	2.9	10.3	2.8	11.3	
Output Enable to Q, $\overline{Q}$	t_{PZL} t_{PZH}	1.5	—	165	—	181	ns
		3.3	5.6	19.2	5.5	21.8	
		5	3.7	13.2	3.6	14.5	
Output Disable to Q, $\overline{Q}$	t_{PLZ} t_{PHZ}	1.5	—	165	—	181	ns
		3.3	4.7	16.5	4.5	18.1	
		5	3.7	13.2	3.6	14.5	
Power Dissipation Capacitance	C_{PD}§	—	67 Typ.		67 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_O C_L$ where f_i = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t_W	5†	3.9	—	4.5	—	ns
Setup Time Data to Clock	t_{SU}	5	2	—	2	—	ns
Hold Time Data to Clock	t_H	5	2.6	—	3	—	ns
Maximum Clock Frequency	f_{MAX}	5	125	—	110	—	MHz

†5 V: min. is @ 4.5 V

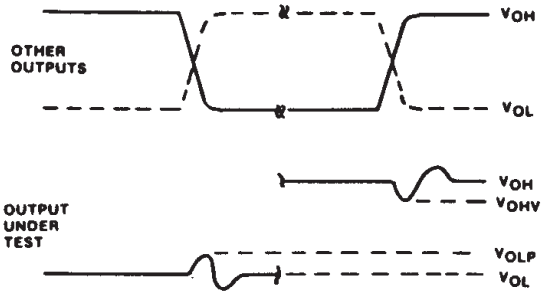
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q ACT574	t_{PLH} t_{PHL}	5†	2.9	10.2	2.8	11.2	ns
Clock to $\bar{Q}$ ACT564	t_{PLH} t_{PHL}	5	3	10.6	2.9	11.7	ns
Output Enable and Disable to Q ACT574	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.7	13.2	3.6	14.5	ns
Output Enable and Disable to $\bar{Q}$ ACT564	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.7	13.2	3.6	14.5	ns
Power Dissipation Capacitance	C_{PD}§	—	67 Typ.		67 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_o C_L + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.

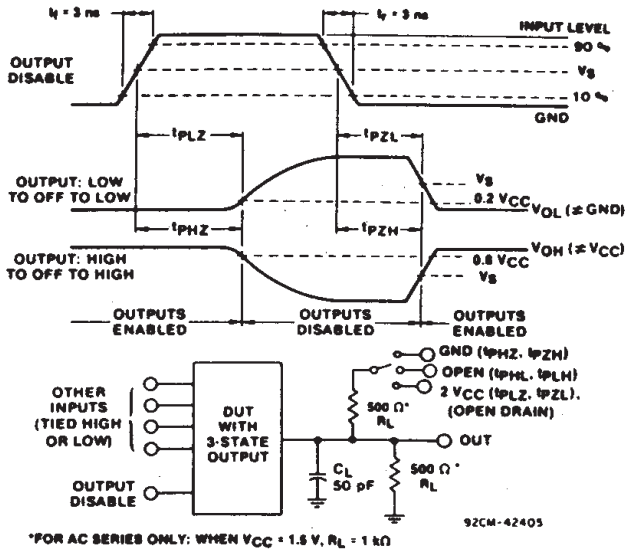
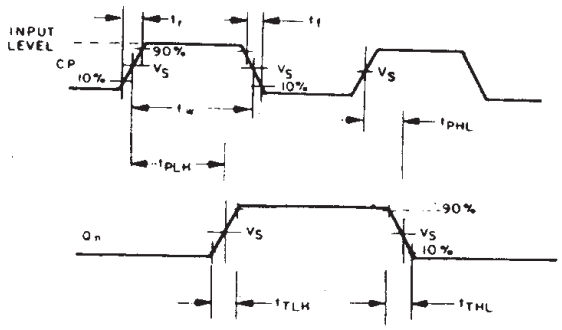


Fig. 2 - Three-state propagation delay waveforms and test circuit.



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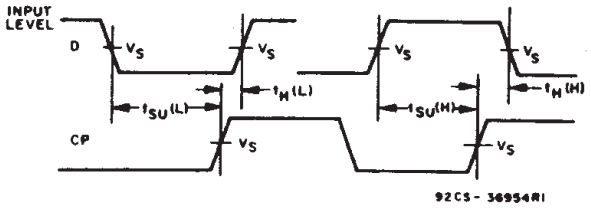

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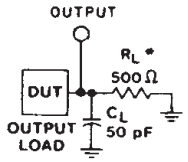

*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CS-42389

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 3 - Propagation delays times and test circuit.

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