RoHS compliant

Features

- Sensor IC based on HALIOS® technology
- Up to 4 sending channels, 1 compensation channel an 1 differential receiver input for various HALIOS® applications
- 16 bit micro controller 'EL16' with debug interface
- Up to 1.5K x 18 (3KByte) SRAM including 2 bit parity per 16 bit word and byte write support
- Up to 30K x 22 (60KByte) FLASH including 6 bit CRC checksum per 16 bit word
- SPI and I²C communication interface
- SCI interface incl. LIN support
- Watchdog, 32 bit timer, up to 8 GPIOs
- Multiply unit
- AEC-Q100 automotive qualification
- Supply voltage range 2.25V to 2.75V

Applications

- Optical or capacitive input devices
- Proximity and gesture detection
- Compact HMI interfaces for one-dimensional up to three-dimensional input

General Description

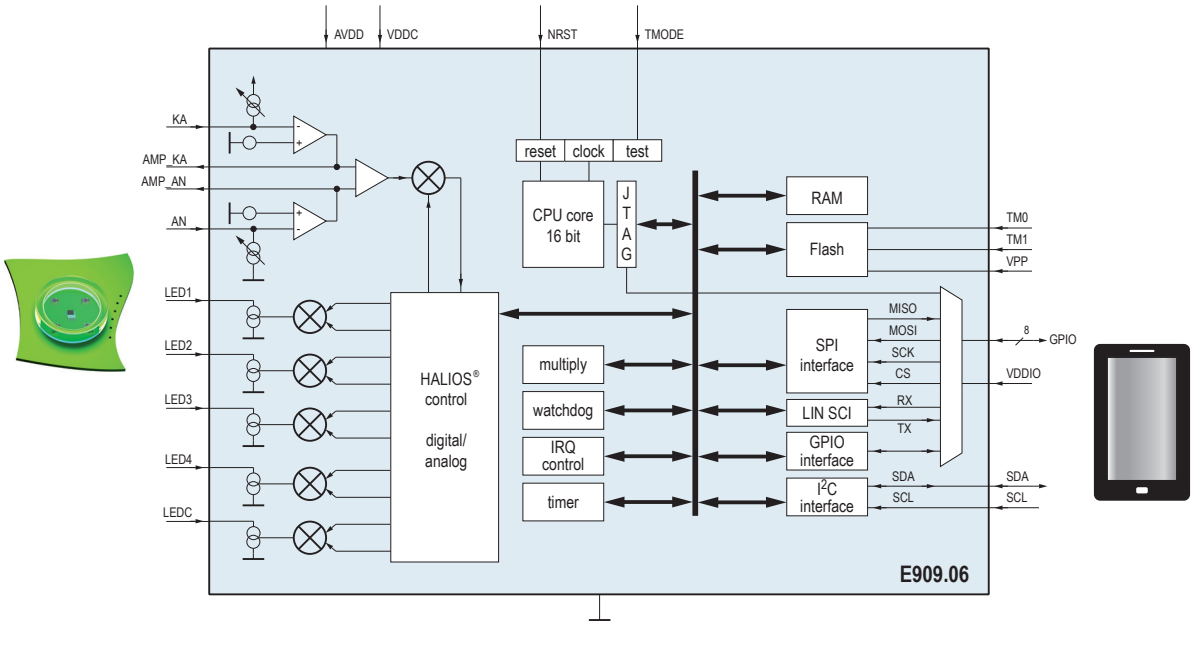
The IC is based on an optical bridge technology which provides a non-mechanical detection of movements.

The system detects the optical reflections of an object in front of the sensor by using a function principle called HALIOS® (High Ambient Light Independent Optical System) which is very effective in the suppression of ambient light and also has self calibration capability to eliminate disturbances caused by housing reflections and scratches.

In the same manner capacitive systems can be addressed by using the integrated charge amplifier.

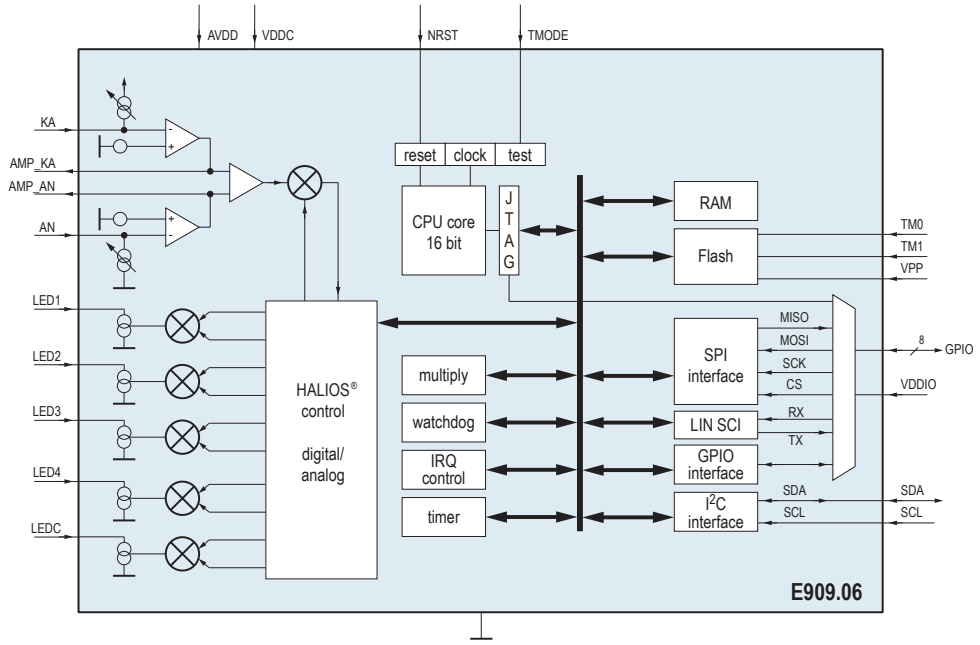
Ordering Information

Ordering No.:	Temp. Range$_{Amb}$	Package
E90906A61C	-40°C to +85°C	QFN32L5



Elmos Semiconductor AG reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

1 Block Diagram



2 Pinout

2.1 Package Pinout

Package: QFN32L5

Package is according JEDEC MO-220-K, version VHHD-4.

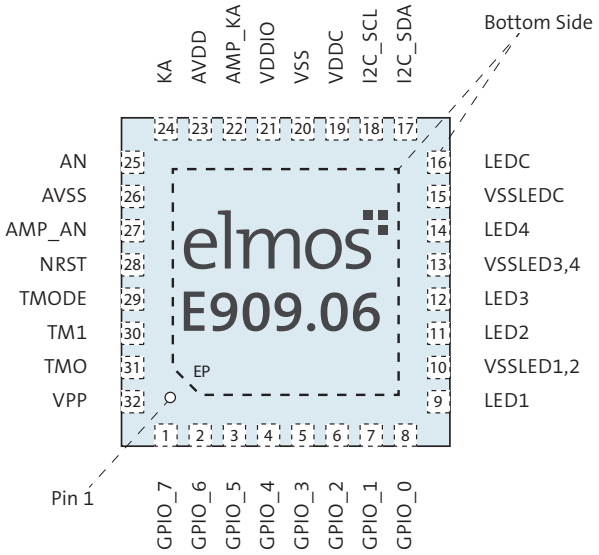


Figure 1. Package Pinout

2.2 Pin Description

No	Name	Type [1)]	Description
1	GPIO_7	D_IO	General Purpose IO 7 (Sr)
2	GPIO_6	D_IO	General Purpose IO 6 (Sr)
3	GPIO_5	D_IO	General Purpose IO 5 (Sr)
4	GPIO_4	D_IO	General Purpose IO 4 (Sr)
5	GPIO_3	D_IO	General Purpose IO 3 (Sr)
6	GPIO_2	D_IO	General Purpose IO 2 (Sr)
7	GPIO_1	D_IO	General Purpose IO 1 (Sr)
8	GPIO_0	D_IO	General Purpose IO 0 (Sr)
9	LED1	A_O	LED Driver output
10	VSSLED1,2	S	Ground LED1,2
11	LED2	A_O	LED Driver output
12	LED3	A_O	LED Driver output
13	VSSLED3,4	S	Ground LED3,4
14	LED4	A_O	LED Driver output
15	VSSLEDC	S	Ground LEDC
16	LEDC	A_O	LED Driver output
17	I2C_SDA	D_IO	I2C SDA (Data)
18	I2C_SCL	D_IO	I2C SCL (CLK)
19	VDDC	S	Core Supply 2.5V
20	VSS	S	Ground
21	VDDIO	S	IO Supply 3.3V
22	AMP_KA	A_O	Output 1. stage amplifier at KA
23	AVDD	S	Analog Supply 2.5V
24	KA	A_I	Cathode
25	AN	A_I	Anode
26	AVSS	S	Analog Ground
27	AMP_AN	A_O	Output 1. stage amplifier at AN
28	NRST	D_I	Reset
29	TMODE	D_I	Testmode
30	TM1	A_IO	Analog Testbus, only used for production test. This Pin must be left open.
31	TM0	A_IO	Analog Testbus, only used for production test. This Pin must be left open.
32	VPP	HV_S	FLASH Testmode pin, only used for production test. This Pin must be connected to GND.
-	EP	S	Exposed Die Pad

1) D = Digital, A = Analog, S = Supply, I = Input, O = Output, HV = High Voltage

3 Operating Conditions

3.1 Absolute Maximum Ratings

Continuous operation of the device above these ratings is not allowed and may destroy the device. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

No.	Description	Condition	Symbol	Min.	Max.	Unit
1	Supply voltage: digital core, analog part	Referenced to V_{SS} / A_{VSS}	V_{DDC} / A_{VDD}	-0.3	2.8	V
2	IO supply voltage/digital pins (see "type"/chapter)	Referenced to V_{SS}	V_{DDIO}	-0.3	3.7	V
3	Input voltage analog pins (see "type"/chapter)	Referenced to A_{VSS}	V_{INA}	-0.3	A_{VDD} + 0.3	V
4	Input voltage digital pins/GPIO (see "type"/chapter)	Referenced to V_{SS}	V_{IND}	-0.3	V_{DDIO} + 0.3	V
5	Ground offset	V_{SS} to A_{VSS} to V_{SSLED}	Ground offset	-0.3	0.3	V
6	Junction Temperature		T_J	-40	+125	°C
7	Storage Temperature		T_{STG}	-50	150	°C

3.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Supply voltage: analog part, digital core	Referenced to V_{SS} / A_{VSS}	V_{DDC} / A_{VDD}	2.25	2.5	2.75	V
2	IO supply voltage/digital pins (see "type"/chapter)	Referenced to V_{SS}	V_{DDIO}	3.0	3.3	3.6	V
3	Filter capacitor analog part	Connected to A_{VDD}	C_{AVDD}		10		µF
4	Filter capacitor digital part	Connected to V_{DDC}	C_{VDDC}		100		nF
5	Ambient operating temperature range		T_{OPT}	-40	25	85	°C
6	Thermal resistance, junction to ambient	QFN32L5	$R_{T,J-A}$		35		°C/W

All voltages are referred to V_{SS}, and currents are positive when flowing into the node unless otherwise specified.

4 Detailed Electrical Specification

The following conditions apply unless otherwise stated. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

4.1 Supply Voltages

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Digital operating current, run mode	FSYS = 8 MHz, system state: run	I_{VDDC}		5.8	12	mA
2	Digital operating current, standby mode	System state: standby	$I_{STANDBY}$		1.8	5	mA
3	Digital operating current, off mode	System state: off	I_{OFF}			35	µA
4	Analog operating current	MCR[13:12] ="11" PCR[14:13] ="11"	I_{AVDD}		3.5	5	mA
5	Analog operating current	Analog on = 0	I_{AVDD_OFF}			15	µA
6	Over all current consumption in application mode	Active mode [1)]	I_{ACTIVE}		2.0	2.25	mA
7	Over all current consumption in application mode	Idle mode ($I_{IDLE} = I_{OFF} + I_{AVDD\_OFF}$)	I_{IDLE}		19 [2)]	88	µA
8	State change from STANDBY to RUN mode		$T_{STANDB-Y2RUN}$			3	1/ FSYS
9	State change from OFF to RUN mode		$T_{OFF2RUN}$			5	1/ FSYS

1) In application mode the current consumption is calculated from the duty cycle of the digital operating current and the analog operating current.
2) at 25°C

MCR - Measurement Configuration Register
PCR - Preamplifier Configuration Register

4.2 Reset Generation

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Power on reset level	Reference is V_{DDC}	V_{POR}			2.25	V
2	Brown out high-to-low threshold level	Reference is V_{DDC}	V_{BOHL}	1.7			V
3	Brown out reset hysteresis		V_{BOHYST}	100	200	300	mV
4	Minimum supply voltage for power on reset and brown out circuit 1)		VDDmin		0.9		V
5	NRST-pin threshold level		$NRST_{LH}$	0.35	0.5	0.65	V_{DDIO}
6	Pull up current NRST-pin	$V_{NRST} = V_{DDIO}$	I_{NRSTPU}	15	35	60	µA
7	Min. pulse width for a valid reset at pin NRST (debouncing)	$V_{DDC} > V_{DDC\ min}$	$T_{DEBNRST}$	1.0		-	µs
8	Delay Watchdog start => reset 1)		T_{WDOG}		timer value		1/ FSYS

1) Will not be tested in production test

4.3 Internal Clock Generation

4.3.1 Reference Clocks

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Wakeup clock frequency	Within recommended operating conditions	FWK	108.2	128.0	147.2	kHz
2	Master clock	Within recommended operating conditions	FSYS	7.2	8.0	8.8	MHz

4.4 Module Description

4.4.1 I²C Interface

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	SDA/SCL: Input voltage low		V_{IL}	-0.3		0.3 x V_{DDIO}	V
2	SDA/SCL: Input voltage high		V_{IH}	0.7 x V_{DDIO}		V_{DDIO} + 0.3	V
3	SDA/SCL: Hysteresis of Schmitt trigger inputs 1)	V_{DDIO} > 2.0 V	V_{hys}	0.05 x V_{DDIO}		-	V
4	SDA/SCL: Output voltage low (open drain)	I = 3 mA, V_{DDIO} > 2.0 V	V_{OL}			0.4	V
5	SDA/SCL: Input current	0 < V_{IN} < V_{DDIO}	I_i	-10		10	µA
6	SDA/SCL: capacitance 1)		C_i	-		10	pF
7	SCL clock frequency		f_{SCL}	0		400	kHz
8	Hold time (repeated) START condition 1)		$t_{HD.:STA}$	600		-	ns
9	LOW period of SCL clock		t_{LOW}	1300		-	ns
10	HIGH period of SCL clock		t_{HIGH}	600		-	ns
11	Set-up time for repeated start condition 1)		$t_{SU.:STA}$	600		-	ns
12	Data hold time 1)		$t_{HD.DAT}$	0		900	ns
13	Data set-up time 1)		$t_{SU:DAT}$	100		-	ns
14	Rise time of SDA and SCL signals with a bus capacitance (C_b) from 10 pF to 400 pF 1)		t_r	20 + 0.1 x C_b		300	ns
15	Fall time of SDA and SCL signals with a bus capacitance (C_b) from 10 pF to 400 pF 1)		t_f	20 + 0.1 x C_b		300	ns
16	SDA/SCL: Output fall time from VIH to VIL with a bus capacitance (C_b) from 10 pF to 400 pF 1)		t_{of}	20 + 0.1 x C_b		250	ns
17	Set-up time for STOP condition 1)		$t_{SU:STO}$	600		-	ns
18	Bus free time between STOP and START 1)		t_{BUF}	1300		-	ns
19	Pulse width of spikes which must be suppressed by the IC-internal input filter		t_{SP}	0		30	ns

1) Will not be tested in production test

4.4.2 SPI Module

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	SCK pulse low width / pulse high width	transfer	Tck	4			1/ FSYS
2	First SCK after falling CSB	start of transfer	Tcs1	2			1/ FSYS
3	Last SCK before rising CSB	end of transfer	Tcs2	2			1/ FSYS
4	Setup time		Tsetup	1			1/ FSYS
5	Hold time		Thold	1			1/ FSYS
6	Data out after shift		Tso			3	1/ FSYS
7	CSB high time		Tcsh	2			1/ FSYS
8	Data out change from Z to driven data	start of transfer	Tz1			1	1/ FSYS
9	Data out change from driven data to Z	end of transfer	Tz2			1	1/ FSYS

4.4.3 GPIO Module

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Threshold point		$GPIO_{TH}$	1.2	1.32	1.46	V
2	Pull down resistor	$V_{IN} > 0.75 \cdot V_{DDIO}$	R_{GPIOPD}	45		155	kΩ
3	Output Voltage Low	GPIOIOL=4 mA; V_{DDIO}=3.3 V	GPIOVOL			0.5	V
4	Output Voltage High	GPIOIOH=-4 mA; V_{DDIO}=3.3 V	GPIOVOH	2.4			V
5	Low Level Output Current	GPIOVOL=0.4V	GPIOIOL	4		17	mA
6	High Level Output Current	GPIOVOH=2.4V	GPIOIOH	-25.6		-6	mA
7	Tri-State Input/Output Leakage Current	Vout=V_{DDIO} or 0 V	GPIOILC	-5		5	µA

4.4.4 HALIOS® Interface

4.4.4.1 Current Generation for LED Modulators

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	DAC resolution		N		10		bit
2	Integral non linearity (INL)		E_i		2		LSB
3	Differential non linearity (DNL)		E_d		2		LSB
4	DAC output voltage at full scale		V_{MAX}	1	1.22	1.5	V

4.4.4.2 LED Driver 1 - 4

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Regulated proportion of LED current @ DAC = 0	DAC = 0	I_{R_MINS}			5 % if I_{R_MAXS} [1)]	mA
2	Max. regulated proportion of LED current (RANGE)	RANGE = 31, DAC = 1023	I_{R_MAXS}	6	10	14	mA
3	Stepsize for regulated current-range configuration		I_{R_STEPS}	90	290	440	µA
4	Resolution current-range configuration		N_{RS}		5		bit
5	Max. fixed proportion of LED current (OFFSET)	OFFSET = 31	I_{O_MAXS}	6.5	10	13.5	mA
6	Stepsize for fixed offset-current configuration		$I_{\_STEPS}$	90	290	440	µA
7	Resolution offset-current configuration		N_{OS}		5		bit
8	DC-bias current		$I_{BIAS\ S}$	60	225	400	µA

1) I_{R_MAXS} is the maximum current selected with parameter RANGE

4.4.4.3 LED Driver C

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Regulated proportion of LED current @ DAC = 0	DAC = 0	I_{R_MINC}			5 % of I_{R_MAXS} [1)]	mA
2	Max. regulated proportion of LED current (RANGE)	RANGE = 31, DAC = 1023	I_{R_MAXC}	2	4	6	mA
3	Stepsize for regulated current-range configuration		I_{R_STEPC}	30	125	200	µA
4	Resolution current-range configuration		N_{RC}		5		bit
5	Max. fixed proportion of LED current (OFFSET)	OFFSET = 127	I_{O_MAXC}	3	5	7	mA
6	Stepsize for fixed offset-current configuration		I_{O_STEPC}	7	40	70	µA
7	Resolution offset-current configuration		N_{OC}		7		bit
8	Minimal value for DC-bias current		I_{BIA_C0}	30	100	200	µA
9	Stepsize for DC-bias current		$I_{DCO\ STEPC}$	0.5	2.5	3.6	mA
10	Max. DC-bias current (DC_OFFSET)	DC_OFFSET = 15	I_{DCO_MAXC}	20	37.6	50	mA

1) I_{R_MAXS} is the maximum current selected with parameter RANGE

4.4.4.4 Receiver

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Feedback resistor of 1. stage amplifier at input KA and AN; bit 0, bit 1 = 1		R_f		50		kΩ
2	Feedback capacitor of 1. stage amplifier at input KA and AN; bit 2, bit 3 = 1		C_f		3.6		pF
3	DC photo-current Gyrator mode; bit 9, bit 10 = 1		I_{DC_photo}			1000	µA
4	Voltage at amplifier input KA		V_{KA}		1.9		V
5	Voltage at amplifier input AN		V_{AN}		1.3		V
6	Corner frequency highpass filter		f_G		10		kHz
7	Gain amplifier 2. stage		G_0	4	6	8	dB
8	Gain amplifier 3. stage	PCR[8:7]="01"	G_3	10	12	14	dB
9	Gain amplifier 3. stage	PCR[8:7]="00" or "11"	G_3	22	24	26	dB
10	Gain amplifier 3. stage	PCR[8:7]="10"	G_3	31	36	38	dB
11	Total gain sym. input	PCR[8:7]="01"	G_{TOT}	114	118	122	dBΩ
12	Total gain sym. input	PCR[8:7]="00" or "11"	G_{TOT}	126	130	134	dBΩ
13	Total gain sym. input	PCR[8:7]="10"	G_{TOT}	138	142	146	dBΩ
14	Total gain nonsym. input	PCR[8:7]="01"	G_{TOT}	108	112	116	dBΩ
15	Total gain nonsym. input	PCR[8:7]="00" or "11"	G_{TOT}	120	124	128	dBΩ
16	Total gain nonsym. input	PCR[8:7]="10"	G_{TOT}	132	136	140	dBΩ
17	Center frequency	1)	f_C		125		kHz
18	Resolution demodulator output		N_{DEMOD}		1		bit
19	Capacitance of photo diode at input KA	1)	C_{DIODE}			70	pF
20	Internal reference current		I_{BIAS}	5	10	16	µA

PCR - Preamplifier Configuration Register

1) Will not be tested in production test

5 Functional Description

5.1 Introduction

The general architecture of the 3D-optical input device is shown in the system block diagram.

The CPU is connected to the memory (FLASH and SRAM) and the peripheral modules via the internal system bus. The system bus provides a 16 bit address space and allows 8 and 16 bit data transfers.

The memory contains the program code and the data. Memory and registers are mapped to the global memory map and can be accessed through all memory related operation provided by the CPUs instruction set. The memory of the ASIC consists a FLASH cell up to 30Kx22 (60KByte) including 6 additional bits per word used as CRC for error detection and error correction and a SRAM cell up to 1.5Kx18 (3KByte) including 2 bit parity per word.

The Interrupt Controller collects requests from all interrupt sources and provides an interrupt signal to the CPU. Interrupt sources can be masked within the interrupt controller. Interrupts are generated by the modules and hold until they are cleared within the module. See module description for clearing procedures.

The SPI can be configured either as a master or a slave. Transfer length is eight bit and can be extended by a multiple of eight bit. Data FIFOs are provided for transmit and receive tasks.

The SCI provides the standard NRZ (Non Return to Zero) mark/space data format where each frame contains one start bit, eight data bits and one stop bit. Several features are implemented for special LIN support.

The timer module contains a 32 bit timer module as well as a watchdog timer. Additionally a second timer module operating on wakeup clock is implemented that remains active even in off mode, so it can be used for a periodical wake up from off mode for applications that require a low current consumption.

8 IO port pins can either be configured as general purpose IO`s or can be configured as ports for the SPI or SCI module. Additionally two ports are reserved for the I²C slave interface.

The clock and reset generator module provides the system clock and the global reset signal. A power-on-reset, brown out detect and a power watch are implemented. As external reset source a reset input will be considered. The system clock is generated by an on-chip oscillators. A more detailed diagram of the clock/reset generation block (CRG) is shown in the following sections.

5.2 Supply Voltages

5.2.1 Block Diagram

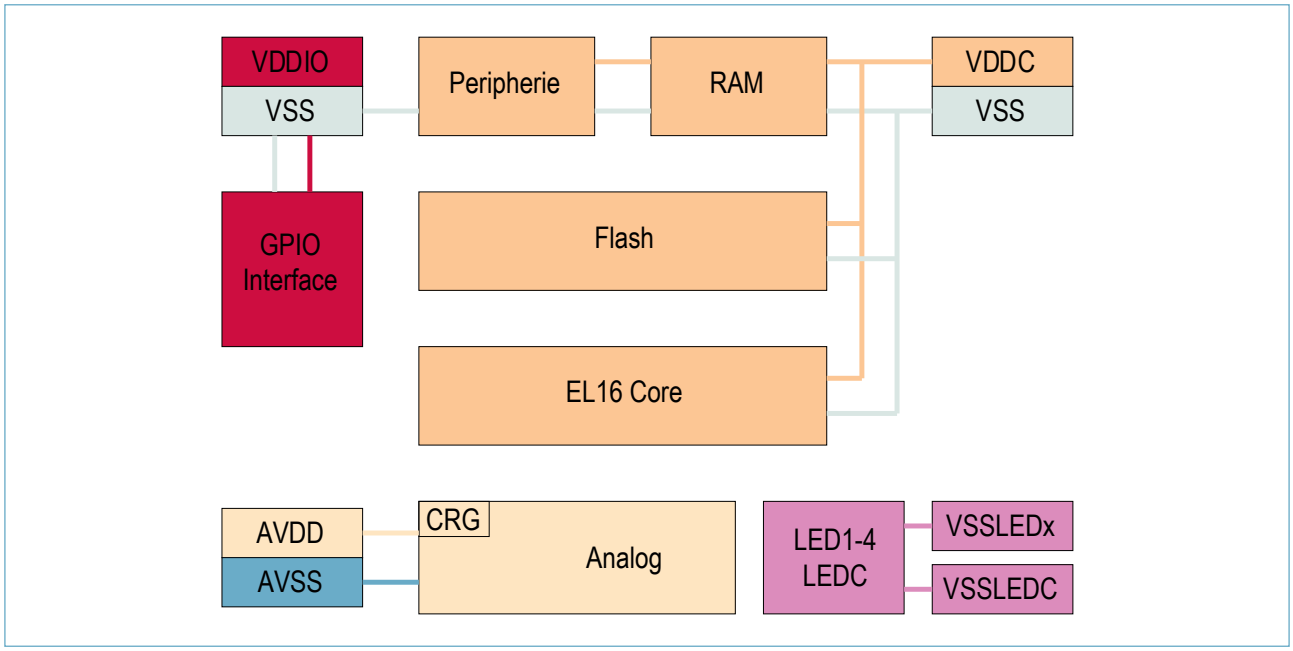


Figure 2. Block Diagram Supply Voltages

5.2.2 Functional Description

Three separate power supplies are needed to operate the IC. The core voltage supplying all digital blocks, the analog parts needed for the oscillator and supply observation as well as the preamplifiers of the output pads and the IO supply which powers the post drivers of the GPIO pads. The third supply is used for the HALIOS® measurement analog part. In the figure above the different power supply regions are depicted.

5.2.3 Power Up Sequence Considerations

During power-up the power-on-reset configures all pads as inputs consequently disabling the output drivers. The IO supply is watched after power up if the core supply is in the specified range and causes a reset if it leaves the allowed region. The core supply is watched via a brown out circuit.

The pads will remain input pads as long as the software does not reconfigure them.

According the following diagram it must be guaranteed that ADVV / DVVC is not switched on before VDDIO. NRST can be switched on if the VDDIO and AVDD/DVVC are stabilized on its potential.

A >= 0ms
B > 5ms (recommended)

To avoid floating gates, A < 100µs is recommended.

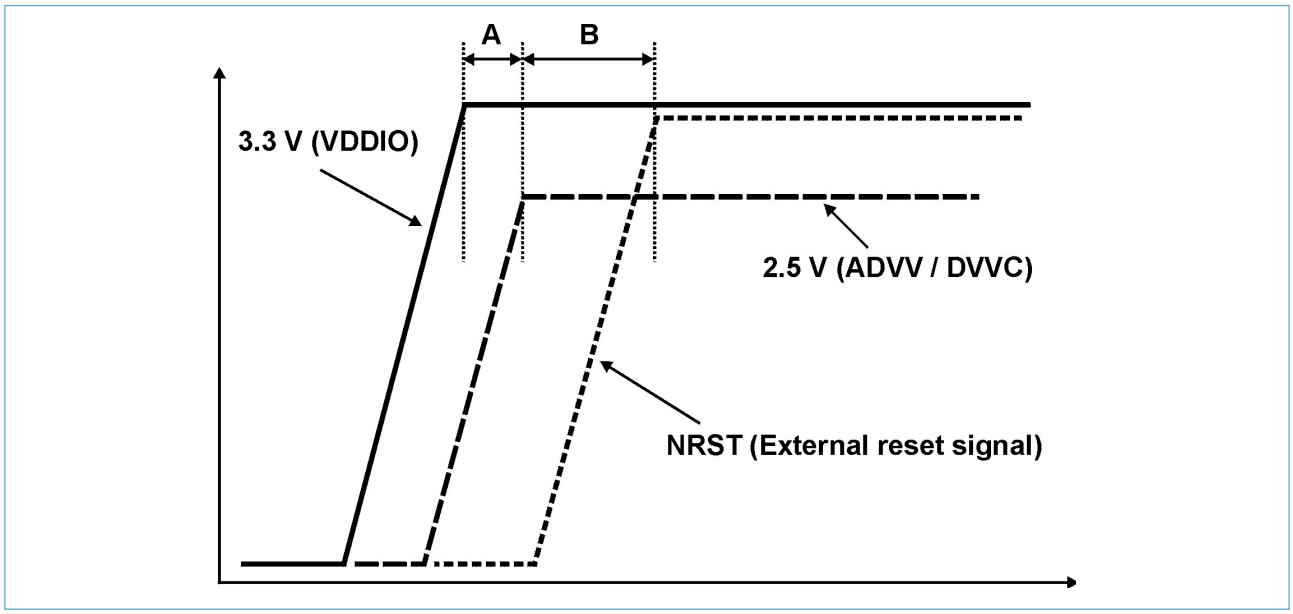


Figure 3. Power Up Sequence: A >= 0 ms; B > 5 ms

5.2.4 Power Down Sequence Considerations

During power down the chip will enter the reset state as soon as the core or IO supply leaves the specified region bringing all pads into input configuration again.

Note: It has to be assured that VDDIO – VDDC > -0.3V at any time during power up and power down.

5.3 Brown Out Detection

5.3.1 Timing Diagram

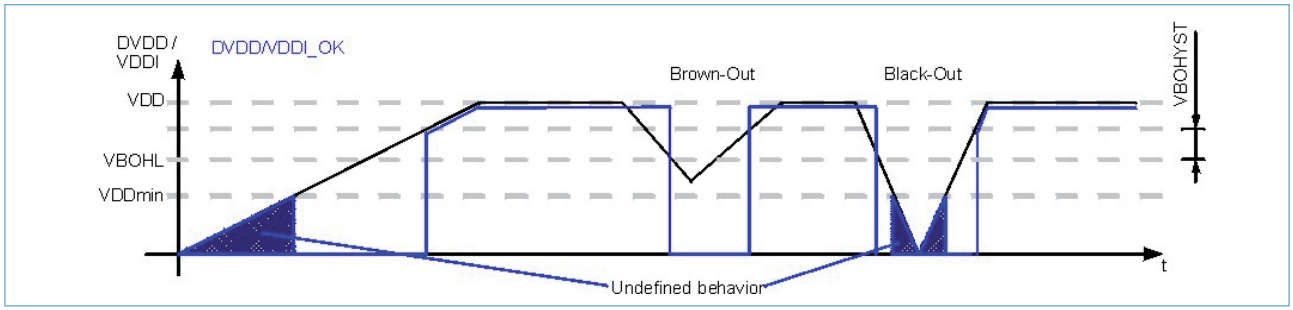


Figure 4. Brown-Out timing diagram

5.3.2 Functional Description

The brown out detection of the chip will cause a reset whenever the core or IO power supply falls below the specified region. An over-voltage protection is not implemented. The circuit will not be operational when the core supply is below VDDmin. In these cases the power-on-reset will take care of proper reset generation.

5.4 Reset Generation

5.4.1 Reset Generation (RESGEN)

The IC is equipped with a reset input pin which can be used to reset the chip. Any low pulse longer than $T_{DEBNRST}$ on the external reset line will be sensed and causes an IC reset.

The IC contains different dynamic and static reset sources. The static sources trigger the master reset as long as the cause for the reset persists. The dynamic sources trigger the reset for a defined minimum reset time. After that time has expired the system reset is released. In case the dynamic source is still signaling a reset the reset is re-triggered.

Static reset sources:
- A power up sequence of the core voltage (power on reset)
- Brown out of the core voltage

Dynamic reset sources:
- Uncorrectable FLASH CRC error
- SRAM parity error
- CPU register parity error
- Watchdog timeout
- Uncorrectable trim register ECC error

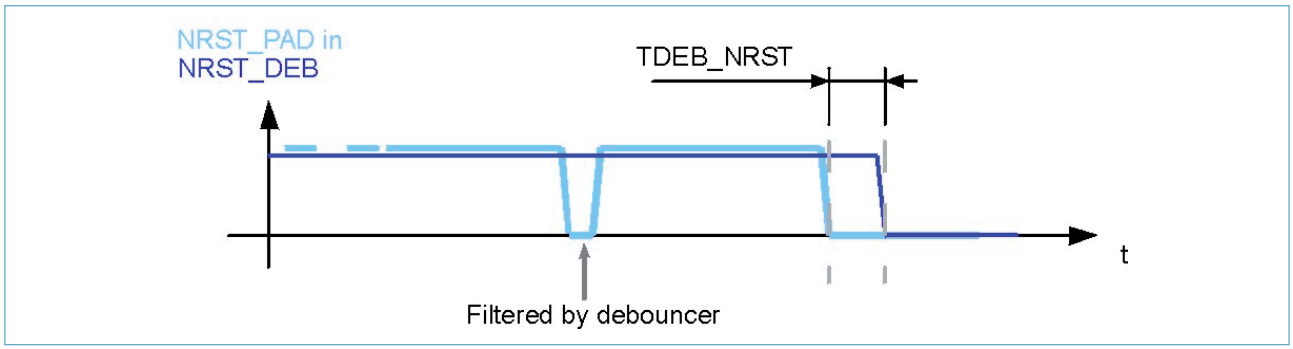


Figure 5. Timing of the external reset signal

5.4.2 Power-On-Reset

5.4.2.1 Timing Diagram

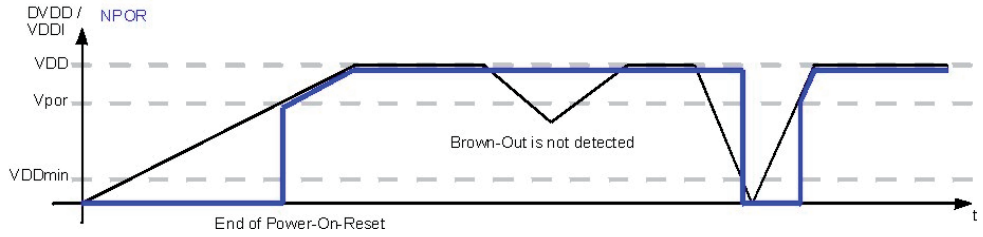


Figure 6. Power-On-Reset timing digram

5.4.2.2 Functional Description

The power on reset is designed to cause a reset during the power on cycle of the chip. The reset will be deactivated when the supply crosses V_{POR}.

After the power up sequence the power on reset block will only cause a new reset if the power supply voltage drops below VDDmin and the rise and fall times of the supply are below the specified values.

5.5 System States

system state	EL16	SPI, watchdog, timer1, GPIO	wakeup timer	I²C interface	current consup-tion
RUN	ON	ON	ON	ON	IRUN
STANDBY	halted	ON	ON	ON	ISTANDBY
OFF	halted	halted	halted	ON	IOFF

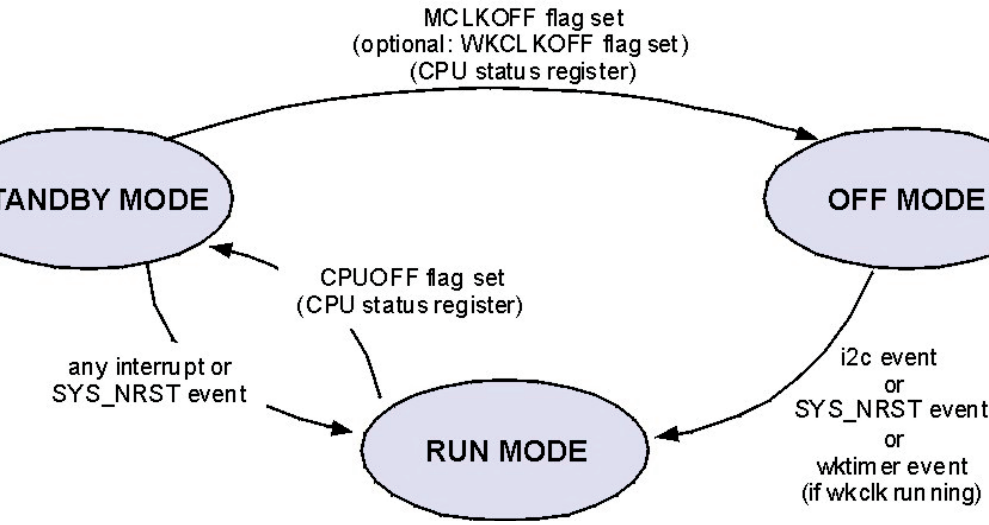


Figure 7. System States Diagram

1. RUN state:

- master clock = FSYS
- wakeup clock = FWK
- standby state by setting CPUOFF flag (CPU status register) -> entering STANDBY state
- off state by setting CPUOFF flag and MCLKOFF flag (CPU status register) -> entering OFF state
- note: after setting the MCLKOFF and/or CPUOFF bit in the CPU status register the following instruction will be executed, the next will be fetched, then standby or off mode will be entered. Therefore it is recommended to execute two NOP instructions after setting the corresponding bits in the status register. The STANDBY or OFF state has to be entered in a save state without enabled interrupts.

2. STANDBY state:

- CPU halted (no system bus requests -> standby of FLASH and SRAM)
- master clock = FSYS
- wakeup clock = FWK
- wakeup by any interrupt -> returns to RUN state
- wakeup by SYS_NRST event (see Reset Generation Diagram) -> returns to RUN state

3. OFF state:

- master clock = off
- wakeup clock = on / off (defined by application software, CPU status register)
- wakeup by specific (external) signal event (I2C or wakeup timer) -> returns to RUN state
- wakeup by SYS_NRST event (see Reset Generation Diagram) -> returns to RUN state

5.6 System Failsafe Features

failsafe feature	asserts interrupt	asserts reset
FLASH CRC (bit error corrected)	X	
FLASH CRC (uncorrectable bit error)		X
empty (erased) FLASH word read detection		X
FLASH write detection	X	
RAM byte parity		X
uninitialized RAM word / byte read detection		X
CPU register parity		X
CPU undefined opcode detection	X	
CPU misaligned word access detection	X	
opcode execution memory protection	X	
stack overflow detection	X	
invalid module register access detection	X	
watchdog time-out		X
watchdog window protection	X	
brownout detection (supply voltage monitoring)		X
system clock monitoring		X

5.7 HALIOS® Interface

5.7.1 HALIOS® Block Diagram

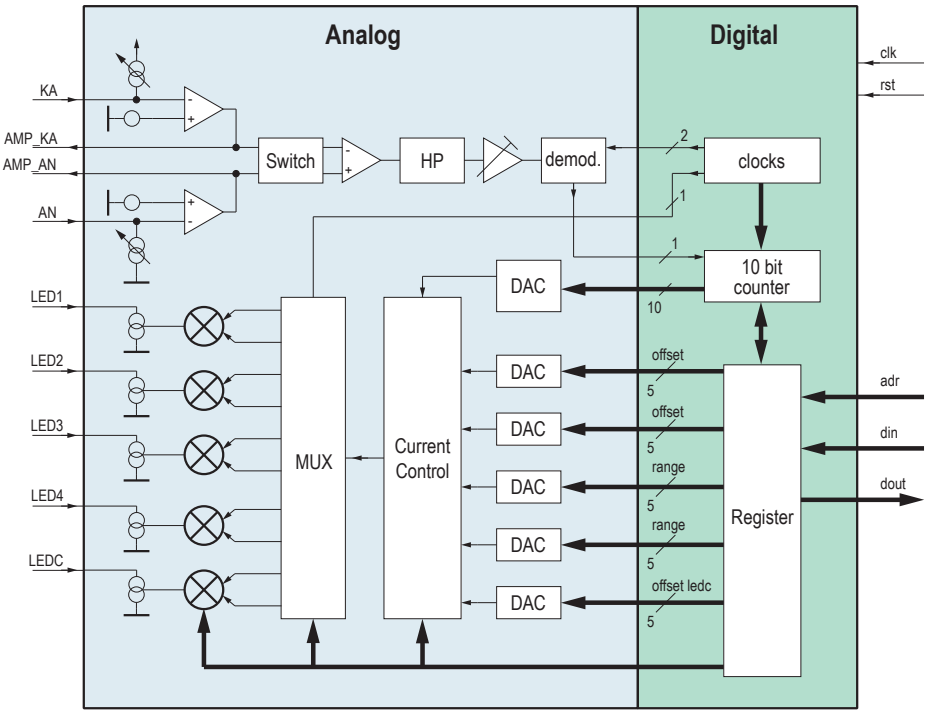


Figure 8. HALIOS® Block Diagram

5.7.2 HALIOS® Features

In order to be able to realize optical as well as capacitive sensors the input amplifier can be changed in its characteristic between transimpedance amplifier and charge amplifier. This is achieved by changing the feedback impedance. To have a good immunity to noise the receiving path consists of a symmetrical differential input.

The HALIOS® ASIC contains a configurable current driver interface. In the case of an optical sensor it is possible to drive up to four sending LEDs and one compensation LED. If a capacitive sensor should be realized, the current is converted into a voltage by connecting pullup resistances at the outputs LEDx. The HALIOS® measurement loop is closed by a 10 bit DAC which regulates the output current for the sending/compensation LED. The DAC is controlled by a counter that sets the DAC dependent on the received signal amplitudes up or down.

To follow fast signal changes the counter can be increased or decreased by 1, 2, 4 or 8 steps, this is called the step size that is set due to the number of up/down-counts in the same direction. To start a new measurement the interface is configured with the counter-value and the step size (generally the values from the last measurement), the LED configuration and the current configuration for the LED driver. The measurement regulates the DAC and performs 25 counter steps to follow the actual reflection conditions of the sensor. After one measurement the interface returns the counter-value, the mean-value (it is calculated from the last 16 counter-steps during one measurement) and the stepsize from the last integrator cycle.

After the automated measurement cycle is finished an interrupt appears if the interrupt is enabled. The interrupt is used to wake the system from standby mode.

The HALIOS® clock is adjustable in 5 frequencies (FSYS=8 MHz):
- 167 kHz
- 125 kHz (default)
- 100 kHz
- 83 kHz
- 71 kHz

5.7.3 HALIOS® Module Registers

Register Name	Address	Description
Start Value Counter	0x00	
Measurement Configuration	0x02	
Measurement Configuration HALIOS® Clock	0x04	
Current Configuration Phase A	0x06	
Current Configuration Phase B	0x08	
Current Configuration Compensator Offset	0x0A	
Measurement Result: Counter Value	0x0C	
Measurement Result: Mean Value	0x0E	
Interrupt	0x10	
Preamplifier Configuration	0x12	
Send Frequency Select	0x14	

Register Start Value Counter (0x00)

	MSB															LSB
Content	15:12					10	9:0									
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:12** : STZ: Startup step size for one step of the integrator (range: "0001", "0010", "0100" or "1000") **10 : 0** - normal settling time of optical gyrator 1 - decrease settling time of optical gyrator **9:0 :** STRTCNT: Startup counter - value from the integrator (range: 0 ... 1023) reset value: 0x0000															

Register Measurement Configuration (0x02)

	MSB															LSB
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : HALMEAS: Starts a new measurement phase, switching from '0' to '1' starts measurement. After measurement the bit resets itself. **14** : ACCON: En/disables the acceleration of the integrator ('0' = disabled, '1' = enabled) **13** : Deactivation of AN input to reduce current consumption in the case that only the KA input is used ('0' = active, '1' = deactivated) **12** : AON: Control of analogue part ('0' = off, '1' = on) **11** : FIXB: Sets the LEDs activated in phase B to fixed sending current ('0' = variable, '1' = fixed) **10** : FIXA: Sets the LEDs activated in phase A to fixed sending current ('0' = variable, '1' = fixed) **9** : LED C A: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: Bits 9 downto 0 will be reset after measurement **8** : LED C B: Decides if LED is active for the measurement ('0' = off, '1' = on) **7** : LED 4 A: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **6** : LED 4 B: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **5** : LED 3 A: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **4** : LED 3 B: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **3** : LED 2 A: Decides if LED is active for the measurement ('0' = off, '1' = on) **2** : LED 2 B: Decides if LED is active for the measurement ('0' = off, '1' = on) **1** : LED 1 A: Decides if LED is active for the measurement ('0' = off, '1' = on) **0** : LED 1 B: Decides if LED is active for the measurement ('0' = off, '1' = on) reset value: 0x0000															

Register Measurement Configuration HALIOS® Clock (0x04)

	MSB															LSB
Content												4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**4** : Polarity of LEDC Modulator clock ('0' = normal, '1' = inverted) **3** : Polarity of LED4 Modulator clock ('0' = normal, '1' = inverted) Note: not available in version 1 and version 2 **2** : Polarity of LED3 Modulator clock ('0' = normal, '1' = inverted) Note: not available in version 1 and version 2 **1** : Polarity of LED2 Modulator clock ('0' = normal, '1' = inverted) **0** : Polarity of LED1 Modulator clock ('0' = normal, '1' = inverted)															

Register Current Configuration Phase A (0x06)

	MSB															LSB
Content							9:5					4:0				
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**9:5** : OFF: Offset phase A **4:0** : RNG: Range phase A															

Register Current Configuration Phase B (0x08)

	MSB															LSB
Content							9:5					4:0				
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**9:5** : OFF: OFFSET phase B **4:0** : RNG: RANGE phase B															

Register Current Configuration Compensator Offset (0x0A))

	MSB															LSB
Content					11:8					6:0						
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**11:8** : DC_OFFSET current LEDC (4 Bit) **6:0** : OFFSET compensation LEDC															

Register Measurement Result: Counter Value (0x0C)

	MSB															LSB
Content	15:12						9:0									
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:12** : STZ: Stepsize integrator **9:0** : COUNT: Integrator value from the measurement															

Register Measurement Result: Mean Value (0x0E)

	MSB															LSB
Content	15:12				11:0											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:12** : STZ: Stepsize integrator **11:0** : MEAN: Mean value from the measurement															

Register Interrupt (0x10)

	MSB							LSB
Content							1	0
Reset value	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R/W	R/W
External access	R	R	R	R	R	R	R/W	R/W
Bit Description	**1** : CLHALI: Clear HALIOS® interrupt 0 - no influence 1 - clear HALIOS® interrupt **0** : HALIE: HALIOS® interrupt enable: 0 - interrupt disabled 1 - interrupt enabled							

Register Preamplifier Configuration (0x12)

	MSB															LSB
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : Enlarge Phasemargin PM for 1. stage amplifiers in capacitive mode ('0' = PM low and fast, '1' = PM high and slow) Bias current **14 13** IB 1 1 2µA 1 0 10µA 0 0 I30µA **12** : Deactivate Gyrator at AN input: ('0' = on, '1' = off) **11** : Deactivate Gyrator at KA input: ('0' = on, '1' = off) **10** : Select between optical and capacitive gyrator at AN input: ('0' = optical, '1' = capacitive) Note: not available in version 1 and version 3 **9** : Select between optical and capacitive gyrator at KA input: ('0' = optical, '1' = capacitive) Note: not available in version 1 and version 3 Select amplification of 3. Stage AMP **8 7** amplification 0 0 16 0 1 4 1 0 64 1 1 16 **6** : Switch AN Input off: ('0' = on, '1' = off) **5** : Switch KA Input off: ('0' = on, '1' = off) **4** : Polarity of the Switch between 1. stage output and summation amplifier: Polarity inverted ('0' = normal, '1' = inverted) **3** : 1. stage amplifier AN input: CF Feedback capacitor deactivation ('0' = on, '1' = off) **2** : 1. stage amplifier KA input: CF Feedback capacitor deactivation ('0' = on, '1' = off) **1** : 1. stage amplifier AN input: RF Feedback resistor deactivation ('0' = on, '1' = off) **0** : 1. stage amplifier KA input: RF Feedback resistor deactivation ('0' = on, '1' = off) reset value: 0x0000															

Register Send Frequency Select (0x14)

	MSB															LSB
Content														2:0		
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Bit Description	**2:0** : HALIOS® send frequency select SendFreq (sfreq) frequency = FSYS/(sfreq*16) sfreq range 3..7 reset value: 0x0004															

5.7.4 Current Generation for LED Modulators

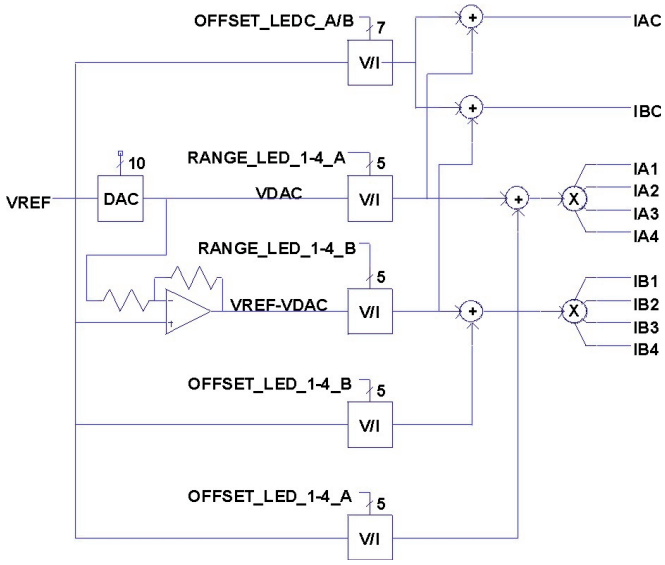


Figure 9. Block Diagram Modulator

This block is used to generate the switched part of the LED-current. The DAC produces an output voltage between 0 and V_{REF} with a resolution of 10 bit. With the help of the amplifier a second voltage is generated which runs interdependently at the same time between V_{REF} and 0 in a way, that the sum of both voltages has a fix value.

These two voltages feed two voltage to current (V/I) converters with a 5 bit digitally adjustable transconductance for independently setting the control range. An individually adjustable offset current is added using three additional V/I-converters.

The setting of the range and offset is done individually for each V/I-converter and LED respectively.

The inputs of the first two V/I-converters can be set to a fixed voltage (not shown for simplicity) to have one branch of the HALIOS® system unregulated at a fixed current level. The outputs are fed into a current mirror to multiple currents for the LED drivers.

5.7.5 LED Driver 1 - 4

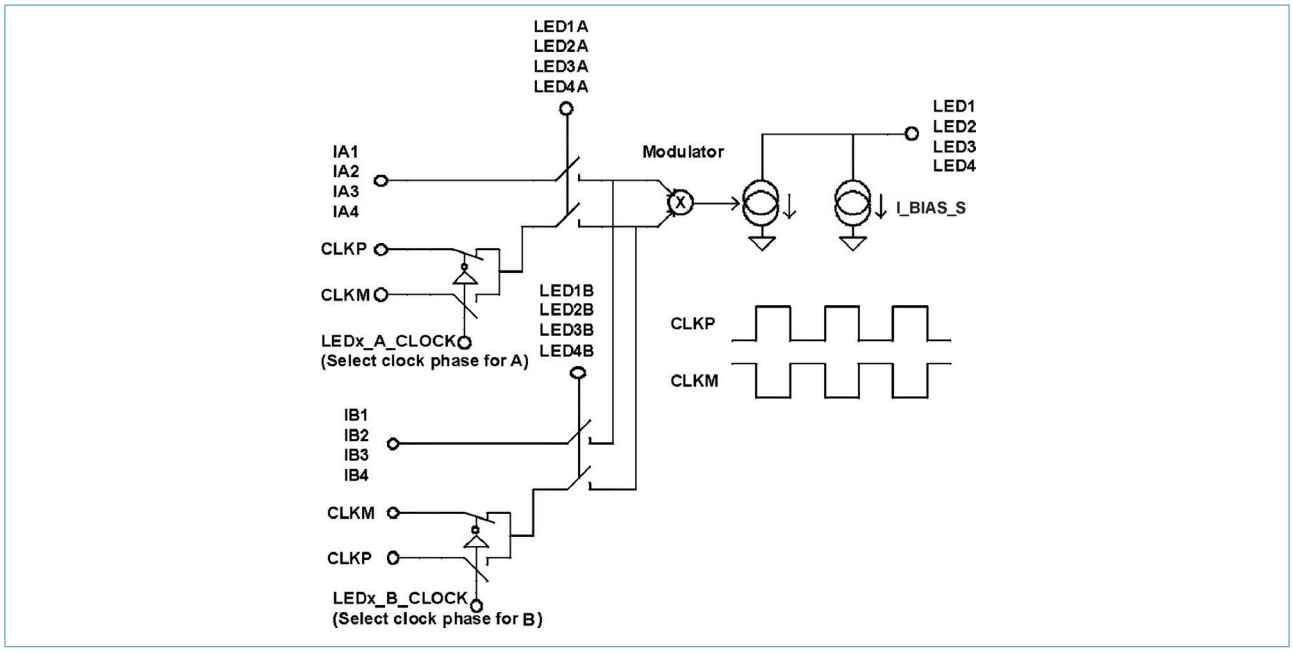


Figure 10. Block Diagram "LED Driver 1 - 4"

This diagram shows the signal flow of one LED driver. The input can be set to a current which increases with the DAC-value (IAx) in clock phase P or clock phase M or to a current which decreases with increasing DAC-value (IBx) in clock phase M or clock phase P. Setting none of the switches LEDxA and LEDxB the driver is inactive. Additionally the LED is biased with a DC-current to have a more linear characteristic, to increase the speed and to reduce the differential voltage drop between turn on and turn off for a low electrical crosstalk between the LEDs and the receiver input.

5.7.6 LED Driver C

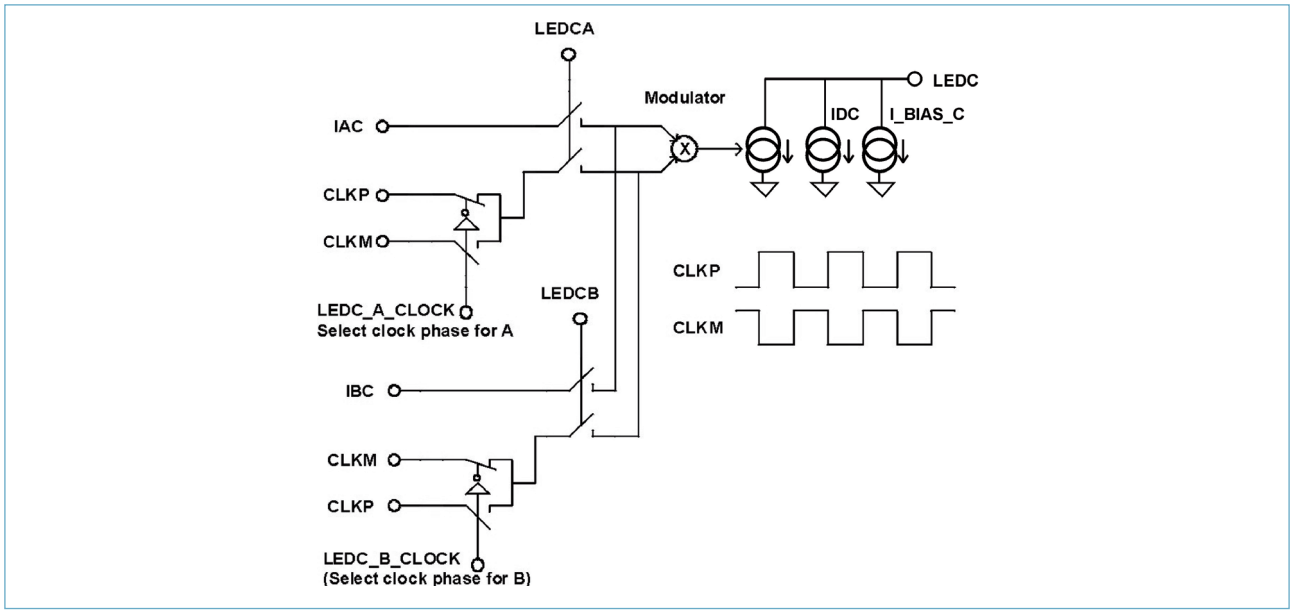


Figure 11. Block Diagram "LED Driver C"

This driver has a special functionality since it is optimized for HALIOS®-loops with a strong asymmetry. This situation is typical in proximity applications. An offset current can be added which is generated in the central current generation block. This can be useful in proximity applications when there is a large optical coupling from the sending LEDs into the receiver.
Additionally the DC current (IDC) of the LEDC output can be set to a value up to several tenth of milliamps with a resolution defined by a four bit DAC. The purpose of this is to improve the temperature behaviour by equalizing the power consumption of the LEDC with the LED1 - 4.

The DC current IDC allows to approach the operating point of LEDC closer to the operating point of LED1..4. Because the power consumption of LEDC is much lower than of LED1..4, the operating points of the LEDs differ. With IDC the operating point of LEDC is adjusted to get a similar operating point like LED1..4 and therefore a compensated temperature behaviour within the system.

5.7.7 Current Equations

Presupposed, the sending phase is Phase B:
In the regulated current mode (FIXB = '0') the total sending current is:

(1) $$I_{SEND} = \left[I_{OFFSET\_S} + \frac{1023 - I_{REGULATE}}{1023} \cdot I_{RANGE\_S} \right] \cdot CLK_S + I_{BIAS\_S}$$

(2) $$I_{REGULATE} = 0...1023 \quad (10\ \text{bit DAC})$$

(3) $$I_{OFFSET\_S} = OFFSET\_S \cdot I_{O\_STEPS\_S}$$

(4) $$I_{RANGE\_S} = RANGE\_S \cdot I_{R\_STEPS\_S}$$

(5) $$CLK_S = \text{'1' or '0' (Phase B; polarity P or N)}$$

In the constant current mode (FIXB = '1') the total sending current is:

(6) $$I_{SEND} = \left[I_{OFFSET\_S} + \frac{I_{RANGE\_S}}{2} \right] \cdot CLK_S + I_{BIAS\_S}$$

Presupposed, the compensating phase is Phase A:
In the regulated current mode (FIXA = '0') the total compensating current is:

(7) $$I_{COMP} = \left[I_{OFFSET\_C} + \frac{I_{REGULATE}}{1023} \cdot I_{RANGE\_C} \right] \cdot CLK_C + I_{BIAS\_C} + I_{DC}$$

(8) $$I_{REGULATE} = 0...1023 \quad (10\ \text{bit DAC})$$

(9) $$I_{OFFSET\_C} = OFFSET\_C \cdot I_{O\_STEPS\_C}$$

(10) $$I_{RANGE\_C} = RANGE\_C \cdot I_{R\_STEPS\_C}$$

(11) $$CLK_C = \text{'1' or '0' (Phase A; polarity P or N)}$$

(12) $$I_{DC} = \text{Current for temperature compensation}$$

In the constant current mode (FIXA = '1') the total sending current is:

(13) $$I_{SEND} = \left[I_{OFFSET\_S} + \frac{I_{RANGE\_S}}{2} \right] \cdot CLK_S + I_{BIAS\_S} + I_{DC}$$

5.7.8 Receiver

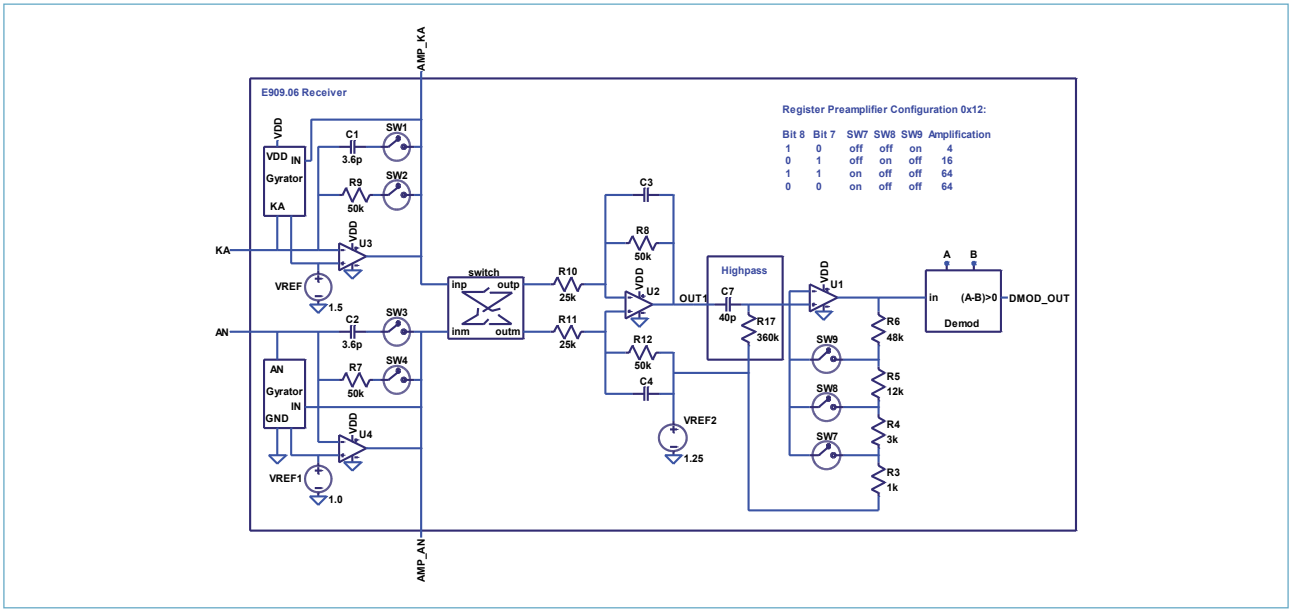


Figure 12. Receiver Block Diagram

The receiving path uses a amplifier with a symmetrical differential input with two stages. The first stage consists of two amplifiers having each its own reference voltage. The second stage does the differential to single ended conversion and has a amplification factor of 2. The behavior of the first stage can be chosen between transimpedance amplifier (TIA) and charge amplifier by using different internal feedback impedances.
The output signal of the second stage is then amplified with an third amplifier stage separated by a high pass filter to remove disturbing signals and amplifier offsets. The demodulator samples the voltages at the output of the amplifier during phase A and phase B, takes the difference and delivers the sign of this difference to its output. H-level means A > B and L-level means A < B.
In the case a photodiode is used at the inputs KA and AN the first stage should configured as TIA and the gyrator, which suppresses the DC photocurrent, must be activated. The voltage difference between the two reference voltage sources of the first stage amplifiers is 0.5V and ensures a reverse voltage at the photodiode.
If the amplifier is used as a capacitive sensor the capacitive gyrator must be switched on (Bit12 of register preamplifier configuration). The first stage can be configured as charge amplifier or as TIA dependent on the application. If the feedback capacitance should be larger than internal available also external feedback capacitors can be used.
The switch between the first stage and the second stage allows to invert the polarity of the signals. This function is needed if the AN input is used as ground referenced input. In order to have a negative feedback of the HALIOS® regulation loop the polarity must be changed. In the case the KA and AN input are used as 2:1 MUX input for two ground referenced sensors it is also possible to switch one of the inputs in high resistance state.

6 Microcontroller EL16H6

The EL16H6 is based on a 16-bit RISC CPU core. It includes a 30Kx22 (60 Kbyte) FLASH Memory with 6 bit CRC checksum per 16 bit word and a 1.5Kx18 (3 Kbyte) SRAM with byte write support. It provides up to 16 general purpose I/O's, one synchronous Serial Peripheral Interface (SPI) and one asynchronous Serial Interface (SCI). SPI and SCI can be mapped to the IO port or to the D2D port. Furthermore a 32 bit timer and a watchdog are included. As the system clock source either an on-chip oscillator or a crystal oscillator can be selected.

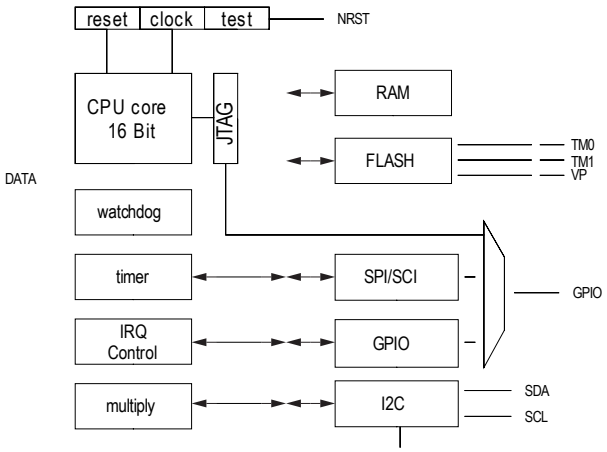


Figure 13. µC Block Diagram

6.1 Feature List

- RISC architecture with 27 instructions and 7 addressing modes
- 16 registers including PC, SP and status register
- 16 bit address range
- Word and byte addressing
- Interrupt support
- Standby and stop mode support
- Automatic bus ready handling
- Debugging support (JTAG interface)
- 3 hardware breakpoint triggers
- Failsafe architecture

6.2 Debugging

To access the debug structures of the EL16 CPU a 4-wire standard JTAG interface is used. The JTAG interface can be accessed via GPIO pins when the TEST_MODE pin is set to one. TEST_MODE pin set to zero resets all test and debug structures and the IC operates in normal mode.

The EL16 embedded breakpoint logic provides the following features:

- 3 breakpoint triggers
- Each trigger can match a separate address or data bus value
- A trigger value compare mask can be defined
- Trigger can match a greater, smaller, equal or non equal value
- Trigger can be configured for read / write or instruction fetch / non instruction fetch bus cycles
- Triggers can be combined (trigger dependency)
- All breakpoints can be used for stepping and run-stop a program

6.3 CPU Registers

The EL16 contains 16 registers (R0 to R15) including Program Counter, Stack Pointer and Status Register.

6.3.1 Program Counter (PC)

The 16-bit Program Counter (PC/R0) points to the next instruction to be executed. Each instruction uses an even number of bytes (two, four, or six), and the PC is incremented accordingly. Instruction accesses in the 64-KB address space are performed on word boundaries, and the PC is aligned to even addresses. The PC can be addressed with all instructions and addressing modes.

6.3.2 Stack Pointer (SP)

The Stack Pointer (SP/R1) is used by the CPU to store the return addresses of subroutine calls and interrupts. It uses a pre-decrement, post-increment scheme. In addition, the SP can be used by software with all instructions and addressing modes. The SP is initialized into RAM by the user, and is aligned to even addresses.

6.3.3 Status Register (SR)

The Status Register (SR/R2), used as a source or destination register, can be used in the register mode only addressed with word instructions. The remaining combinations of addressing modes are used to support the constant generator.

Register Name	Address	Description
Status Register	SR/R2	

Register Status Register (SR/R2)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**Bit 8** : V **Bit 5** : CLK OFF **Bit 4** : CPU OFF **BIT3** : GIE **Bit2** : N **Bit1** : Z **BIT0** : C															

V: Overflow bit
This bit is set when the result of an arithmetic operation overflows the signed-variable range.

CLKOFF: Stop flag
CPU clock gated

CPUOFF: Standby flag
CPU halted

GIE: Global Interrupt Enable

N: Negative bit
This bit is set when the result of a byte or word operation is negative and cleared when the result is not negative. Word operation: N is set to the value of bit 15 of the result Byte operation: N is set to the value of bit 7 of the result

Z: Zero bit
This bit is set when the result of a byte or word operation is 0 and cleared when the result is not 0.

C: Carry bit
This bit is set when the result of a byte or word operation produced a carry and cleared when no carry occurred.

6.3.4 Constant Generation Registers CG1 and CG2

Six commonly-used constants are generated with the constant generator registers R2 and R3, without requiring an additional 16-bit word of program code. The constants are selected with the source-register addressing modes (As), as described in the table below:

Register Name	As	Value	Remarks
R2	00	-	register mode (access R2)
R2	01	(0)	used for absolute address mode
R2	10	0x0004	constant +4
R2	11	0x0008	constant +8
R3	00	0x0000	constant 0
R3	01	0x0001	constant +1
R3	10	0x0002	constant +2
R3	11	0xFFFF	constant -1

The constant generator advantages are:

No special instructions required
No additional code word for the six constants
No code memory access required to retrieve the constant

The assembler uses the constant generator automatically if one of the six constants is used as an immediate source operand. Registers R2 and R3, used in the constant mode, cannot be addressed explicitly; they act as source-only registers.

6.3.5 General-Purpose Register R4 - R15

The twelve registers, R4-R15, are general-purpose registers. All of these registers can be used as data registers or address pointers and can be used with byte or word instructions.

6.4 Addressing Modes

Seven addressing modes for the source operand and four addressing modes for the destination operand can address the complete address space with no exceptions. The bit numbers in the table below describe the contents of the As (source) and Ad (destination) mode bits.

As/Ad	Addressing Mode	Syntax	Description
00/0	Register mode	Rn	Register contents are operand
01/1	Indexed mode	X(Rn)	(Rn + X) point to the operand. X is stored in the next word.
01/1	Symbolic mode	ADDR	(Rn + X) point to the operand. X is stored in the next word. Indexed mode X(PC) is used.
01/1	Absolute mode	&ADDR	(Rn + X) point to the operand. X is stored in the next word. Indexed mode X(0) is used.
10/-	Indirect Register mode	@Rn	Rn is used as a pointer to the
11/-	Indirect auto increment	@Rn+	Rn is used as a pointer to the operand. Rn is incremented afterwards by 1 for .B instructions and by 2 for .W instructions
11/-	Immediate mode	#N	The word following the instruction contains the immediate constant N. Indirect auto-increment mode @PC+ is used.

6.5 EL16 Instruction Set

The complete EL16 instruction set consists of 27 instructions. There are three instruction formats:

- Dual-operand
- Single-operand
- Jump

All dual-operand and single-operand instructions can be byte or word instructions by using .B or .W extensions. Byte instructions are used to access byte data. Word instructions are used to access word data. If no explicit extension is used, the instruction is a word instruction.

The source and destination of an instruction are defined by the following fields:

Abbr.	Description
src	The source operand defined by As and S-reg
dst	The destination operand defined by Ad and D-reg
As	The addressing bits responsible for the addressing mode used for the source (src)
S-reg	The working register used for the source (src)
Ad	The addressing bits responsible for the addressing mode used for the destination (dst)
D-reg	The working register used for the destination (dst)
B/W	Byte or word operation: 0: word operation, 1: byte operation

The following tables shows coding of the 16 bit op-code:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Mnemonic
0	0	0	0	0	0											--
0	0	0	1	0	0	0	0	0	0	Ad/As		D-Reg/S-Reg				RRC
						0	0	0	1							RRC.B
						0	0	1	0							SWP.B
						0	0	1	1							---
						0	1	0	0							RRA
						0	1	0	1							RRA.B
						0	1	1	0							SXT
						0	1	1	1							---
						1	0	0	0							PUSH
						1	0	0	1							PUSH.B
						1	0	1	0							CALL
						1	0	1	1							---
						1	1	0	0							RETI
						1	1	0	1							---
						1	1	1	0							---
						1	1	1	1							---
0	0	0	1	0	1											---
				1	0											---
				1	1											---
0	0	1	0	0	0	10-Bit PC Offset										JNZ / JNE
			0	0	1											JZ / JEQ
			0	1	0											JNC / JLO
			0	1	1											JC / JHS
			1	0	0											JN
			1	0	1											JGE
			1	1	0											JL
			1	1	1											JMP
0	1	0	0	S-Reg				Ad	B/W	As		D-Reg				MOV
0	1	0	1													ADD
0	1	1	0													ADDC
0	1	1	1													SUBC
1	0	0	0													SUB
1	0	0	1													CMP
1	0	1	0													DADD
1	0	1	1													BIT
1	1	0	0													BIC
1	1	0	1													BIS
1	1	1	0													XOR
1	1	1	1													AND

Figure 14. Coding of the 16 bit op-code

The table below shows a list of all instructions::

Mnemonic	Parameters	Description		V	N	Z	C
ADC(.B)**	dst	Add C to destination	dst + C -> dst	*	*	*	*
ADD(.B)	src, dst	Add source to destination	src + dst -> dst	*	*	*	*
ADDC(.B)	src, dst	Add source to C and destination	src + dst + C -> dst	*	*	*	*
AND(.B)	src, dst	AND source and destination	src AND dst -> dst	0	*	*	*
BIC(.B)	src, dst	Clear bits in destination	NOT(src) AND dst -> dst	-	-	-	-
BIS(.B)	src, dst	Set bits in destination	src OR dst -> dst	-	-	-	-
BIT(.B)	src, dst	Test bits in destination	src AND dst	0	*	*	*
BR	dst	Branch to destination	dst -> PC	-	-	-	-
CALL	dst	Call destination	SP-2 -> SP, PC+2 -> @SP, dst -> PC	-	-	-	-
CLR (.B)**	dst	Clear destination 0	0 -> dst	-	-	-	-
CLRC**	---	Clear C 0	0 -> C	-	-	-	0
CLRN**	---	Clear N 0	0 -> N	-	0	-	-
CLRZ**	---	Clear Z 0	0 -> Z	-	-	0	-
CMP (.B)	src, dst	Compare source and destination	dst - src	*	*	*	*
DADC (.B)**	dst	Add C decimally to destination	dst + C -> dst	0	*	*	*
DADD (.B)	src, dst	Add source and C decimally to destination	src + dst + C -> dst	0	*	*	*
DEC (.B)**	dst	Decrement destination	dst -1 -> dst	*	*	*	*
DECD (.B)**	dst	Double decrement destination	dst -2 -> dst	*	*	*	*
DINT**	---	Disable interrupts 0	0 -> GIE	-	-	-	-
EINT**	---	Enable interrupts 1	1 -> GIE	-	-	-	-
INC (.B)	dst	Increment destination	dst +1 -> dst	*	*	*	*
INCD (.B)**	dst	Double increment destination	dst +2 -> dst	*	*	*	*
INV (.B)**	dst	Invert destination	NOT(dst) -> dst	*	*	*	*
JC / JHS	label	Jump if C set / Jump if higher or same	if (condition) PC + 2 * offset -> PC	-	-	-	-
JZ / JEQ	label	Jump if Z set / Jump if equal	if (condition) PC + 2 * offset -> PC	-	-	-	-
JGE	label	Jump if greater or equal	if (condition) PC + 2 * offset -> PC	-	-	-	-
JL	label	Jump if less	if (condition) PC + 2 * offset -> PC	-	-	-	-
JMP	label	Jump	PC + 2 * offset -> PC	-	-	-	-
JN	label	Jump if N set / Jump if negative	if (condition) PC + 2 * offset -> PC	-	-	-	-
JNC /JLO	label	Jump if C not set / Jump if lower	if (condition) PC + 2 * offset -> PC	-	-	-	-
JNZ / JNE	label	Jump if Z not set / Jump if equal	if (condition) PC + 2 * offset -> PC	-	-	-	-
MOV (.B)	src, dst	Move source to destination	src -> dst	-	-	-	-
NOP	---	No operation	---	-	-	-	-
POP (.B)**	dst	Pop item from stack to destination	@SP+ -> dst	-	-	-	-
PUSH (.B)	src	Push source onto stack	SP -2 -> SP, src -> SP	-	-	-	-
RET**	---	Return from subroutine	@SP -> PC	-	-	-	-
RETI	---	Return from interrupt	@SP -> SR, @SP+ -> PC	*	*	*	*
RLA (.B)**	dst	Rotate left arithmetically	dst * 2 -> dst	*	*	*	*
RLC (.B)**	dst	Rotate left through C	dst * 2 -> dst, C -> LSB(dst)	*	*	*	*
RRA (.B)	dst	Rotate right arithmetically	dst / 2 -> dst	0	*	*	*
RRC (.B)	dst	Rotate right through C	dst / 2 -> dst, C -> MSB(dst)	0	*	*	*
SBC (.B)**	dst	Subtract not(C) from destination	dst + NOT(0) + C -> dst	*	*	*	*
SETC**	---	Set C	1 -> C	-	-	-	1
SETN**	---	Set N	1 -> N	-	1	-	-
SETZ**	---	Set Z	1 -> Z	-	-	1	-
SUB (.B)	src, dst	subtract source from destination	dst + NOT(src) + 1 -> dst	*	*	*	*
SUBC (.B)**	src, dst	subtract source and not(C) from destination	dst + NOT(src) + C -> dst	*	*	*	*
SWPB	dst	Swap bytes	---	-	-	-	-
SXT	dst	Extend sign	---	0	*	*	*
TST (.B)**	dst	Test destination	dst + NOT (0) + 1	0	*	*	1
XOR(.B)	src, dst	Exclusive OR source and destination	src XOR dst -> dst	*	*	*	*

** emulated instruction

Figure 15. Instruction Set of EL16

6.5.1 EL16 Instruction Cycle Counts

command type	operation	cycles	cycles(dreg==PC)
MOV DOUBLE	sreg -> dreg sreg x dreg -> dreg	1 1	2 2
MOV DOUBLE	sreg -> Y(dreg) -> dreg sreg x Y(dreg) -> Ydreg	3 4	--
MOV DOUBLE	@sreg -> dreg @sreg x dreg -> dreg	2 2	3 3
MOV DOUBLE	@sreg -> Y(dreg) -> dreg @sreg x Y(dreg) -> Ydreg	4 5	--
MOV DOUBLE	@sreg+ -> dreg @sreg+ x dreg -> dreg	2 2	3 3
MOV DOUBLE	@sreg+ -> Y(dreg) -> dreg @sreg+ x Y(dreg) -> Ydreg	4 5	---
MOV DOUBLE	Xsreg+ -> dreg Xsreg+ x dreg -> dreg	3 3	4 4
MOV DOUBLE	Xsreg+ -> Y(dreg) -> dreg Xsreg+ x Y(dreg) -> Ydreg	5 6	---
SINGLE SINGLE SINGLE SINGLE	dreg @dreg @dreg+ Y(dreg)	--- --- --- ---	2 --- --- ---
JUMP RETI IRCQ	--- --- ---	2 3 4	--- --- ---
PUSH PUSH PUSH PUSH	reg @reg @reg+ X(reg)	3 4 4 5	--- --- --- ---
CALL CALL CALL CALL	reg @reg @reg+ X(reg)	3 4 4 5	--- --- --- ---

Figure 16. EL16 Instruction Cycle Counts

SINGLE includes RRC, RRA, SWPB and SXT
DOUBLE includes all double operand instructions except MOV

6.6 Memory Description

6.6.1 Memory Map

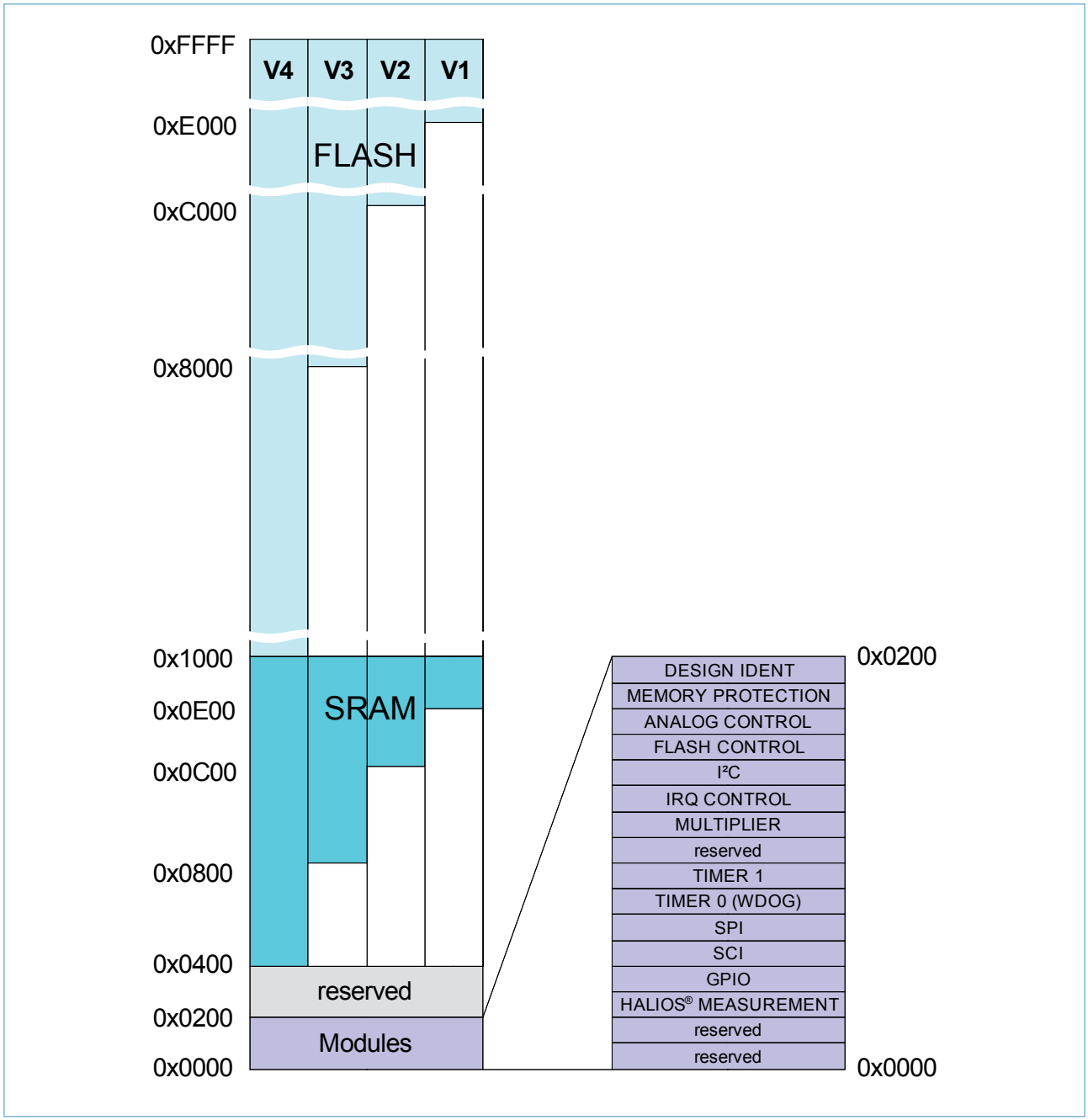


Figure 17. Memory Map

6.6.2 Base Address Table

Base address	Size	Module name
0x1000	0xF000	FLASH address
0x0400	0x0C00	SRAM address
0x0200	0x0200	reserved
0x01E0	0x0020	Design Ident Module
0x01C0	0x0020	Memory Protection Module
0x01A0	0x0020	Analog Control Module
0x0180	0x0020	FLASH Control Module
0x0160	0x0020	I²C Interface
0x0140	0x0020	Interrupt Control Module
0x0120	0x0020	Multiplier Module
0x0100	0x0020	reserved
0x00E0	0x0020	Timer 1
0x00C0	0x0020	Timer 0 (Window-Watchdog)
0x00A0	0x0020	SPI Module
0x0080	0x0020	LIN-SCI Module
0x0060	0x0020	GPIO Module
0x0040	0x0020	HALIOS® Interface
0x0020	0x0020	reserved
0x0000	0x0020	reserved

The differences in base addresses for the 3 additional devices of the EL16H6 versions are described in the tables below.

Base address	Size	Module name
0x8000	0x8000	FLASH
0x1000	0x7000	reserved
0x0800	0x0800	SRAM
0x0400	0x0400	reserved

Base address	Size	Module name
0xC000	0x4000	FLASH
0x1000	0x3000	reserved
0x0C00	0x0400	SRAM
0x0400	0x0800	reserved

Base address	Size	Module name
0xE000	0x2000	FLASH
0x1000	0xD000	reserved
0x0E00	0x0200	SRAM
0x0400	0x0A00	reserved

6.6.3 FLASH EL

- Main block size: up to 30K x 22 bit (60Kbyte) CRC protected
  - V4: 120 pages (60KByte)
  - V3: 64 pages (32KByte)
  - V2: 32 pages (16KByte)
  - V1: 16 pages (8KByte)
  - 256 words per page
  - 8 rows per page -> 32 words per row
  - Page erase support
- See TSMC FLASH documentation for timing details
  - 20 ms page erase
  - 200 ms mass erase
  - About 30 µs programming time per word

FLASH CRC calculation

- CRC polynomial: $x^6 + x^4 + x^3 + x^2 + x^1 + 1$
- Hamming distance: 4 (1 bit error correctable, 2 bit errors detectable)
- Erased FLASH words will cause an uncorrectable bit error when read, which asserts a reset

6.6.4 SRAM EL

- Size: up to 1.5K x 18Bit (3KByte)
  - V4: 3KByte
  - V3: 2KByte
  - V2: 1KByte
  - V1: 512Byte
- Byte write enable support
- Each byte is extended by a parity bit

6.7 Design Ident Module

The Design Ident Module of the EL16H6 contains following information:

- Design Ident (split into 4x16 bit words), a unique number which identifies every single device
- Design Version Code

All information are read only.

6.7.1 Design Ident Module Registers

Register Name	Address	Description
Design Ident 0	0x00	
Design Ident 1	0x02	
Design Ident 2	0x04	
Design Ident 3	0x06	
Version	0x08	

Register Design Ident 0 (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : Design Ident 0															

Register Design Ident 1 (0x02)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : Design Ident 1															

Register Design Ident 2 (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : Design Ident 2															

Register Design Ident 3 (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : Design Ident 3															

Register Version (0x08)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : Design Version Code V1 - 0x0000 V2 - 0x0025 V3 - 0x001A V4 - 0x003F															

6.8 Memory Protection Module

- Op-code execute area configuration (granularity: 1KByte, 64 areas)
- Stack area configuration (granularity: 256Byte, 12 areas)
- Invalid module register address handling

NOTE: In versions smaller then EL16H6V4 activation of non existent memory areas in Op-code Execute Enable Registers and Stack Enable Register have no effect.

6.8.1 Memory Protection Module Registers

Register Name	Address	Description
Op-code execute enable 0	0x00	
Op-code execute enable 1	0x02	
Op-code execute enable 2	0x04	
Op-code execute enable 3	0x06	
Failure address value	0x08	
Stack enable	0x0A	
Invalid address value	0x0C	
Interrupt clear	0x0E	

Register op-code execute enable 0 (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : area 0x3000 to 0x3FFE ... : ... **1** : area 0x0400 to 0x07FE **0** : area 0x0000 to 0x03FE enable 0 - execution of op-code denied 1 - execution of op-code allowed area size: 1 KByte reset value: 0xFFF0															

Register op-code execute enable 1 (0x02)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : area 0x7000 to 0x7FFE ... : ... **1** : area 0x4400 to 0x47FE **0** : area 0x4000 to 0x43FE enable 0 - execution of op-code denied 1 - execution of op-code allowed area size: 1 KByte reset value: 0xFFFF															

Register op-code execute enable 2 (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : area 0xB000 to 0xBFFE ... : ... **1** : area 0x8400 to 0x87FE **0** : area 0x8000 to 0x83FE enable 0 - execution of op-code denied 1 - execution of op-code allowed area size: 1 KByte reset value: 0xFFFF															

Register op-code execute enable 3 (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : area 0xF000 to 0xFFFE ... : ... **1** : area 0xC400 to 0xC7FE **0** : area 0xC000 to 0xC3FE enable 0 - execution of op-code denied 1 - execution of op-code allowed area size: 1 KByte reset value: 0xFFFF															

Register failure address value (0x08)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : address of last detected failure (execute protection, stack protection, misaligned 16 bit access, undefined op-code) reset value: 0x0000															

Register stack enable (0x0A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**11** : area 0x0F00 to 0x0FFE to **1** : area 0x0500 to 0x05FE **0** : area 0x0400 to 0x04FE reset value: 0x0FFF															

Register invalid address value (0x0C))

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : address of last invalid module register access reset value: 0x0000															

Register interrupt clear (0x0E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access												W	W	W	W	W
External access												W	W	W	W	W
Bit Description	**4** : undefined op-code IRQ clear (address of undefined op-code can be obtained by looking to the return address stored in stack minus - 2) 0 - no influence 1 - clear interrupt **3** : misaligned 16 bit access IRQ clear 0 - no influence 1 - clear interrupt **2** : invalid address IRQ clear 0 - no influence 1 - clear interrupt **1** : stack protection IRQ clear 0 - no influence 1 - clear interrupt **0** : execute protection IRQ clear 0 - no influence 1 - clear interrupt															

6.9 Analog Control Module

- Controls clock and reset generator (CRG)

6.9.1 Analog Control Module Registers

Register Name	Address	Description
Wake-up timer config	0x00	
Reset source status	0x0C	
Reset source status clear	0x0E	
Wake-up timer interrupt status	0x14	
Wake-up timer interrupt clear	0x16	

Register wake-up timer config (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5, will always be read as 0x96 **4** : enable timer 0 - timer off 1 - timer on **3:0** : timer value: timer period = 2 ms * [timer value + 1], with timer value 0...15 reset value: 0x0010															

Register reset source status (0x0C)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15** : level of incoming external reset signal (NRST) **8** : Trap -> masked interrupt event occurred (interrupt number 0 and 1) **7** : RAM parity error **6** : FLASH uncorrectable bit error **5** : CPU register parity error **4** : watchdog reset **1** : external reset **0** : power on reset / supply observe / trim register ECC error reset value: 0x0000															

Register reset source status clear (0x0E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access																W
External access																W
Bit Description	**0** : clears all reset status bits 0 - no influence 1 - clears all reset status bits															

Register wake-up timer interrupt status (0x14)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**0** : wake-up timer interrupt status 0 - no interrupt 1 - interrupt was asserted reset value: 0x0000															

Register wake-up timer interrupt clear (0x16)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access																W
External access																W
Bit Description	**0** : timer IRQ clear 0 - no influence 1 - clear interrupt															

6.10 FLASH Control Module

6.10.1 FLASH Control Module Registers

NOTE: In versions smaller then V4 activation of non existent memory areas in Area Protection Registers have no effect.

Register Name	Address	Description
Area protection (areas 0 - 7)	0x00	
Area protection (areas 8 - 14)	0x02	
Mode	0x04	
Status	0x06	
IRQ clear	0x08	
Bit error corrected address	0x0C	
Word config	0x0E	
Frequency config	0x10	

Register area protection (areas 0 - 7) (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **7:0** : writable 0 - area protected 1 - area writable areas 0 - 7 are FLASH main block areas (each 4 Kbyte) area 0: 0x1000 - 0x1FFF area 7: 0x8000 - 0x8FFF reset value: 0x9600															

Register area protection (areas 8 - 14) (0x02)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **6:0** : writable 0 - area protected 1 - area writable areas 8 - 14 are FLASH main block areas (each 4 Kbyte) area 8: 0x9000 - 0x9FFF area 14: 0xF000 - 0xFFFF reset value: 0x9600															

Register mode (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **7:0** : mode 0x01 - main block read 0x04 - main block program 0x10 - erase main block page 0x40 - mass erase main block . : every over written mode value results in "main block read" mode . : program/erase modes: write access to appropriate flash address starts program / erase cycle (see busy flag of status register, consider word config and row programming incomplete flag in program mode) -> Program/Erase Mode FSM reset value: 0x9600															

Register status (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**3** : bit error corrected bit error detected and corrected this bit is cleared by bit error corrected IRQ clear **2** : write error unexpected FLASH write access this bit is cleared by write error IRQ clear **1** : row programming incomplete current number of programmed row words != word config (see below) 0 : busy 0 - ready 1 - busy (program or erase is still in progress) reset value: 0x0002															

Register IRQ clear (0x08)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access															W	W
External access															W	W
Bit Description	**1** : bit error detected IRQ clear 0 - no influence 1 - clear interrupt **0** : write error IRQ clear 0 - no influence 1 - clear interrupt Note: A write error interrupt handler which is asserted on a bad write access during FLASH erase or program should be located in RAM because FLASH content may not be readable during these operations.															

Register bit error corrected address (0x0C)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : address of last correctable flash bit error reset value: 0x0000															

Register word config (0x0E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	0	0	1	0	1	1	0	0	0	0	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **4:0** : number of words to program within row 0: 1 word 1: 2 words ... 31: 32 words (default, a complete row) reset value: 0x961F															

Register frequency config (0x10)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **1:0** : system frequency config to get a correct erase and program timing 0: system frequency is 8 MHz (default) 1: system frequency is 16 MHz 2: system frequency is 24 MHz 3: system frequency is 32 MHz reset value: 0x9600															

6.10.1.1 Program/Erase Mode FSM

Principle mechanism of program and erase cycles is illustrated by the FSM.

Note: Execution of program code located in Flash memory strictly requires "main block read" mode. When switching to other Flash modes (program or erase) the user has to ensure that during this time code is executed in RAM. Before returning to code in Flash, mode has to be switched back to "main block read".

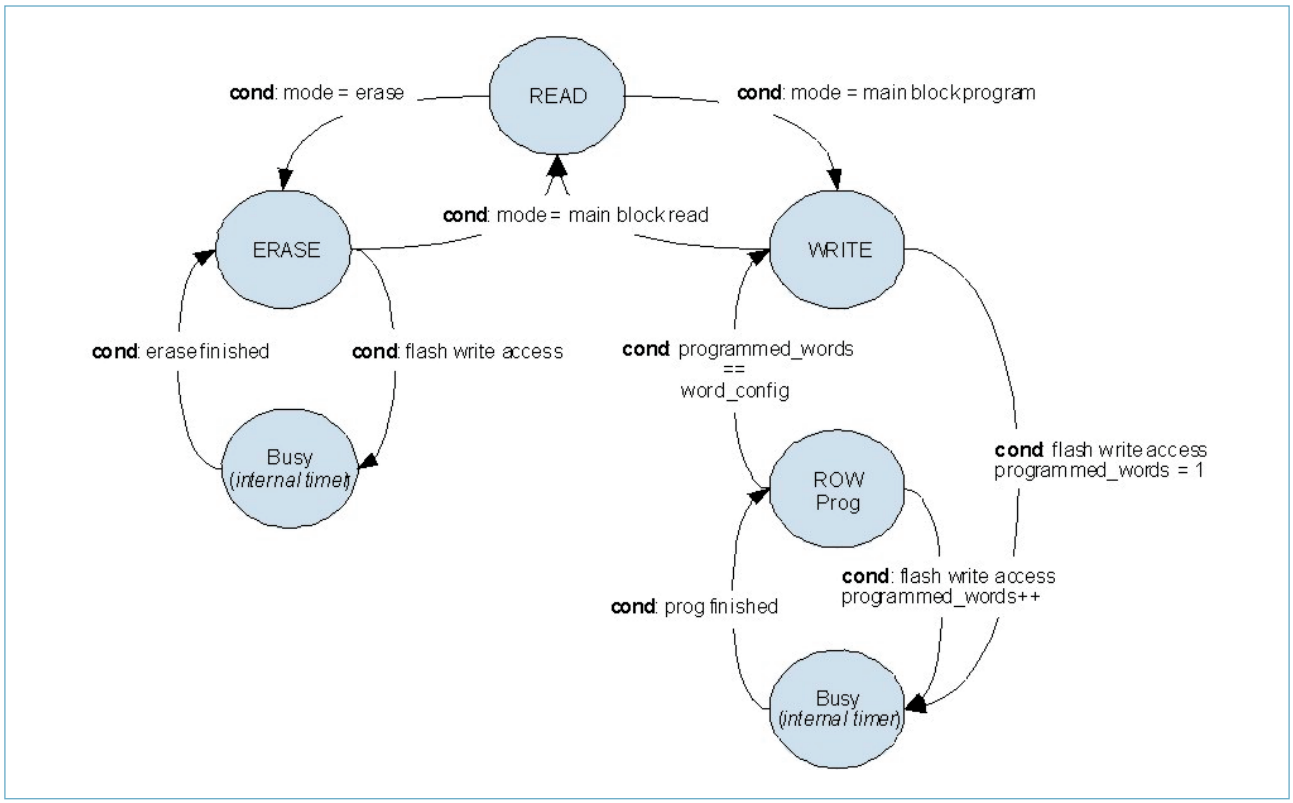


Figure 18. FSM: Program/Erase Cycle

6.11 I²C Interface

6.11.1 I²C Block Diagram

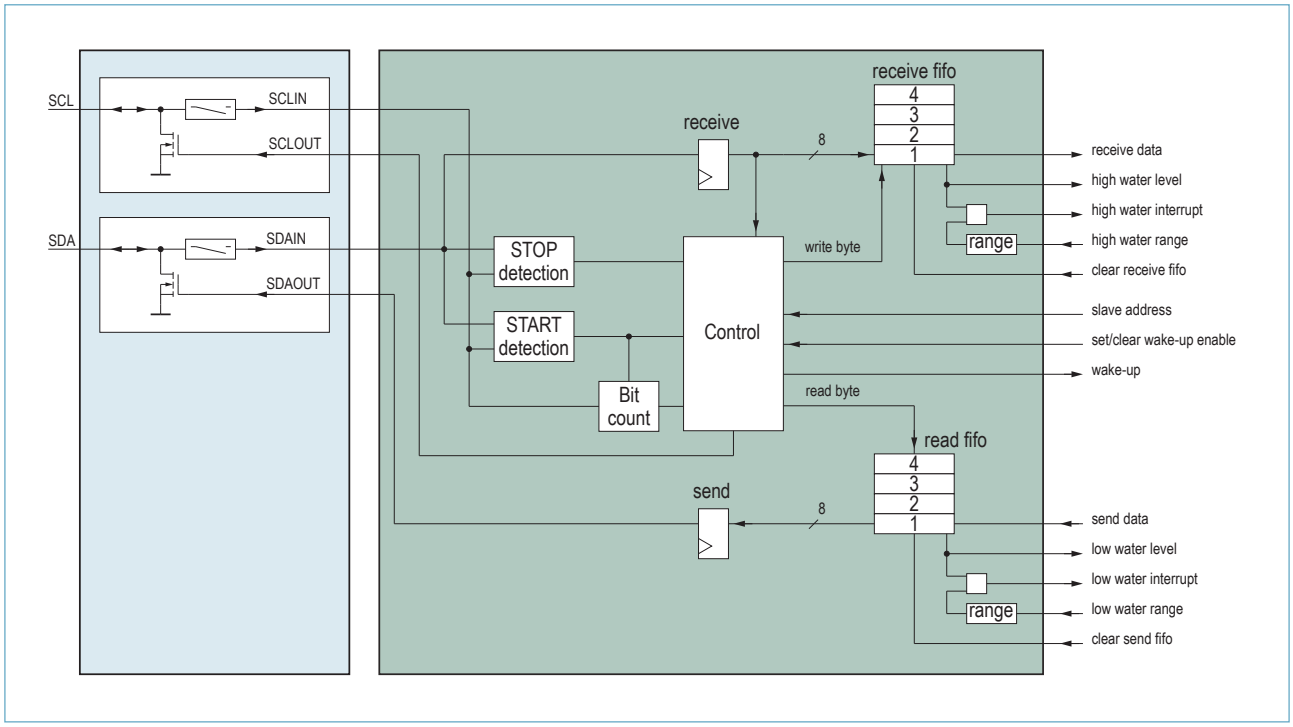


Figure 19. I²C Block Diagram

6.11.2 I²C Function

The I²C slave interface operates in 7 bit addressing mode with a maximum frequency of 400 kHz (fast mode). To synchronize the IC to different operation voltages of the I²C bus the interface has a separate supply voltage input at pin V_{DDIO} which is responsible for all interface pins. For more details of the addressing modes please refer to the "I²C - BUS SPECIFICATION VERSION 2.1" from Philips.

6.11.3 I²C Bus Timing Diagram

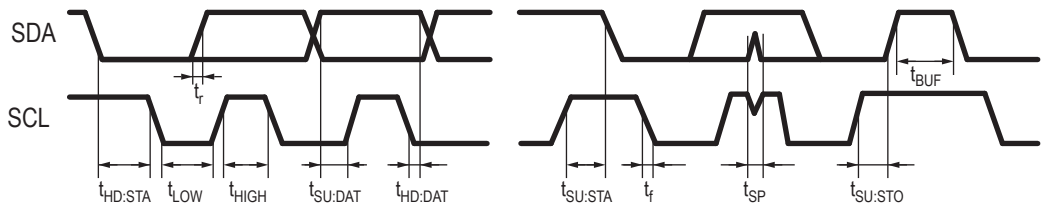


Figure 20. I²C Bus Timing Diagram

6.11.4 I²C Module Registers

Register Name	Address	Description
Receive Data FIFO Register	0x00	
Send Data FIFO Register	0x02	
Control Register	0x04	
Status Register	0x06	

Register Receive Data FIFO Register (0x00)

	MSB							LSB
Content	7:0							
Reset value	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R
Bit Description	**7:0** : receive data (see Data FIFO Registers for details)							

Register Send Data FIFO Register (0x02)

	MSB							LSB
Content	7:0							
Reset value								
Internal access	W	W	W	W	W	W	W	W
External access	W	W	W	W	W	W	W	W
Bit Description	**7:0** : send data (see Data FIFO Registers for details)							

Register Control Register (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Internal access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
External access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit Description	**13** : Clear contents of send FIFO registers 0 - read 1 - write **12** : Clear contents of receive FIFO registers 0 - read 1 - write **11** : Clear wake-up mode enable bit (see description below) 0 - read 1 - write **10** : Set wake-up mode enable bit (see description below) 0 - read 1 - write **9:8** : Slave address "00" - $58 (reset value) "01" - $59 "10" - $5A "11" - $5B **6:4** : High water range for receive FIFO (range 0....4) **2:0** : Low water range for send FIFO (range 0....4)															

Register Status Register (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	8 : Wake-up mode enable bit 0 - wake-up mode disabled 1 - wake-up mode enabled **6:4** : Fill level of receive FIFO **2:0** : Fill level of send FIFO															

6.11.5 Data FIFO Registers

Receive Data FIFO Registers:

The data received from the master is stored in the receive FIFO registers and has a depth of 4. The current fill level can be read in the status register. If the FIFO is completely filled up and another byte should be received the interface will force the master into a wait state until the application software reads one byte from the FIFO.

Send Data FIFO Registers:

The master reads data that is stored in the send FIFO registers. This FIFO buffer has a depth of 4 registers. The current fill level can be read in the status register. If the FIFO is empty and a byte is requested by the master the interface will force the master into a wait state until the application software writes one byte to the FIFO.

6.11.6 Interrupt Handling

I²C receive command (see List Of All Interrupts)

Command word pending in receive FIFO, this means the next byte read from the receive FIFO is the first received byte after the slave has been addressed. Depending on the application software this byte could be interpreted as a command. The interrupt flag is set back by reading a byte from the receive FIFO. The master will force the interface into a wait state until the application software reads one byte from the FIFO.

I²C send request (see List Of All Interrupts)

This flag signalizes that the master is requesting a byte but the send FIFO is empty. The interrupt flag is set back by writing a byte to the send FIFO. The master will force the interface into a wait state until the application software writes one byte to the FIFO.

I²C send FIFO low water (see List Of All Interrupts)

In case the low water mark (defined in control register) is reached or is exceeded the send FIFO low water flag becomes active. The flag is set back by filling to the send FIFO.

I²C receive FIFO high water (see List Of All Interrupts)

If the high water mark (defined in control register) is reached or is exceeded the receive FIFO high water flag becomes active. The flag is set back by reading from the receive FIFO.

6.11.7 I²C Wake-up Detection

The I²C interface can be used to wake up the IC from any system state. In system state "off" the interface has to be configured to wake the CPU Therefore the 'wake-up mode enable bit' has to be set (defined in control register) before setting the IC to "off-mode".

It is only possible to set the 'wake-up mode enable bit' if the I²C Master has closed the communication on the bus, so the application software has to poll the bit 'wake-up mode enable' (defined in status register) after it was set to make sure the bus is in idle state and the IC can be set to "off-mode".

After a new addressing of the slave on the bus the system will wake up from "off-mode" and the "I²C wake-up event" interrupt is active as long as the 'wake-up mode enable bit' is set back to zero (defined in control register). While the wake-up process the interface will force the Master into a wait state by holding the SCL line low. The application software has to clear the 'wake-up mode enable bit' (defined in control register) to release the SCL line in order to continue the communication.

6.12 Interrupt Control Module

6.12.1 Interrupt Control Module Structure

- Interrupt pending bit flip-flops (request hold elements) are located inside asserting modules
- Interrupt vector support for more simple and faster interrupt entry
- Fast vector based interrupt enable / disable
- Nested interrupt support
- FLASH based main interrupt vector
- Main interrupt enable MIE for easy cli() and sei() implementation
- N is the number of interrupt vectors

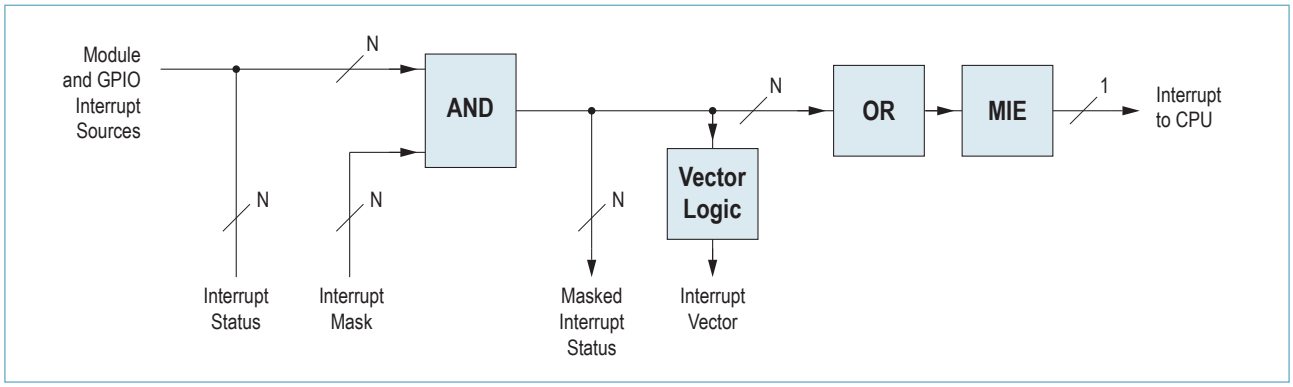


Figure 21. Interrupt control circuit

6.12.2 List Of All Interrupts

Vector Number	Interrupt Source	Priority
0	undefined op-code	highest
1	misaligned word access	
2	op-code execute protection error	
3	stack protection error	
4	invalid module register address access	
5	FLASH bit error corrected	
6	FLASH write error	
7	HALIOS® measurement ready	
8	timer0 window error (watchdog)	
9	timer1 event	
10	I2C receive command	
11	I2C send request	
12	I2C send FIFO low water	
13	I2C receive FIFO high water	
14	SPI timeout	
15	SPI FIFO error	
16	SPI receive high water	
17	SPI send low water	
18	SCI break received	
19	SCI measurement completed	
20	SCI receive full	
21	SCI transmit empty	
22	GPIO rising	
23	GPIO falling	
24	I2C wake-up event	
25	wake-up timer wake-up event	lowest

6.12.3 Interrupt Control Module Registers

Register Name	Address	Description
Interrupt mask	0x00	
Interrupt status	0x04	
Masked interrupt status	0x08	
Interrupt vector number	0x10	
Maximum interrupt level	0x14	
Main interrupt enable	0x16	
Interrupt enable	0x18	
Interrupt disable	0x1A	

Register interrupt mask (0x00)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**31:0** : mask (see List Of All Interrupts for details) 0 - disable 1 - enabled reset value: 0x0000.0000																															

Register interrupt status (0x04)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**31:0** : status (see List Of All Interrupts for details) 0 - not active 1 - active reset value: 0x0000.0000																															

Register masked interrupt status (0x08)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**31:0** : masked status (see List Of All Interrupts for details) 0 - not active 1 - active reset value: 0x0000.0000																															

Register interrupt vector number (0x10)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : number (see List Of All Interrupts for details) vector number of pending interrupt with highest priority (smallest vector number) when no interrupt is pending, vector will be 0xFFFF reset value: 0x0000															

Register maximum interrupt level (0x14)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**5:0** : level needed for nested interrupt support software writes current vector number to this register, so only interrupts with higher priority (lower vector number) can nest. reset value: 0x0020															

Register main interrupt enable (0x16)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit Description	**0** : MIE Main interrupt enable flag which can be used for easy implementation of cli() and sei() routines. reset value: 0x0001 **Note**: cli() usually must check (save current enable status) and then clear interrupt enable flag atomic (non interruptable). EL16 has no such operation, so GIE flag cannot be used. GIE should only be used for interrupt nesting. When MIE is only used inside cli() and sei(), cli() must not save current status, because MIE is always enabled on cli() entry.															

Register interrupt enable (0x18)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access												W	W	W	W	W
External access												W	W	W	W	W
Bit Description	**4:0** : set addressed enable bit in Interrupt Mask register to 1 vector number of interrupt to enable **Trap**: when a disabled interrupt 0 or 1 occurred a system reset will be generated															

Register interrupt disable (0x1A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access												W	W	W	W	W
External access												W	W	W	W	W
Bit Description	**4:0** : set addressed enable bit in Interrupt Mask register to 0 vector number of interrupt to disable															

6.13 Multiplier Module

The hardware multiplier is a peripheral and is not part of the EL16 CPU. This means, its activities do not interfere with the CPU activities. The multiplier registers are peripheral registers that are loaded and read with CPU instructions.

The hardware multiplier supports:

- Unsigned multiply
- Signed multiply
- Unsigned multiply accumulate
- Signed multiply accumulate
- 16 x 16 bits, 16 x 8 bits, 8 x 16 bits, 8 x 8 bits
- CPU is halted until result is valid (1 clock cycle)

The hardware multiplier supports unsigned multiply, signed multiply, unsigned multiply accumulate, and signed multiply accumulate operations. The type of operation is selected by the address the first operand is written to. The hardware multiplier has two 16-bit operand registers, OP1 and OP2, and three result registers, SumLo, SumHi, and SumExt. SumLo stores the low word of the result, SumHi stores the high word of the result, and SumExt stores information about the result.

6.13.1 Multiplier Module Registers

Register Name	Address	Description
MPY	0x10	
MPYS	0x12	
MAC	0x14	
MACS	0x16	
Operand 2	0x18	
SumLo	0x1A	
SumHi	0x1C	
SumExt	0x1E	

Register MPY (0x10)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 unsigned multiply reset value: 0x000															

Register MPYS (0x12)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 signed multiply reset value: 0x0000															

Register MAC (0x14)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 unsigned multiply accumulate reset value: 0x0000															

Register MACS (0x16)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 signed multiply accumulate reset value: 0x0000															

Register Operand 2 (0x18)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	15:0															
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 2 (write access starts multiplication) reset value: 0x0000															

Register SumLo (0x1A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : lower 16 bit of result reset value: 0x0000															

Register SumHi (0x1C)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : In case of operation: MPY: upper 16 bit of result MPYS: The MSB is the sign of the result. The remaining bits are the upper 15-bits of the result. Two's complement notation is used for the result. MAC: upper 16 bit of result MACS: Upper 16-bits of the result. Two's complement notation is used for the result. reset value: 0x0000															

Register SumExt (0x1E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : In case of operation: MPY: always 0x0000 MPYS: contains the extended sign of the result 0x0000 if result was positive 0xFFFF if result was negative MAC: contains the carry of the result 0x0000 no carry result 0x0001 result with carry MPYS: contains the extended sign of the result 0x0000 if result was positive 0xFFFF if result was negative reset value: 0x0000															

6.14 Timer 0 (Window-Watchdog) and Timer

- Two 32 bit wide decrementing timers
- Timer 0 is used as a window-watchdog, so it triggers a system reset instead of an interrupt when timer value = 0
- Window-watchdog timer is disabled after reset and has to be armed by software
- Window-watchdog cannot be disabled or changed when armed
- 16 times SCI Baud rate can be configured as timer1 clk base
- NOTE: watchdog will be halted during FLASH erase / program
- NOTE: watchdog and timer will be halted during debug CPU halt
- Window-watchdog generates an interrupt when watchdog is reset outside specified window (see diagram below)

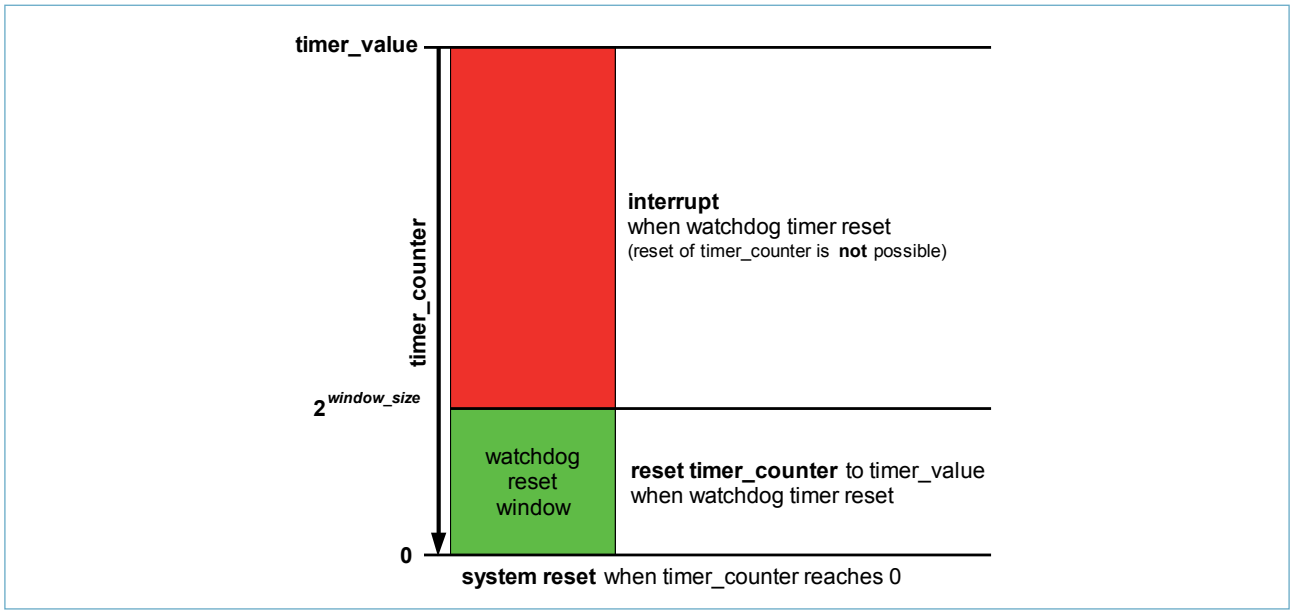


Figure 22. Window-Watchdog Timing

6.14.1 Timer 0 and Timer 1 Module Registers

Register Name	Address	Description
Timer value	0x00	
Timer counter	0x04	
Timer control	0x08	
Timer window config	0x0A	
Timer interrupt clear	0x0C	

Register timer value (0x00))

	MSB																													LSB
Content	31:0																													
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**31:0** : timer start value reset value: 0xFFFF.FFFF																													

Register timer counter (0x04)

	MSB																													LSB
Content	31:0																													
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**31:0** : timer start value reset value: 0xFFFF.FFFF																													

Register timer control (0x08)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	(R) W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	(R) W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **3** : clock base selector (timer 1 only) 0 - MCLK 1 – MCLK/(16*baud rate) synchronize timer to SPI clock **2** : timer reset 0 - no influence 1 - reset to start value **1** : loop 0 - run once and hold afterwards (clears "run enable") 1 - loop **0** : run enable 0 - timer stopped 1 - timer enabled reset value: 0x0000															

Register timer window config (0x0A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : Timer Window Config (only applicable for window-watchdog) password must be written as 0xA5 will always be read as 0x96 **5** : window enable 0 - no window (default) 1 - window active **4:0** : window size reset window is defined as: timer value < (2^window size - 1) reset value: 0x001F															

Register timer interrupt clear (0x0C)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access															W	W
External access															W	W
Bit Description	**1** : timer IRQ clear 0 - no influence 1 - clear interrupt **0** : window IRQ clear 0 - no influence 1 - clear interrupt															

6.15 SPI Module

- Can be used as master or slave
  - The SPI Interface consists of the following 4 signals:
  - SCK: SPI clock (driven by master)
  - CSB: low active chip select (driven by master)
  - MISO: master in, slave out (data from slave to master)
  - MOSI: master out, slave in (data from master to slave)
- Configurable phase, polarity and bit order
- Byte and multi-byte transfer support
- Slave mode SPI clock monitoring (timeout)
- 4 data word transmit and receive FIFOs

NOTE: Data will not be send as long as SPI interface is not routed to IO ports

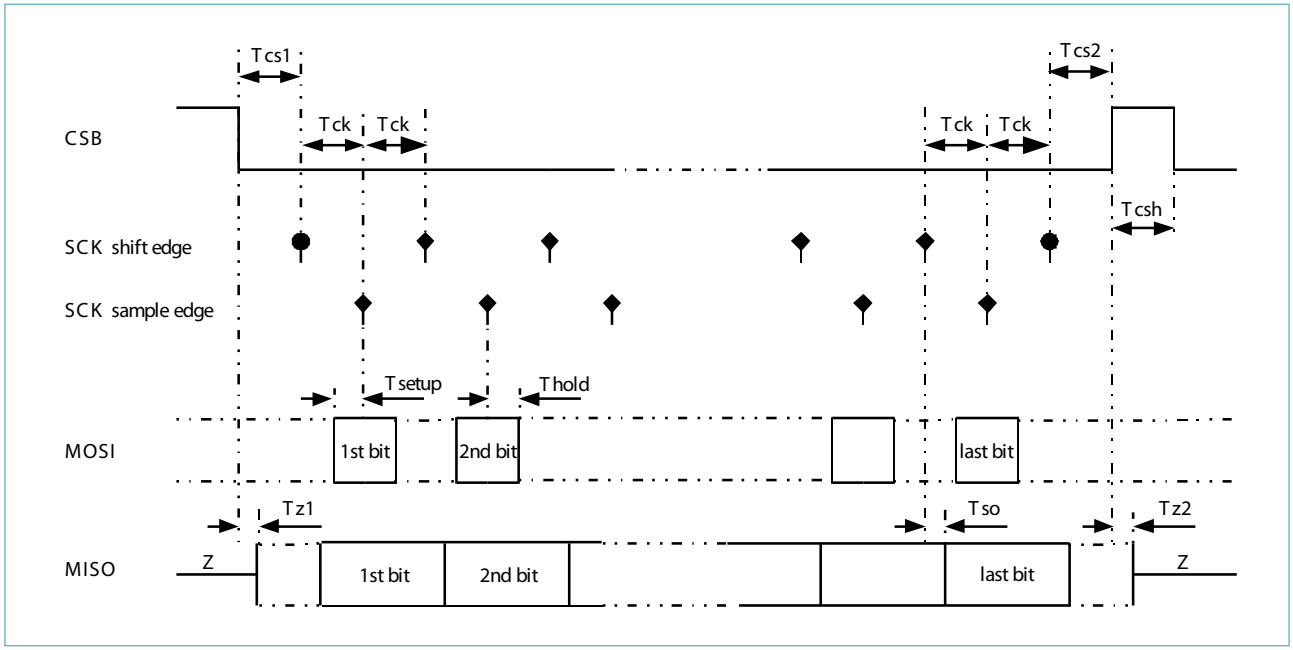


Figure 23. SPI Bus Timing Diagram

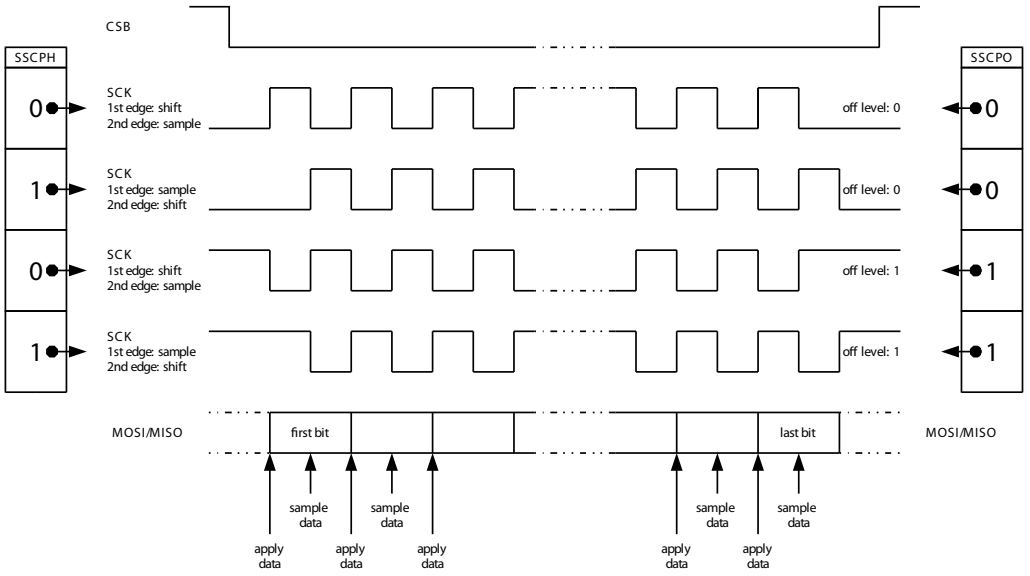


Figure 24. SPI Mode Diagram

6.15.1 SPI Module Registers

Register Name	Address	Description
Transmit data / receive data	0x00	
Control	0x02	
Baud config	0x04	
Timeout config	0x06	
Module reset	0x08	
Status	0x0A	
Error	0x0C	
Interrupt clear	0x0E	

Register transmit data / receive data (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	(R) W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	(R) W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**8** : csb control (only for data transition and in master mode) 0 - byte mode 1 - keep csb active after related byte was transmitted **7:0** : transmit data / receive data reset value: 0x0000 The 'send low water' interrupt will be cleared by writing a byte to the transmit data register (FIFO). The 'receive high water' interrupt will be cleared by reading a byte from the receive data register (FIFO). (see List Of All Interrupts)															

Register control (0x02)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
Internal access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
External access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	**14:12** : high water receive FIFO level interrupt will be asserted when receive FIFO fill level increases to this value default value: 2 **10:8** : low water transmit FIFO level interrupt will be asserted when transmit FIFO fill level decreases to this value default value: 0 **3** : slave 0 - master 1 - slave **2** : polarity: SSCPO, see SPI mode diagram 0 - clock off level 0 1 - clock off level 1 **1** : phase: SSCPH, see SPI mode diagram 0 - 1st edge shift, 2nd edge sample 1 - 1st edge sample, 2nd edge shift **0** : order 0 - LSB first 1 - MSB first															

Register baud config (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : baud divider = (system clock frequency) / (2 * baud rate) **NOTE**: Minimal value for baud divider is 4 reset value: 0x0004															

Register timeout config (0x06))

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : timeout value maximum allowed count of system clock cycles between 2 SPI clock edges reset value: 0xFFFF															

Register interrupt clear (0x8E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access															W	W
External access															W	W
Bit Description	**2** : SPI module reset **1** : receive FIFO clear **0** : transmit FIFO clear															

Register status (0x0A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**6:4** : receive FIFO level **2:0** : transmit FIFO level															

Table 70: Interrupt clear

Register error (0x0C))

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**1** : transmit FIFO was empty (only in slave mode) will be cleared on read **0** : receive FIFO was full (received data will be lost) will be cleared on read															

Register interrupt clear (0x0E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access															W	W
External access															W	W
Bit Description	**1** : clear error IRQ **0** : clear timeout IRQ															

6.16 LIN-SCI Module

- Full duplex operation
- 8N1 data format, standard mark/space NRZ format
- Extended baud rate selection options
- Interrupt-driven operation with four flags: receiver full, transmitter empty, measurement finished, break character received

Special LIN Support:

- 13 Bit break generation
- 11 Bit break detection threshold
- A fractional-divide baud rate prescaler that allows fine adjustment of the baud rate
- Measurement counter which has 16 bits and can be used as a mini-timer to measure break and bit times (baud rate recovery).
- Baud Measurement Results can directly be fed into the baud register to adjust the baud rate (Baud self-synchronization with SYNC byte)

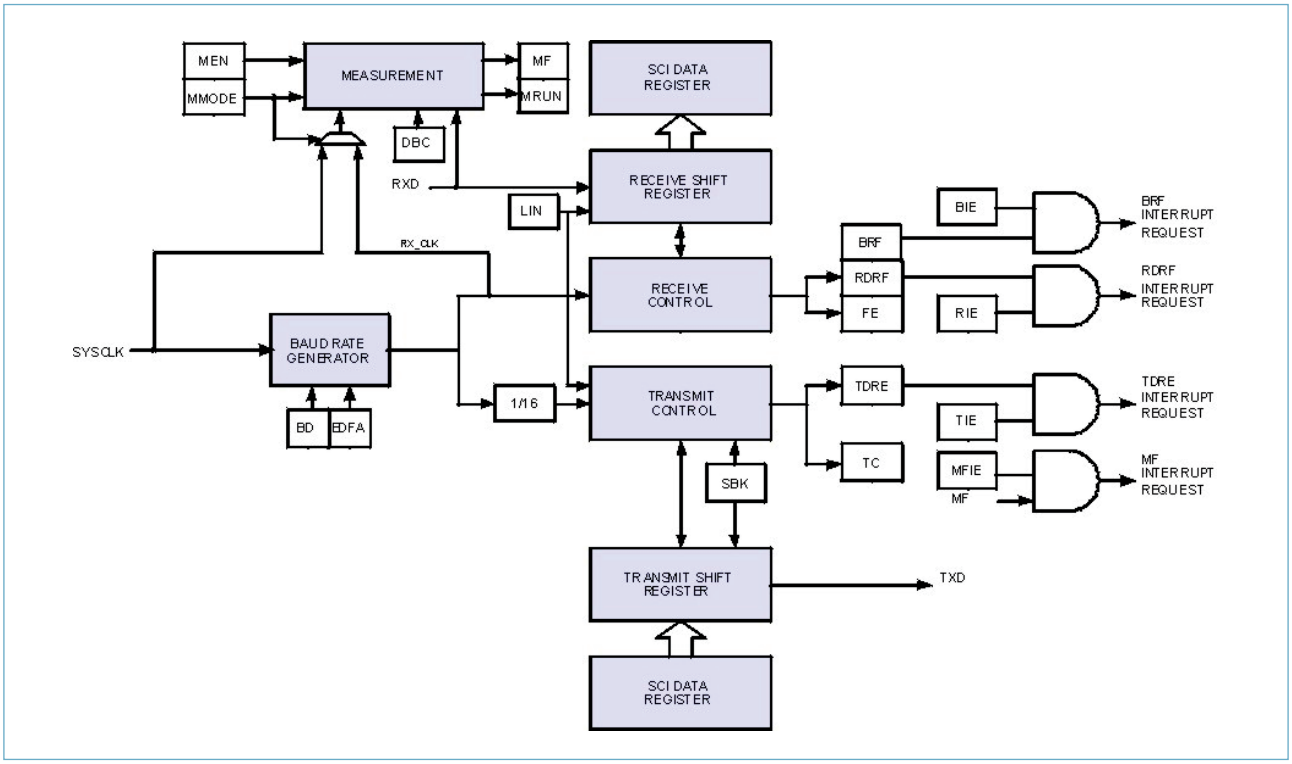


Figure 25. SCI block diagram

6.16.1 LIN-SCI Module Registers

Register Name	Address	Description
Sci baud rate	0x00	
Sci control	0x02	
Sci status	0x04	
Sci data (in/out)	0x06	
Sci measurement control	0x08	
Sci measurement counter	0x0A	

Register sci baud rate (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:5** : BD - SCI baud divisor select Divisor: 0x000 --> 1 (bypass divider) 0x001 --> 2 0x002 --> 3 ... 0x007 --> 8 ... **4:0** : BDFA - SCI baud divisor fine adjust These bits select the number of clocks inserted in each 32 output cycle frame to achieve more timing resolution on the average baud frequency shown in the following table. BDFA[00000] = 0/32 = 0 BDFA[00001] = 1/32 = 0.03125 BDFA[00010] = 2/32 = 0.0625 ... BDFA[10000] = 16/32 = 0.5 ... BDFA[11111] = 31/32 = 0.96875 reset value: 0x0000 The divider can be used to achieve divisor values between 1 and 2047.96875. The baud divisor fine adjust can be used to fine tune the baud rate in 1/32 steps of the divisor. Use the following formula to calculate the SCI baud rate: Baud Rate = clk_{sys}/(16*(BD+BDFA)) Note: The 16 bit baud divisor value represents the number of system clock cycles of two bit lengths. The result of a baud measurement (see measurement counter below) can directly be written to the baud rate register.															

Register sci control (0x02)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7** : TIE - TxD interrupt enable (generates interrupt when TDRE is set) **6** : LIN - LIN Mode: LIN break transmit enable (13 bit break symbol instead of 10 bit), LIN break receive detection enable (detects a 11 bit break symbol instead of 10 bit) **5** : RIE - RxD interrupt enable (generates interrupt when RDRF is set) **4** : BIE - break detection interrupt enable (generates interrupt when BRF is set) **3** : TE - transmitter enable If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE **2** : RE - receiver enable RE set to '0' suppresses start bit recognition, setting RE to '1' during an ongoing transfer can cause erroneous data reception and interrupt generation (RDRF) setting RE to '0' during an ongoing transfer can cause erroneous data reception and interrupt generation (RDRF), received data should be ignored **1** : MFIE - measurement finish interrupt enable (generates interrupt when MF is set) **0** : SBK - send break bit Toggling SBK sends one break character (10 logic 0s, respectively 13 logic 0s if LINT is set). Toggling implies clearing the SBK bit before the break character has finished transmitting. As long as SBK is set, the transmitter continues to send complete break characters (10 bits respectively 13 bit). reset value: 0x0000															

Register sci status (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**9** : AUTO_BAUD_TRIGGERED set when new Baud value was copied automatically to baud config register after a valid SNYC byte measurement (see also measurement control register -> AUTO_BAUD) cleared when reading the msb of the status word **8** : AUTO_MEAS_TRIGGERED set when measurement was started automatically after reception of a valid break (see also measurement control register -> AUTO_MEAS) cleared when reading the msb of the status word **7** : TDRE - transmit data register empty Clear TDRE by writing to sci data reg. Write will be ignored when transmit register is not empty -> check if TDRE = 1 before writing to transmit register **6** : TC - transmit complete flag TC is reset to '0' when a transmission is in progress **5** : RDRF - receive data register full flag Clear RDRF by reading sci status with RDRF set and then reading sci data reg NOTE: RDRF will be set: a) in case of data reception: 1/8 nominal bit length after the recognized stop bit, e.g. since the bits are sampled in the middle of a nominal bit length the flags and with it the irq will be set after the estimated end of the active stop bit. b) in case of break reception: see BRF description below **4** : BRF - break received flag (LIN-Mode dependent) Clear BRF by reading sci status with BRF set and then reading sci data reg. The BR flag will be set when the start bit is followed by 8 (respectively 9 when Lin Mode is set) logic 0 data bits and a logic 0 where the stop bit should be. When BRF is set also FE and RDRF will be set, the SCI data register will be cleared Note: flag generation (incl BRF) will be suppressed when AUTO_MEAS is set **3** : OV - receiver overrun detected Clear OV by reading sci status with OV set and then reading sci data reg. OV will be set when a received data byte is not read before the data byte of the next frame or a break character arrives. The second data byte will be disallowed **2** : MRUN - measurement running **1** : MF - measurement finish flag Clear MF by read accessing the measurement counter **0** : FE - framing error flag FE is set when the logic does not detect a logic 1 where the stop bit should be. FE will be set and reset together with RDRF reset value: 0x0000															

Register sci data (in/out) (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : sci data register, write for transmitting byte, read received byte reset value: 0x0000															

Register sci measurement control (0x08)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
External access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	**13:8** : DBC[6:1] - denounce filter threshold for baud rate measurement (MMODE=0) DBC[0] is always set to logic 1. DBC[6:0] form the upper threshold value for the denouncing filter. Denounce filter is reset to 81 which results in minimum filter delay of 81x62,5ns=5,1us@16MHz **3** : AUTO_BAUD automatically copy baud measurement result to baud config register after a valid baud measurement (expecting SYNC Byte) --> AUTO_BAUD_TRIGGERED will be set NOTE: During baud measurement the receiver is disabled an therefore no data will be received, only the measurement logic is active which will generate a measurement finish flag (configurable as interrupt) **2** : AUTO_MEAS automatically start a baud rate measurement after reception of a valid break --> AUTO_MEAS_TRIGGERED will be set NOTE: AUTO_MEAS mode suppresses the flag specific flag generation (see sci_status -> BRF) **1** : MMODE measurement mode select 0 -> baud rate measurement, counter runs with system clock and measures time between 4 falling edges (8 bit length are measured), bouncer is enabled Note: baud measurement expects a 0x55 data byte to measure, this is the SYNC byte in the LIN protocol 1 -> break time measurement, counter runs with 16 x baud rate, measures time when RxD line is zero NOTE: only applicable together with MEN control bit **0** : MEN - measurement enable Set to '1' to start a measurement When measurement is finished, MEN bit will be cleared automatically NOTE: When AUTO_MEAS bit is set MEN must not be used NOTE: Writing a '0' to MEN resets the measurement logic and allows a clean restart reset value: 0x2800																

Register sci measurement counter (0x0A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : MEASUREMENT COUNTER Counter is cleared by every start of a new measurement When the measurement counter overflows the counter value is saturated to 0xFFFF and the measurement will be stopped (MF flag set). The measurement should be repeated with an adapted baud rate setting. Note: In Baud measurement mode the result of the baud measurement (8 bit length) is divided by 4 and rounded (resulting 2 bit length value) the resulting 16 bit can be fed into the baud divider register to adjust the baud rate. reset value: 0x0000															

6.17 GPIO Module

- Up to 8 GPIOs (see IO Port Multiplexer table)
- Interrupt capable (configurable for positive and / or negative signal edge interrupt)

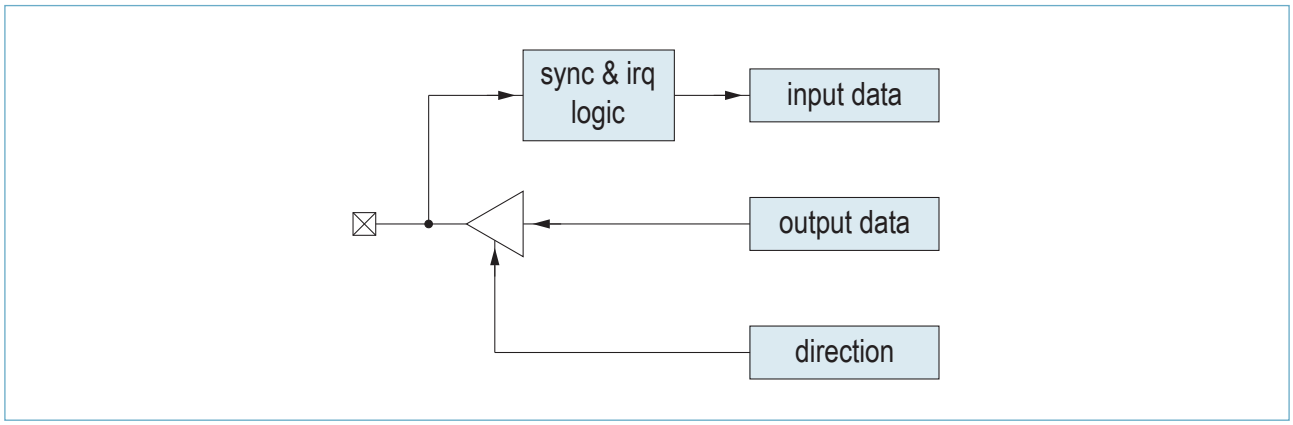


Figure 26. Principle io cell structure

6.17.1 GPIO Module Registers

Register Name	Address	Description
Output data	0x00	
Direction	0x02	
Input data	0x04	
Posedge interrupt enable	0x06	
Posedge interrupt status	0x08	
Posedge interrupt clear	0x0A	
Negedge interrupt enable	0x0C	
Negedge interrupt status	0x0E	
Negedge interrupt clear	0x10	
Port config	0x12	

Register output data (0x00)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : output data reset value: 0x0000															

Register direction (0x02)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : direction 0 - output, pull down disabled 1 - input, pull down enabled reset value: 0x00FF															

Register input data (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**7:0** : input data reset value: 0x0000															

Register posedge interrupt enable (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : enable 0 - disabled 1 - a positive edge on related "input data" bit will set interrupt bit reset value: 0x0000															

Register posedge interrupt clear (0x0A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access									W	W	W	W	W	W	W	W
External access									W	W	W	W	W	W	W	W
Bit Description	**7:0** : clear 0 - no influence 1 - clears related interrupt bit															

Register negedge interrupt enable (0x0C)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : enable 0 - disabled 1 - a negative edge on related "input data" bit will set interrupt bit reset value: 0x0000															

Register negedge interrupt status (0x0E)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**7:0** : status 0 - no interrupt 1 - interrupt was asserted reset value: 0x0000															

Register negedge interrupt clear (0x10)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value																
Internal access									W	W	W	W	W	W	W	W
External access									W	W	W	W	W	W	W	W
Bit Description	**7:0** : clear 0 - no influence 1 - clears related interrupt bit															

Register port config (0x12)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit Description	**1:0** : IO port config for details see IO Port Multiplexer reset value: 0x0000															

6.17.2 IO Port Multiplexer

IO Port	JTAG Debug TMODE=1	Normal Mode cfg[1:0]=00	Normal Mode cfg[1:0]=01	Normal Mode cfg[1:0]=10	Normal Mode cfg[1:0]=11
TMODE	1	0	0	0	0
IO0	GPIO00	GPIO00	GPIO00	GPIO00	GPIO00
IO1	GPIO01	GPIO01	GPIO01	GPIO01	GPIO01
IO2	GPIO02	GPIO02	TXD	GPIO02	TXD
IO3	GPIO03	GPIO03	RXD	GPIO03	RXD
IO4	TDO	GPIO04	GPIO04	SCK	SCK
IO5	TDI	GPIO05	GPIO05	MISO	MISO
IO6	TMS	GPIO06	GPIO06	MOSI	MOSI
IO7	TCK	GPIO07	GPIO07	CSB	CSB

7 Robustness

7.1 EMC

EMC qualification is performed on packaged device level.
Applied standards:
• Emission: IEC61967-2 (radiated, GTEM method) and IEC61967-4 (conducted, 150 Ohm method)
• Susceptibility: IEC62132-2 (radiated, GTEM method) and IEC62132-4 (conducted, DPI method)

7.2 ESD

The ESD protection circuitry is measured according to AEC-Q100-002 with the following conditions:

Test Method (HBM):
VIN = 2000 V (according to device class H1C)
REXT = 1500 Ohm
CEXT = 100 pF

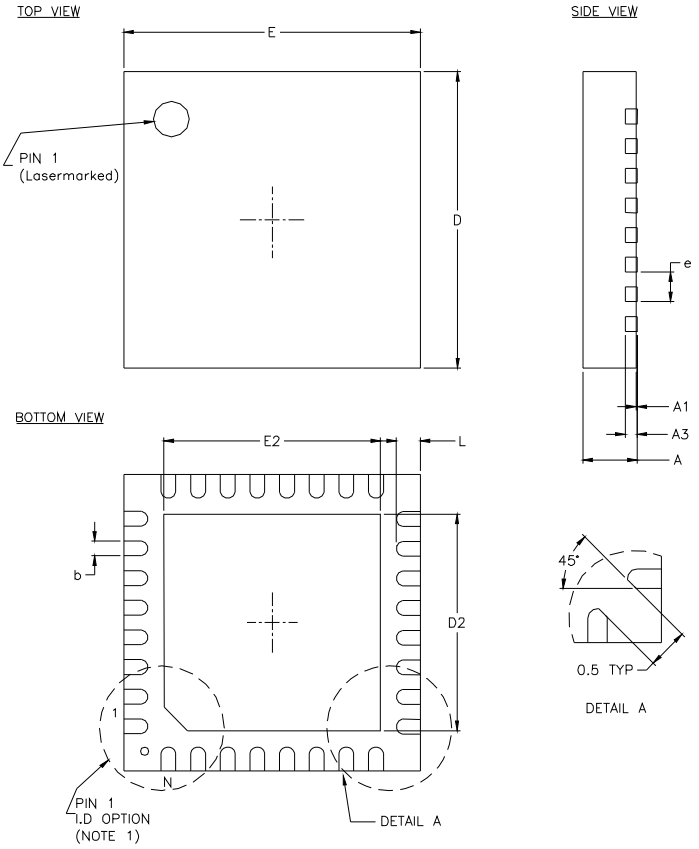
Test Method (CDM):
VIN = 500 V for all pins
VIN = 750 V for corner pins

7.3 Latch up Test

Test Method:
100 mA positive and negative pulses at 85 °C according to AEC-Q100-004.

8 Package Information

Package Outline and Dimensions are according JEDEC MO-220 K, variant VHHD-4



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.18	0.25	0.30	0.007	0.010	0.012
Package length / width	D / E	--	5.00 BSC	--	--	0.197 BSC	--
Length / width of exposed pad	D2 / E2	3.50	3.65	3.80	0.138	0.144	0.150
Lead pitch	e	--	0.5 BSC	--	--	0.02 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		32			32	

Note: the mm values are valid, the inch values contains rounding errors

9 Marking

9.1 Top Side

Elmos (Logo)
90906
YWW*#
XXXXU

Signature	Explanation
90906	Elmos project number
B	Elmos project revision code
Y	Year of assembly (e.g. 2014)
WW	Week of assembly
*	Mask revision code
#	Elmos internal code
XXXX	Production lot number (1 to 4 digits)
U	Assembler Code

10 Record of Revision

Chapter	Revision	Change and Reason for Change	Date	Released Elmos
-	.04	complete document revised	Feb 27, 2014	BR/ZOE
7.1	.05	new text	Mar 26, 2014	BR/ZOE

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