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THE DEVELOPMENT SYSTEMS COMPANY

Ashling Product Brief APB192

Ashling EVBA7 On-Board Emulator Support for Philips LPC211x/2x/92 64-pin and LPC22xx 144-pin Microcontrollers

1 Ashling support for Philips ARM7-core microcontrollers

Ashling supplies a range of debugging tools, trace systems and Development Kits for Philips' entire range of LPC2000-family ARM7-core Microcontrollers.

The EVBA7 Evaluation Board with On-Board JTAG Emulator (supplied with Ashling's ASK-2000, APK-2000 and DEVK-2000 Kits) is normally supplied with an LPC2106 48-pin device fitted. Ashling also supplies a range of Adapters for Philip's 64-pin LPC211x/212x/219x devices and 144-pin LPC22xx devices; if you plan to use an Adapter you should order Kits with the **–NP** option (No Processor fitted on the EVBA7 board).

2 Enabling LPC2000-family debug functions

Various members of the Philips LPC2000 use different methods to enable Debug (EmbeddedICE) and In-System Flash Programming (Flash Boot Programming) modes, as shown in Table 1; you must configure the EVBA7 On-Board Emulator and the Ashling Adapter to suit the device in use.

Device Family:	*LPC210x (48-pin)*	*LPC211x/212x/219x (64-pin), LPC22xx (144-pin)*
Enable debug:	If RTCK is (driven or floats) high when RST* goes high *and* DBGSEL is high, then Primary JTAG debug and ETM functions are enabled.	If P1.26 (RTCK) is pulled low when RST* goes high, then JTAG debug is enabled.
Enable ETM trace:	See Enable (primary) debug above.	If P1.20 (TRACESYNC) is pulled low when RST* goes high, then ETM trace function is enabled.
Enable In-System Flash Programming (ISP):	If P0.14 is pulled low when RST* goes high and remains low for at least 3ms thereafter, then ISP mode is enabled (P0.14 must be high at reset if ISP mode is *not* required).	If P0.14 is pulled low when RST* goes high and remains low for at least 3ms thereafter, then ISP mode is enabled (P0.14 must be high at reset if ISP mode is *not* required).
RTCK pin operation	Bidirectional, with internal pull-up. Functions as Input (HI = Primary JTAG) during Reset; after Reset, functions as Output (RTCK) pin.	Bidirectional, with internal pull-up. Functions as Input (LO = JTAG) during Reset; after Reset, functions as Output (P1.26/RTCK) pin. To enable JTAG debug, tie 4.7KΩ resistor from P1.26/RTCK to Ground.
TRACESYNC pin operation	Internal pull-up. Functions as TRACESYNC if Primary JTAG Debug and ETM are enabled; see above.	Bidirectional, with internal pull-up. Functions as Input (LO = ETM) during Reset. After Reset, functions as TRACESYNC Output pin if ETM is enabled. To enable ETM, tie 4.7KΩ resistor from P1.20/TRACESYNC to Ground.
P0.14 pin operation	High-impedance input at reset (no internal pull-up). Functions as ISP-enable input pin during Reset; after Reset, functions as P0.14 pin if ISP is not enabled.	Internal pull-up. Functions as ISP-enable input pin during Reset; after Reset, functions as P0.14 pin if ISP is not enabled.

Table 1: How to enable Debug, Trace and ISP functions on Philips' LPC2000-family devices

3 Using Ashling's Device Adapters for LPC211x/212x and LPC22xx

Figure 1 shows the Jumpers on Ashling's AD-EVBA7-LPC2129-64/FA-EVBA7-64 (for LPC211x/212x) and AD-EVBA7-LPC2292-144/FA-EVBA7-144-DR (for LPC22xx) Device Adapters. (Please note that Figure 1 does *not* apply to Ashling's AD-CA064QFP-J2J3PS/PA-EVBA7-64 or AD-CA144QFP-J2J3PS/PA-EVBA7-144 Programming Socket Adapters; see later).

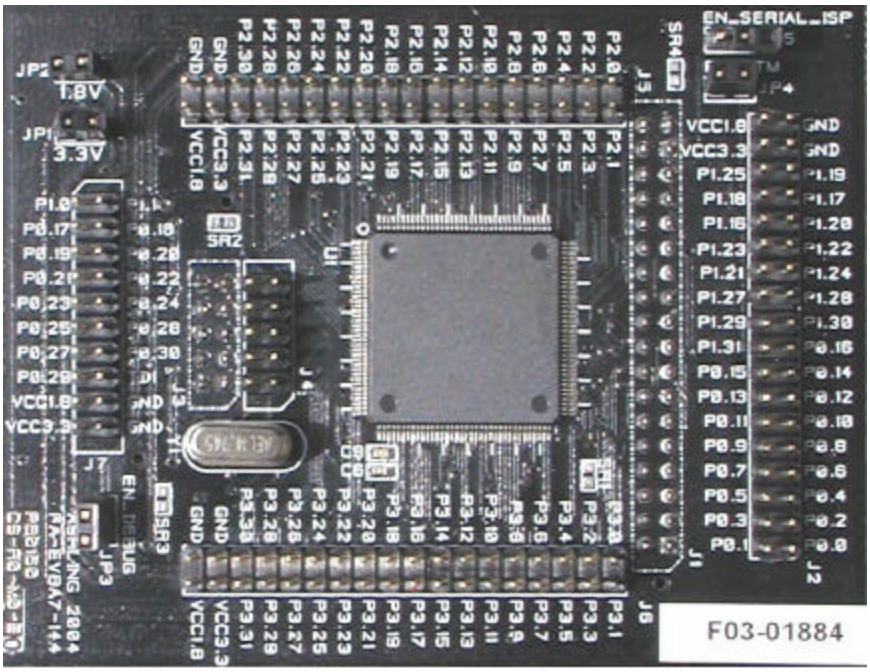

Figure 1: The Ashling AD-EVBA7-LPC2129-64/FA-EVBA7-64 (for LPC211x/212x) and AD-EVBA7-LPC2292-144/FA-EVBA7-144-DR (for LPC22xx) Device Adapters include Jumpers to select the appropriate Debug or Trace mode (Note! Ashling's AD-CA064QFP-J2J3PS/PA-EVBA7-64 and AD-CA144QFP-J2J3PS/PA-EVBA7-144 Programming Socket Adapters have a different layout)

To enable JTAG Debug: fit Jumper EN_DEBUG on the Device Adapter board; **otherwise** leave EN_DEBUG open.

To enable ETM Trace: fit Jumper EN_TRACE on the Device Adapter board; **otherwise** leave EN_TRACE open.

(Do *not* fit jumper EN_SERIAL_ISP unless you want the LPC2000 device to boot-up in Flash ISP boot mode; in this mode the device expects to receive serial RS232 flash programming commands over its UART port)

4 Using Ashling's Programming Socket Adapters for LPC211x/212x and LPC22xx

As illustrated in Figure 2, the EVBA7 On-Board Emulator has a 4.7KΩ resistor fitted from Vcc (+ve supply) to RTCK, to ensure that the LPC210x device has JTAG Debug mode enabled. Figure 2 also illustrates the Jumpers and resistors on Ashling's AD-CA064QFP-J2J3PS/PA-EVBA7-64 (for LPC211x/212x) and AD-CA144QFP-J2J3PS/PA-EVBA7-144 (for LPC22xx) Programming Socket Adapter boards. (Please note that Figure 2 does *not* apply to Ashling's AD-EVBA7-LPC2129-64/FA-EVBA7-64 and AD-EVBA7-LPC2292-144/FA-EVBA7-144 Device Adapters).

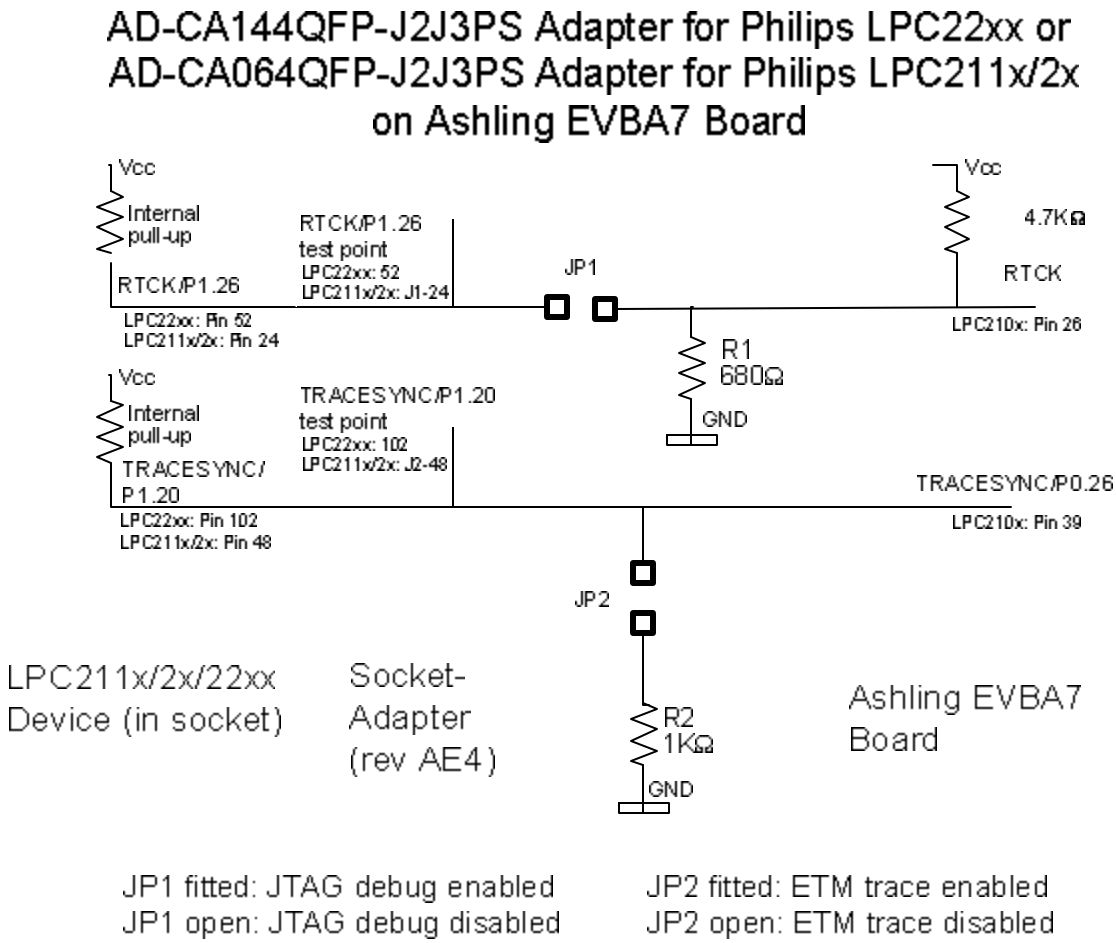

Figure 2:
The Ashling AD-CA064QFP-J2J3PS/PA-EVBA7-64 (for LPC211x/212x) and AD-CA144QFP-J2J3PS/PA-EVBA7-144 (for LPC22xx) Programming Socket Adapter boards include Jumpers to select the appropriate Debug or Trace mode (Note! Ashling's AD-EVBA7-LPC2129-64/FA-EVBA7-64 and AD-EVBA7-LPC2292-144/FA-EVBA7-144 Device Adapters have a different schematic

To enable JTAG Debug: fit Jumper JP1 on the Programming Adapter board; **otherwise** leave JP1 open.

To enable ETM Trace: fit Jumper JP2 on the Programming Adapter board; **otherwise** leave JP2 open.

5 Primary and Secondary Debug modes on LPC210x

The 48-pin LPC210x devices offer a choice of Primary or Secondary JTAG Debug modes. The Primary JTAG port and ETM Trace port are enabled *only* if the DBGSEL and RTCK pins are high at Reset. If either DBGSEL or RTCK or both are low when RST* goes high, neither primary JTAG nor ETM is enabled; in this case, secondary debug (*not* ETM) may be enabled by writing to the PINSEL1 register. (This choice does *not* apply to the 64-pin LPC211x/212x and 144-pin LPC22xx devices). More details and application information on using the LPC210x's Secondary Debug mode are available at the **Knowledge base and FAQ** link on www.ashling.com/support/lpc2000

6 Analog +1.8V supply and Analog Ground on LPC211x/212x/219x and LPC22xx devices

For correct operation of LPC211x/212x/219x and LPC22xx devices, you must ensure that the V18A pin (Analog 1.8V core supply; pin 63 on LPC211x/212x/219x or pin 143 on LPC22xx) and the

VSSA/VSSA_PLL pins (Analog ground; pins 59/58 on LPC211x/212x/219x or pins 138/139 on LPC22xx) are correctly wired.

V18A and VSSA/VSSA_PLL should be at the same voltage as V18 and VSS; ideally, they should be isolated from the main V18, VSS supply to minimize noise. When prototyping your design using the Ashling 64-pin or 144-pin sockets, you will generally want to connect V18A and VSSA/VSSA_PLL direct to V18 and VSS, respectively. When using any of the Adapters, you must ensure that V18A and VSSA/VSSA_PLL are correctly connected; incorrectly wired or open-circuited pins will likely result in failure of the on-chip PLL to operate correctly; this, in turn, may prevent operation of the device's JTAG EmbeddedICE debug port.

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