LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON OPTOCOUPLERS

HCPL-0700 HCPL-0701

DESCRIPTION

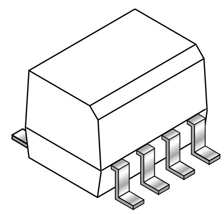
The HCPL-0700 and HCPL-0701 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector housed in a compact 8-pin small outline package.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

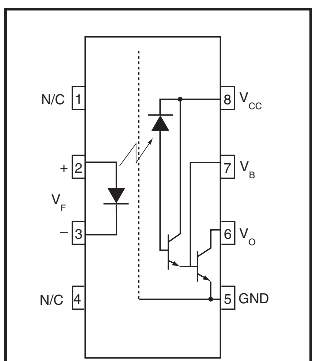
FEATURES

- Low current - 0.5 mA
- Superior CTR-2000%
- Superior CMR-10 kV/µs
- CTR guaranteed 0-70°C
- *BSI, CSA and UL approval



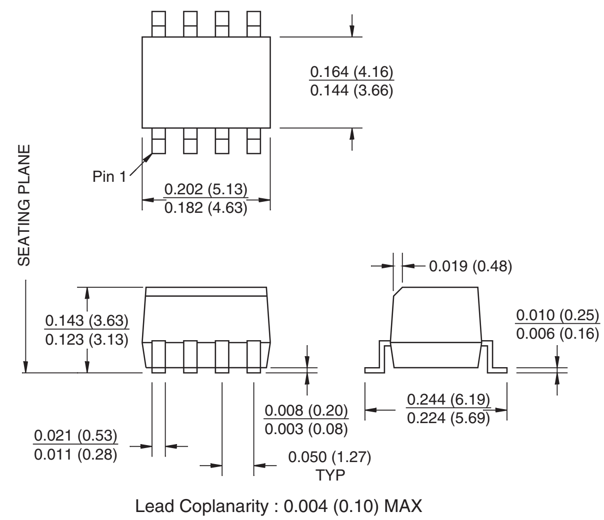
APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- µP bus isolation
- Current loop receiver



HCPL-0700 / HCPL-0701

PACKAGE DIMENSIONS



NOTE
All dimensions are in inches (millimeters)

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HCPL-0700 HCPL-0701

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Value	Units
Storage Temperature		T_{STG}	-55 to +125	°C
Operating Temperature		T_{OPR}	-55 to +85	°C
Reflow Temperature Profile (Refer to fig. 11)				
EMITTER				
DC/Average Forward Input Current		I_F (avg)	20	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)		I_F (pk)	40	mA
Peak Transient Input Current - (≤1 µs P.W., 300 pps)		I_F (trans)	1.0	A
Reverse Input Voltage		V_R	5	V
Input Power Dissipation		P_D	35	mW
DETECTOR				
Average Output Current (Pin 6)		I_O (avg)	60	mA
Emitter-Base Reverse Voltage		V_{EBR}	0.5	V
Supply Voltage, Output Voltage	HCPL-0700	V_{CC}, V_O	-0.5 to 7	V
	HCPL-0701		-0.5 to 18	
Output power dissipation		P_D	100	mW

*Samples submitted for certification - Approval pending

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER	(T_A =25°C)	V_F	All	1.0	1.27	1.7	V
Input Forward Voltage	(I_F = 1.6 mA)					1.75	
Input Reverse Breakdown Voltage	(T_A =25°C, I_R = 10 µA)	BV_R	All	5.0	20		
Temperature coefficient of forward voltage	(I_F = 1.6 mA)	($\Delta V_F/\Delta T_A$)	All		-1.8		mV/°C
DETECTOR Logic high output current	(I_F = 0 mA, V_O = V_{CC} = 18 V)	I_{OH}	HCPL-0701		0.01	100	µA
	(I_F = 0 mA, V_O = V_{CC} = 7 V)		HCPL-0700		0.01	250	
Logic low supply	(I_F = 1.6 mA, V_O = Open)	I_{CCL}	HCPL-0700		0.4	1.5	mA
	(V_{CC} = 18 V)		HCPL-0701				
Logic high supply	(I_F = 0 mA, V_O = Open)	I_{CCH}	HCPL-0700		0.05	10	µA
	(V_{CC} = 18 V)		HCPL-0701				

TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)								
Parameter	**Test Conditions**	**Symbol**	**Device**	**Min**	**Typ****	**Max**	**Unit**
COUPLED	(I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5V)	CTR	HCPL-0701	400	2000	5000	%
Current transfer ratio (Notes 1,2)	(I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5V)		HCPL-0701	500	1300	2600	
	(I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5V)		HCPL-0700	300	1300	2600	
Logic low output voltage output voltage	(I_F = 0.5 mA, I_O = 2 mA, V_{CC} = 4.5V)	V_{OL}	HCPL-0701		0.05	0.4	V
	(I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5V)				0.10	0.4	
	(I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5V)				0.13	0.4	
	(I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5V)				0.20	0.4	
	(I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5V)		HCPL-0700		0.08	0.4	

ISOLATION CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)						
Characteristics	**Test Conditions**	**Symbol**	**Min**	**Typ****	**Max**	**Unit**
Input-output insulation leakage current	(Relative humidity = 45%) (T_A = 25°C, t = 5 s) (V_{I-O} = 3000 VDC) (Note 4)	I_{I-O}			1.0	μA
Withstand insulation test voltage	(R_H ≤ 50%, T_A = 25°C) (Note 4, 5) (t = 1 min.)	V_{ISO}	2500			V_{RMS}
Resistance (input to output)	(Note 4) (V_{I-O} = 500 VDC)	R_{I-O}		10^{12}		Ω

** All typicals at T_A = 25°C

SWITCHING CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified., V_{CC} = 5 V)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low (Note 2) (Fig. 13)	(R_L = 4.7 kΩ, I_F = 0.5 mA) T_A = 25°C	T_{PHL}	HCPL-0701		4	30 25	µs
	(R_L = 270 Ω, I_F = 12 mA) T_A = 25°C		HCPL-0701		0.2	2 1	
	(R_L = 2.2 kΩ, I_F = 1.6 mA) T_A = 25°C		HCPL-0700		1.5	15 10	
Propagation delay time to logic high (Note 2) (Fig. 13)	(R_L = 4.7 kΩ, I_F = 0.5 mA)	T_{PLH}	HCPL-0701		12	90	µs
	(R_L = 4.7 kΩ, I_F = 0.5 mA) T_A = 25°C					60	
	(R_L = 270 Ω, I_F = 12 mA) T_A = 25°C		HCPL-0701		1.3	10 7	
	(R_L = 2.2 kΩ, I_F = 1.6 mA)		HCPL-0700		7	50	
	T_A = 25°C					35	
Common mode transient immunity at logic high	(I_F = 0 mA, $\|V_{CM}\|$ = 10 V_{P-P}) T_A = 25°C (R_L = 2.2 kΩ) (Note 3) (Fig. 14)	$\|CM_H\|$	HCPL-0700 HCPL-0701	1,000	10,000		V/µs
Common mode transient immunity at logic low	(I_F = 1.6 mA, $\|V_{CM}\|$ = 10 V_{P-P}, R_L = 2.2 kΩ) T_A = 25°C (Note 3) (Fig. 14)	$\|CM_L\|$	HCPL-0700 HCPL-0701	1,000	10,000		V/µs

NOTES

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 open. Use of a resistor between pins 5 and 7 will decrease gain and delay time.
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O<0.8 V).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

** All typicals at TA = 25°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified)

Current Limiting Resistor Calculations

$$R_1(\text{Non-Invert}) = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1(\text{Invert}) = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} = V_{OLX}(@ I_L - I_2)}{I_L}$$

Where:

- V_{DD1} - Input Supply Voltage
- V_{DD2} - Output Supply Voltage
- V_{DF} - Diode Forward Voltage
- V_{OL1} - Logic “0” Voltage of Driver
- V_{OH1} - Logic “1” Voltage of Driver
- I_F - Diode Forward Current
- V_{OLX} - Saturation Voltage of Output Transistor
- I_L - Load Current Through Resistor R2
- I_2 - Input Current of Output Gate

INPUT			OUTPUT						
			CMOS @ 5V	CMOS @ 10V	74XX	74LXX	74SXX	74LSXX	74HXX
		R1 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10 V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Fig. 1 Resistor Values for Logic Interface

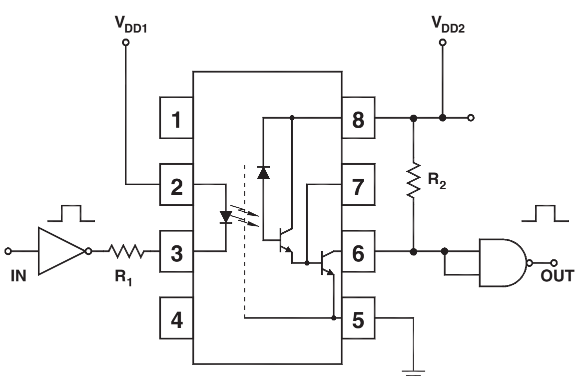


Fig. 2 Non-Inverting Logic Interface

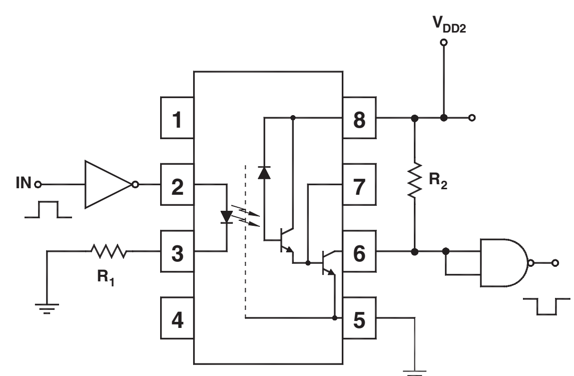


Fig. 3 Inverting Logic Interface

TYPICAL PERFORMANCE CURVES

Fig. 4 Propagation Delay vs. Temperature

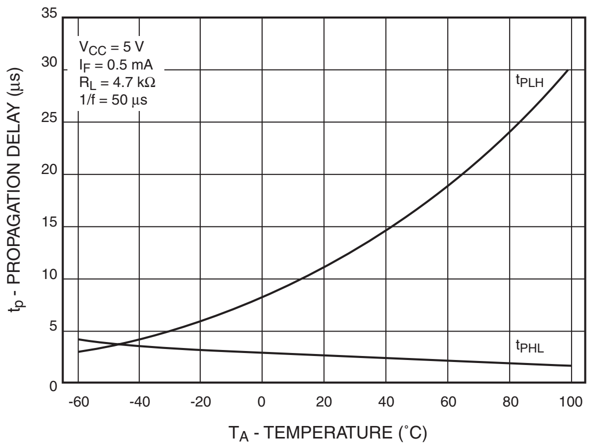


Fig. 5 Propagation Delay vs. Temperature

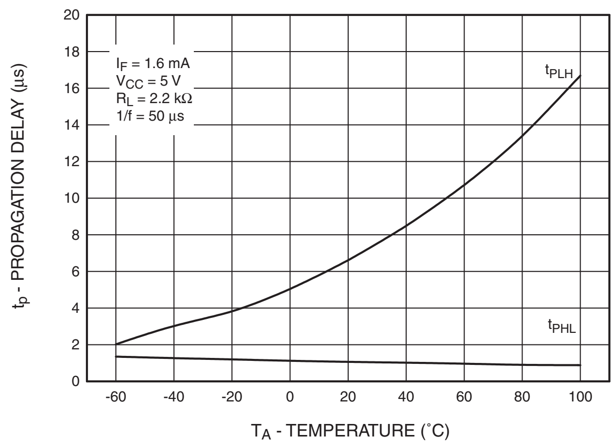


Fig. 6 Propagation Delay vs. Temperature

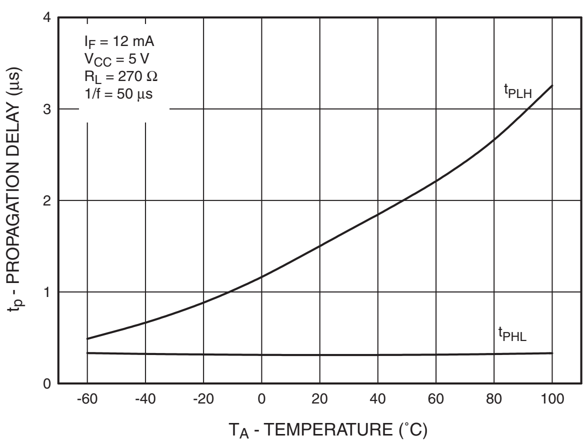
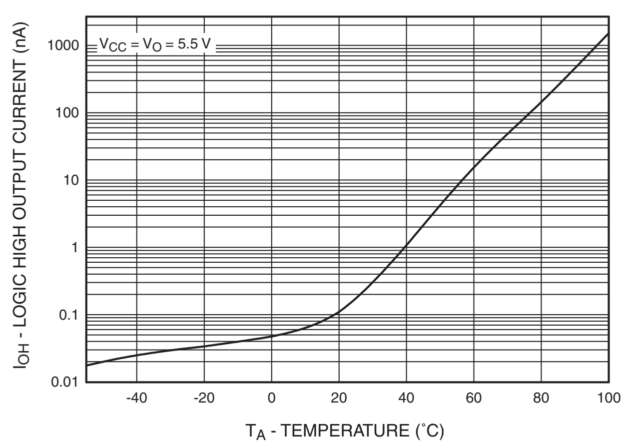


Fig. 7 Logic High Output Current vs. Temperature



TYPICAL PERFORMANCE CURVES

Fig. 8 Output Current vs. Input Forward Current

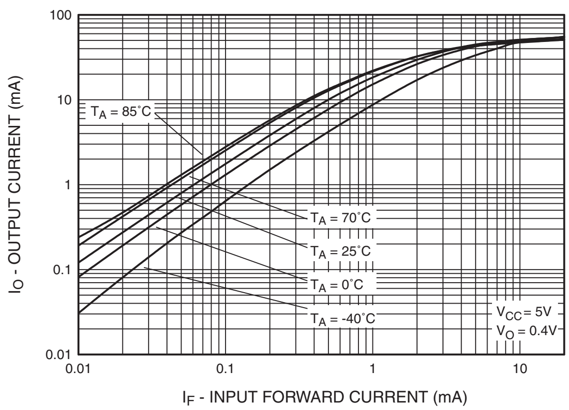


Fig. 9 Input Forward Current vs. Forward Voltage

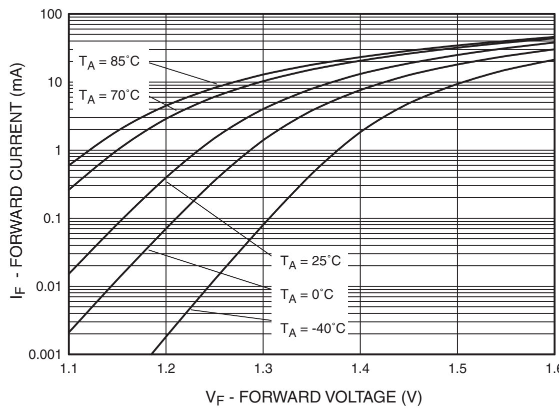


Fig. 10 Logic Low Supply Current vs. Input Forward Current

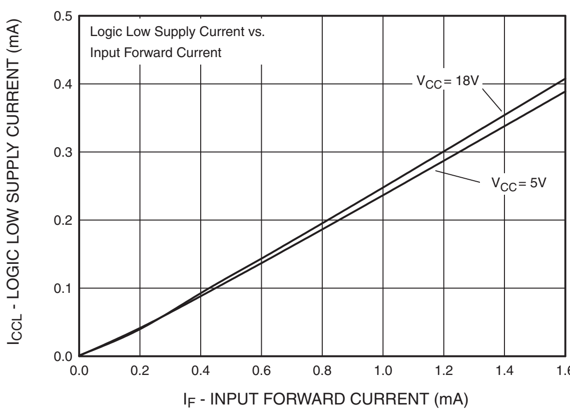


Fig. 11 DC Transfer Characteristics

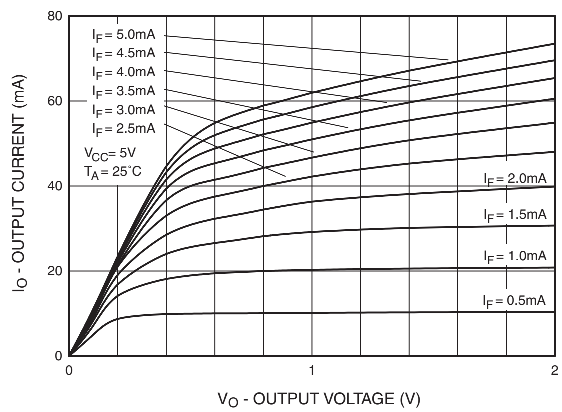
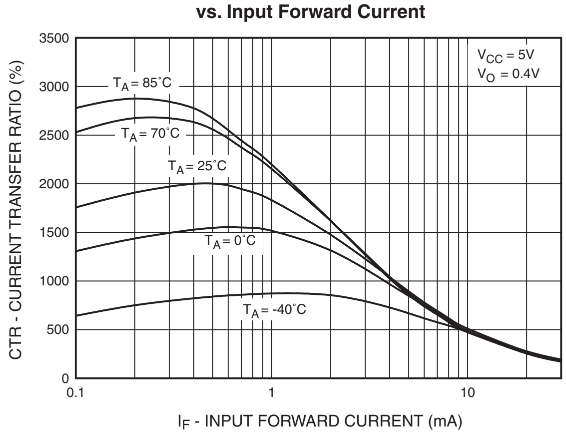
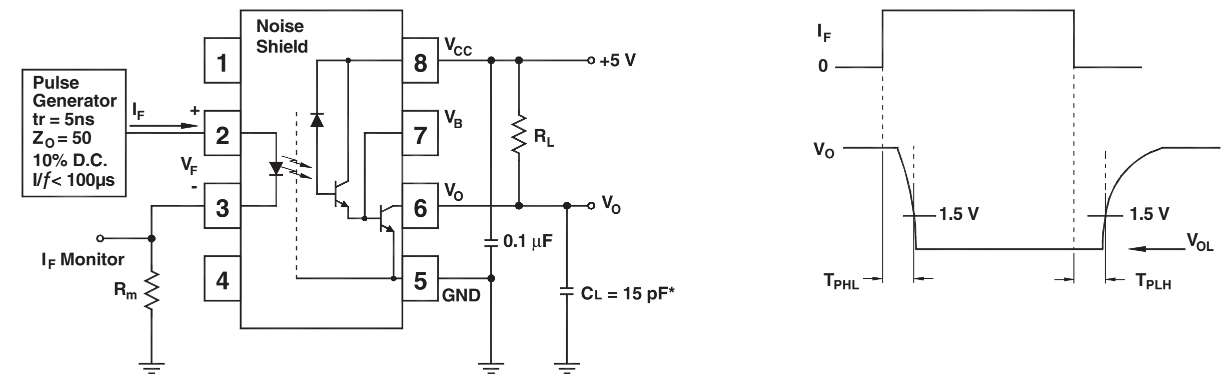


Fig. 12 Current Transfer Ratio vs. Input Forward Current





* Includes probe and fixture capacitance

Fig. 13 Switching Time Test Circuit

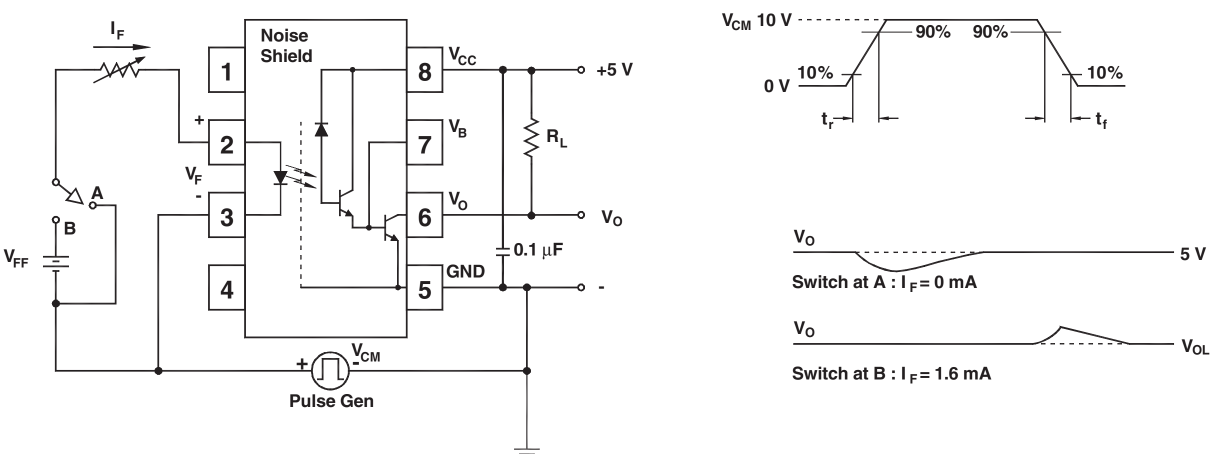
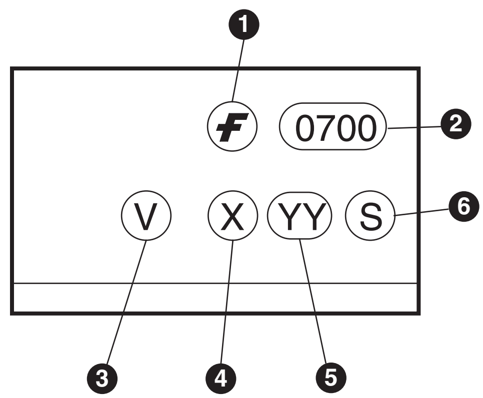


Fig. 14 Common Mode Immunity Test Circuit

ORDERING INFORMATION

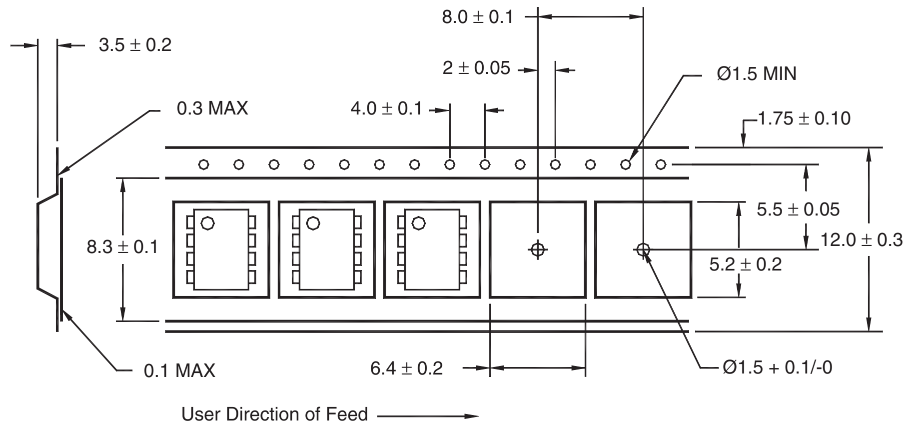
Option	Order Entry Identifier	Description
V	V	VDE 0884
R1	R1	Tape and reel (500 units per reel)
R1V	R1V	VDE 0884, Tape and reel (500 units per reel)
R2	R2	Tape and reel (2500 units per reel)
R2V	R2V	VDE 0884, Tape and reel (2500 units per reel)

MARKING INFORMATION

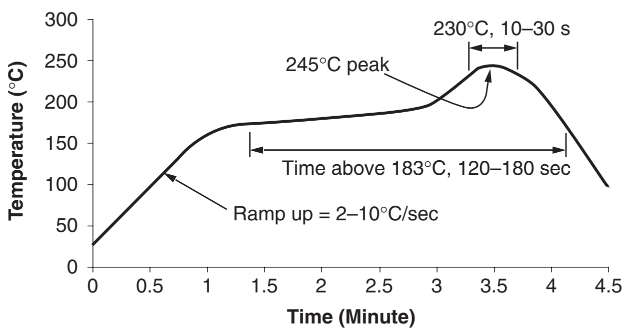


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., ‘3’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Carrier Tape Specifications



Reflow Profile



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

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HCPL-0700 HCPL-0701

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