International
IOR Rectifier

Data Sheet PD No.60238

IRS2153D(S)PbF

SELF-OSCILLATING HALF-BRIDGE DRIVER IC

Features

- Integrated 600V Half-Bridge Gate Driver
- CT, RT programmable oscillator
- 15.4V Zener Clamp on VCC
- Micropower Startup
- Non-latched shutdown on CT pin (1/6th VCC)
- Internal bootstrap FET
- Excellent Latch Immunity on All Inputs & Outputs
- +/- 50V/ns dV/dt immunity
- ESD Protection on All Pins
- 8-lead SOIC or PDIP package
- 1.1 usec (typ.) internal deadtime

Product Summary

VOFFSET	**600V Max**
Duty Cycle	**50%**
Driver source/sink current	**180/260mA typ.**
Vclamp	**15.4V typ.**
Deadtime	**1.1us typ.**

Description

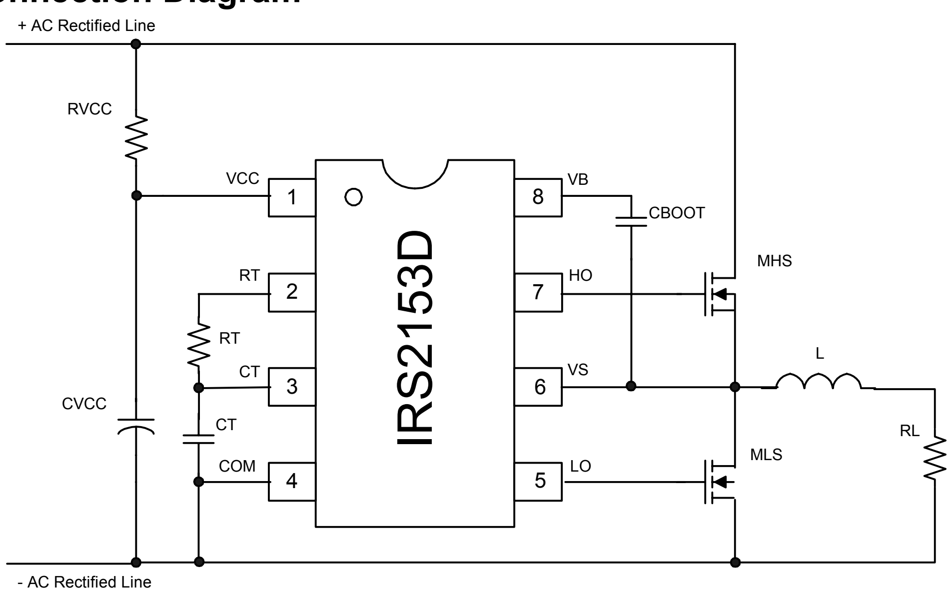
The IRS2153D is based on the popular IR2153 self-oscillating half-bridge gate driver IC using a more advanced silicon platform, and incorporates a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable rugged monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers.

Package

PDIP8
IRS2153DPBF

SO8
IRS2153DSPBF

Typical Connection Diagram



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter				
Symbol	**Definition**	**Min.**	**Max.**	**Units**
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	V
V_{HO}	High-Side Floating Output Voltage	V_S – 0.3	V_B + 0.3	V
V_{LO}	Low-Side Output Voltage	-0.3	V_{CC} + 0.3	V
I_{RT}	R_T Pin Current	-5	5	mA
V_{RT}	R_T Pin Voltage	-0.3	V_{CC} + 0.3	V
V_{CT}	C_T Pin Voltage	-0.3	V_{CC} + 0.3	V
I_{CC}	Supply Current (Note 1)	---	20	mA
IOMAX	Maximum allowable current at LO and HO due to external power transistor Miller effect.	-500	500	
dV_S/dt	Allowable Offset Voltage Slew Rate	-50	50	V/ns
P_D	Maximum Power Dissipation @ $T_A \le$ +25ºC, 8-Pin DIP	---	1.0	W
P_D	Maximum Power Dissipation @ $T_A \le$ +25ºC, 8-Pin SOIC	---	0.625	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 8-Pin DIP	---	85	ºC/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, 8-Pin SOIC	---	128	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	---	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.4V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

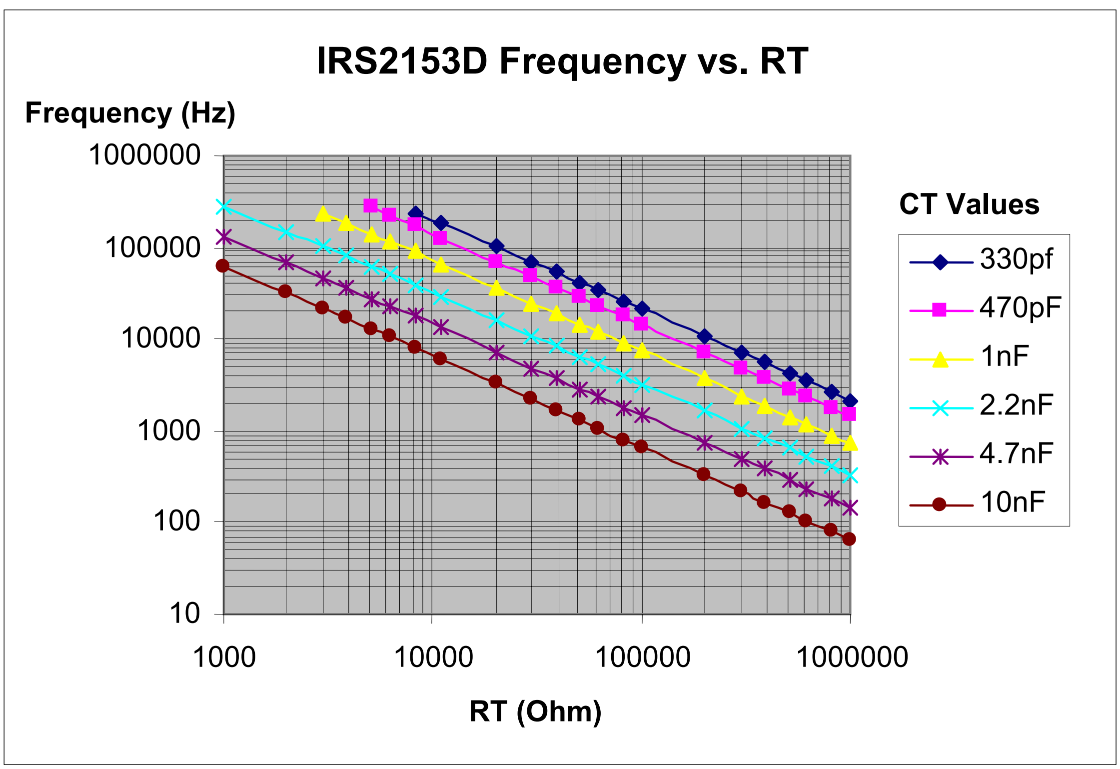
Parameter		Min.	Max.	Units
Symbol	Definition			
V_{BS}	High Side Floating Supply Voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady State High Side Floating Supply Offset Voltage	-3.0 (Note 2)	600	V
V_{CC}	Supply Voltage	V_{CCUV+} +0.1V	$V_{CC\ CLAMP}$	V
I_{CC}	Supply Current	(Note 3)	5	mA
T_J	Junction Temperature	-40	125	ºC

Note 2: Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5V.

Note 3: Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6V zener diode clamping the voltage at this pin.

Recommended Component Values

Parameter		Min.	Max.	Units
Symbol	Component			
R_T	Timing Resistor Value	1	---	kΩ
C_T	C_T Pin Capacitor Value	330	---	pF



Electrical Characteristics

VBIAS (VCC, VBS) = 14V, CT = 1 nF, VS=0V and TA = 25°C unless otherwise specified. The output voltage and current (VO and IO) parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

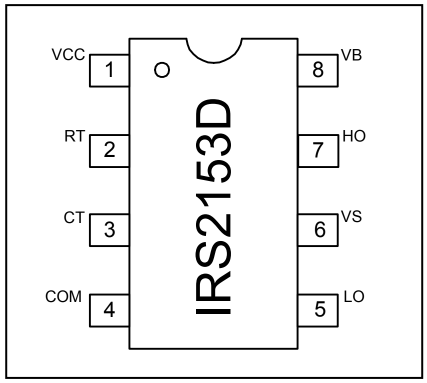
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} Undervoltage Lockout Threshold	10.2	10.8	11.5	V	
V_{CCUV-}	Falling V_{CC} Undervoltage Lockout Threshold	8.3	8.8	9.4	V	
$V_{CCUVHYS}$	V_{CC} Undervoltage Lockout Hysteresis	1.6	2.0	2.4	V	
I_{QCCUV}	Micropower Startup V_{CC} Supply Current	---	130	170	µA	$V_{CC} \le V_{CCUV-}$
I_{QCC}	Quiescent VCC Supply Current	---	800	1000	µA	
I_{CC}	VCC Supply Current	---	1.8	---	mA	R_T = 36.9kΩ
$V_{CC\ CLAMP}$	V_{CC} Zener Clamp Voltage	14.4	15.4	16.8	V	I_{CC} = 5mA
Floating Supply Characteristics						
I_{QBS}	Quiescent V_{BS} Supply Current	---	60	80	µA	
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.0	9.0	9.5	V	
V_{BSUV-}	V_{BS} Supply Undervoltage negative Going Threshold	7.0	8.0	9.0	V	
I_{LK}	Offset Supply Leakage Current	---	---	50	µA	$V_B = V_S$ = 600V
Oscillator I/O Characteristics						
f_{OSC}	Oscillator Frequency	18.4	19.0	19.6	kHz	R_T = 36.5kΩ
		88	93	100	kHz	R_T = 7.15kΩ
d	R_T Pin Duty Cycle	---	50	---	%	f_o < 100kHz
I_{CT}	C_T Pin Current	---	0.02	1.0	µA	
I_{CTUV}	UV-Mode C_T Pin Pulldown Current	0.20	0.30	0.6	mA	V_{CC} = 7V
V_{CT+}	Upper C_T Ramp Voltage Threshold	---	9.32	---	V	
V_{CT-}	Lower C_T Ramp Voltage Threshold	---	4.66	---	V	
V_{CTSD}	C_T Voltage Shutdown Threshold	2.2	2.3	2.4	V	
V_{RT+}	High-Level R_T Output Voltage, $V_{CC} - V_{RT}$	---	10	50	mV	I_{RT} = -100µA
		---	100	300	mV	I_{RT} = -1mA
V_{RT-}	Low-Level R_T Output Voltage	---	10	50	mV	I_{RT} = 100µA
		---	100	300	mV	I_{RT} = 1mA
V_{RTUV}	UV-Mode R_T Output Voltage	---	0	100	mV	$V_{CC} \le V_{CCUV-}$
V_{RTSD}	SD-Mode R_T Output Voltage, $V_{CC} - V_{RT}$	---	10	50	mV	I_{RT} = -100µA, V_{CT} = 0V
		---	100	300	mV	I_{RT} = -1mA, V_{CT} = 0V

Electrical Characteristics

VBIAS (VCC, VBS) = 14V, CT = 1 nF, VS=0V and TA = 25°C unless otherwise specified. The output voltage and current (VO and IO) parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

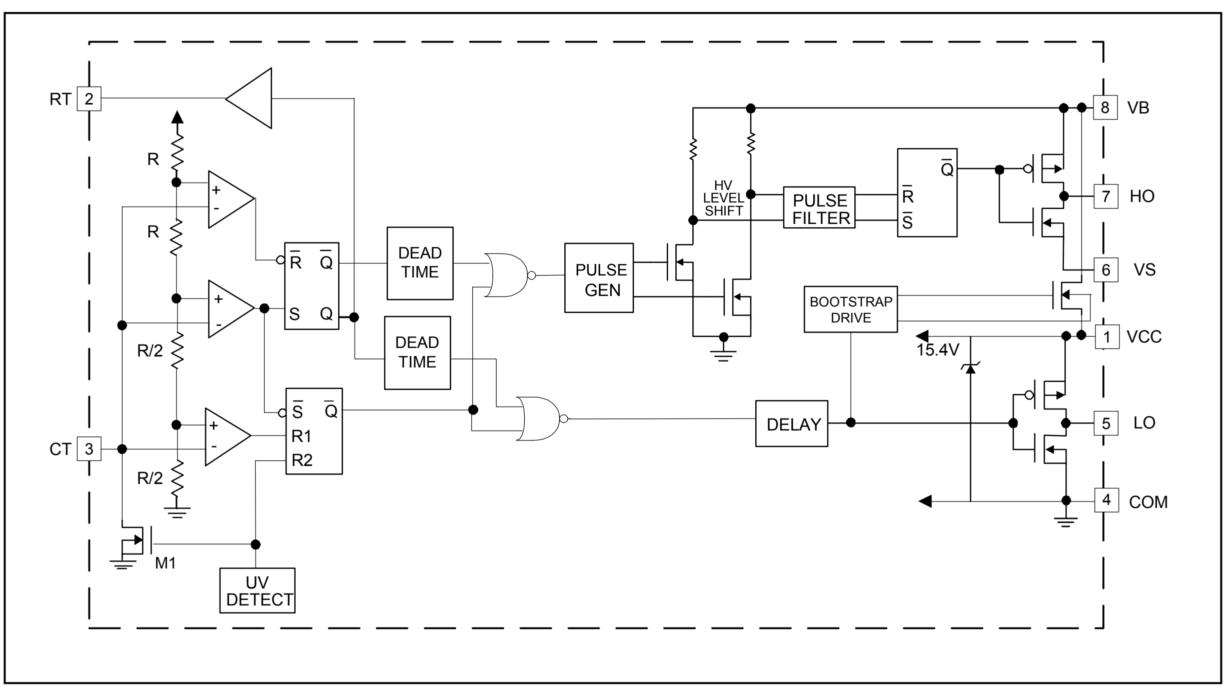
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver Output Characteristics						
V_{OH}	High-Level Output Voltage	---	VCC	---		$I_O = 0A$
V_{OL}	Low-Level Output Voltage	---	COM	---		$I_O = 0A$
V_{OL_UV}	UV-Mode Output Voltage	---	COM	---		$I_O = 0A$, $V_{CC} \leq V_{CCUV-}$
t_r	Output Rise Time	---	120	220	nsec	
t_f	Output Fall Time	---	50	80		
t_{sd}	Shutdown Propagation Delay	---	350	---		
t_d	Output Deadtime (HO or LO)	0.65	1.1	1.75	µsec	
IO+	Output source current	---	180	---	mA	
IO-	Output sink current	---	260	---		
Bootstrap FET Characteristics						
VB_ON	VB when the bootstrap FET is on	---	13.7	---	V	
IB_CAP	VB source current when FET is on	40	55	---	mA	CBS=0.1uF
IB_10V	VB source current when FET is on	10	12	---		VB=10V

Lead Definitions



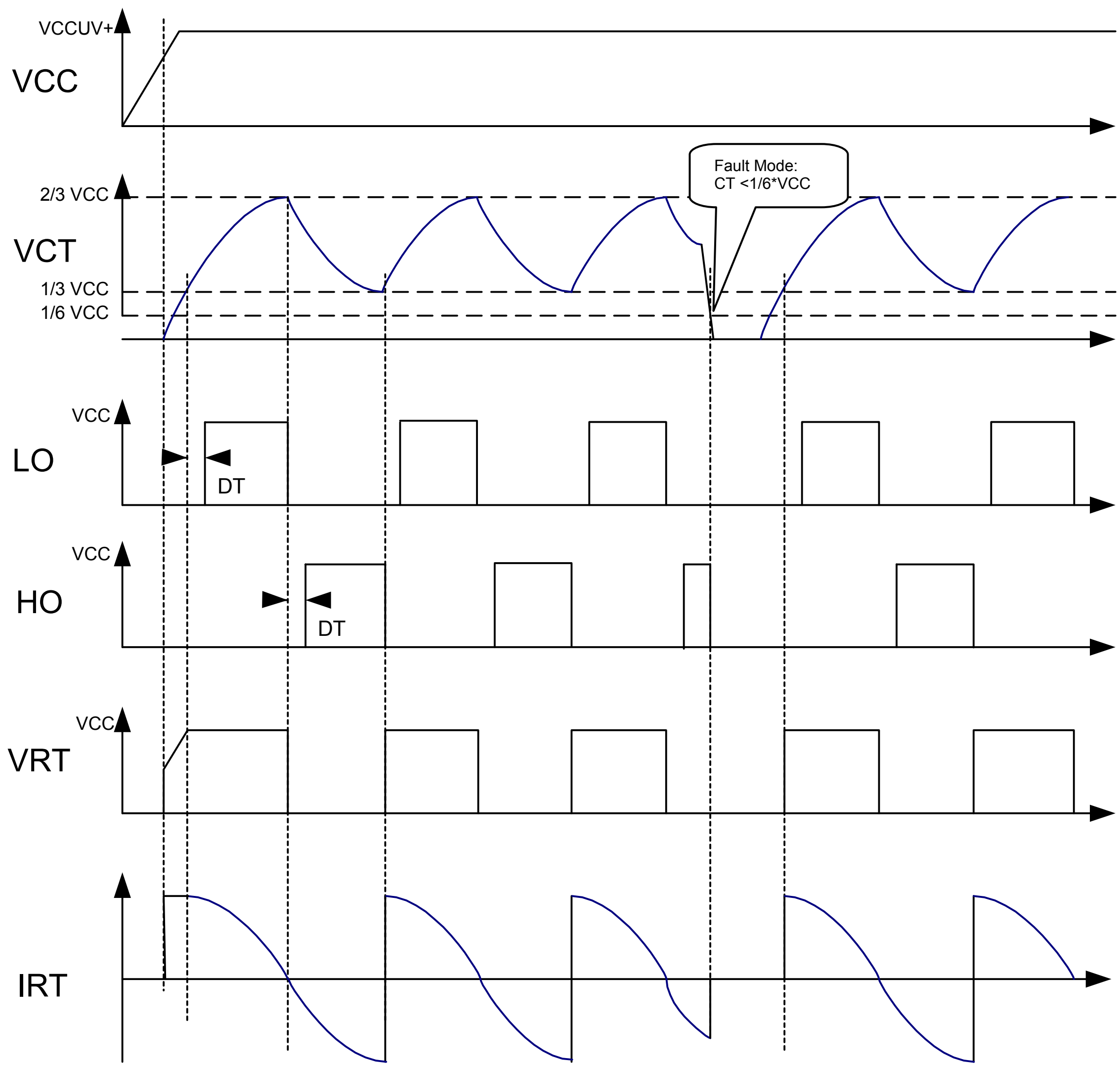
Symbol	Lead Description
V_{CC}	Logic and internal gate drive supply voltage
R_T	Oscillator timing resistor input
C_T	Oscillator timing capacitor input
COM	IC power and signal ground
LO	Low-side gate driver output
V_S	High voltage floating supply return
HO	High-side gate driver output
V_B	High side gate driver floating supply

Functional Block Diagram

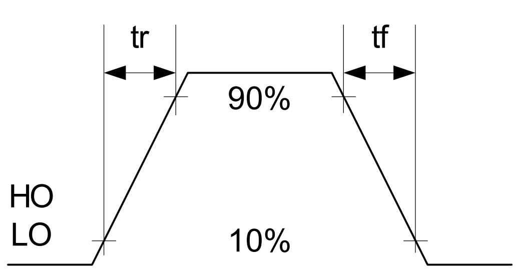


Timing Diagram

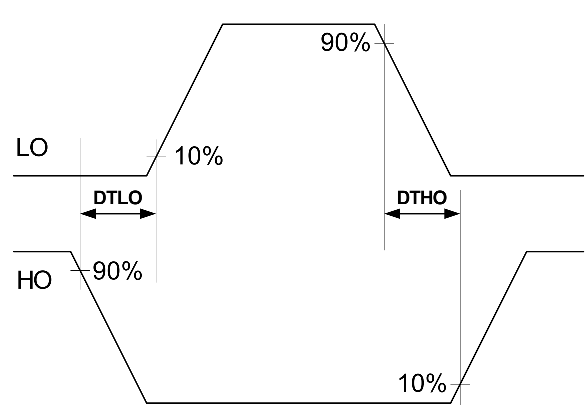
Operating Mode



Switching Time Waveform



Deadtime Waverform



Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. The IRS2153D under voltage lock-out is designed to maintain an ultra low supply current of less than 155uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under voltage lock-out mode, the high and low-side driver outputs HO and LO are both low.

Supply voltage

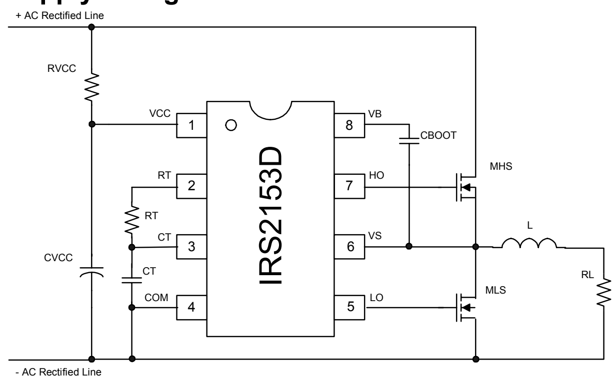


Fig. 1 Typical Connection Diagram

Fig. 1 shows an example of supply voltage. The start-up capacitor (C_{VCC}) is charged by current through supply resistor (R_{VCC}) minus the start-up current drawn by the IC. This resistor is chosen to provide sufficient current to supply the IRS2153D from the DC bus. C_{VCC} should be large enough to hold the voltage at Vcc above the UVLO threshold for one half cycle of the line voltage as it will only be charged at the peak, typically 0.1uF. It will be necessary for RVCC to dissipate around 1W.

The use of a two diode charge pump made of DC1, DC2 and CVS (Fig. 2) from the half bridge (VS) is also possible however the above approach is simplest and the dissipation in R_{VCC} should not be unacceptably high.

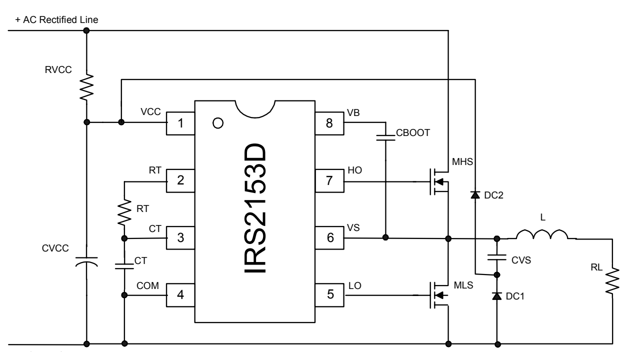


Fig. 2 Charge pump circuit

The supply resistor (R_{VCC}) must be selected such that enough supply current is available over all operating conditions.

Once the capacitor voltage on VCC reaches the start-up threshold VCCUV+, the IC turns on and HO and LO begin to oscillate.

Bootstrap MOSFET

The internal bootstrap FET and supply capacitor (C_{BOOT}) comprise the supply voltage for the high side driver circuitry. The internal boostrap FET only turns on when LO is high. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin.

Normal operating mode

Once the VCCUV+ threshold is passed, the MOSFET M1 opens, RT increases to approximately VCC (VCC-VRT+) and the external CT capacitor starts charging. Once the CT voltage reaches VCT- (about 1/3 of VCC), established by an internal resistor ladder, LO turns on with a delay equivalent to the deadtime td. Once the CT voltage reaches VCT+ (approximately 2/3 of VCC), LO goes low, RT goes down to approximately ground (VRT-), the CT capacitor discharges and the deadtime circuit is activated. At the end of the deadtime, HO goes high. Once the CT voltage reaches VCT-, HO goes low, RT goes high again, the deadtime is activated. At the end of the deadtime, LO goes high and the cycle starts over again.

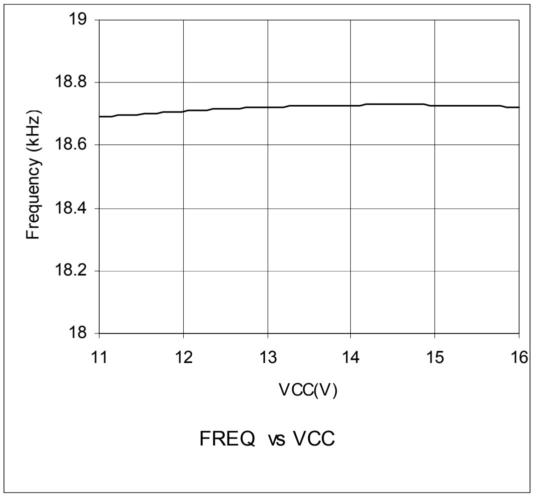
The following equation provides the oscillator frequency:

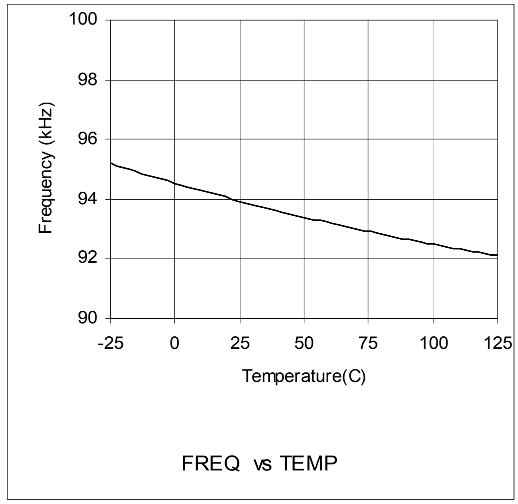
$$f \sim \frac{1}{1.453 \times RT \times CT}$$

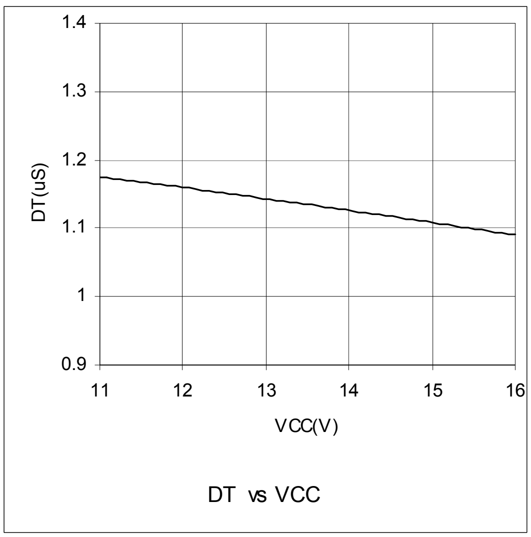
This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays. For a more accurate determination of the output frequency, the frequency characteristic curves should be used (RT vs. Frequency, Page 3).

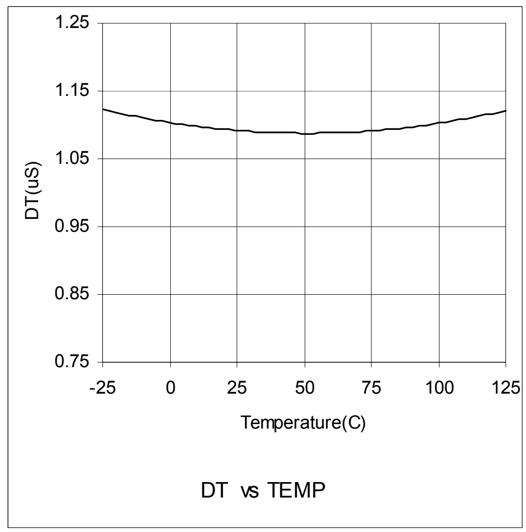
Shut-down

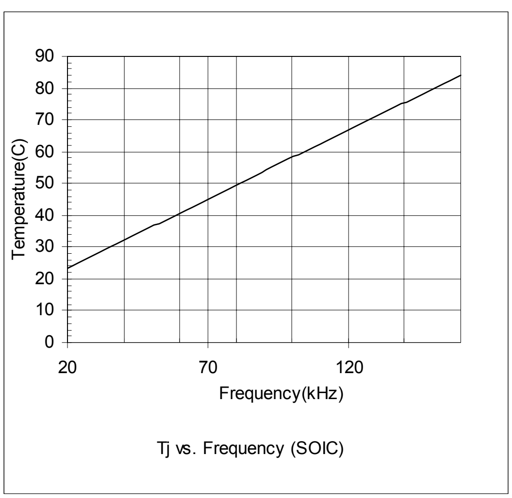
If CT is pulled down below VCTSD (approximately 1/6 of VCC) by an external circuit, CT doesn't charge up and oscillation stops. LO is held low and the bootstrap FET is off. Oscillation will resume once CT is able to charge up again to VCT-.

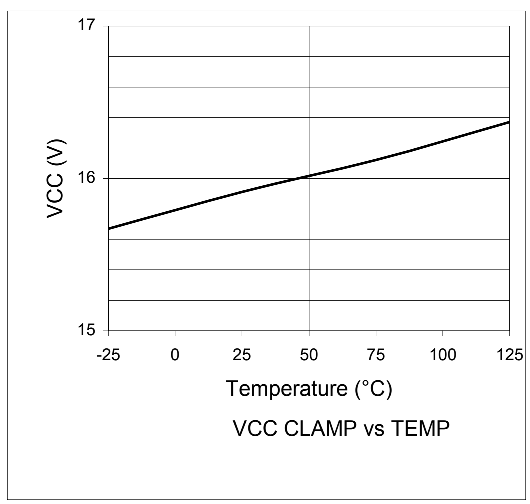

19
18.8
18.6
18.4
18.2
18
11
12
13
14
15
16
Frequency (kHz)
VCC(V)
FREQ vs VCC

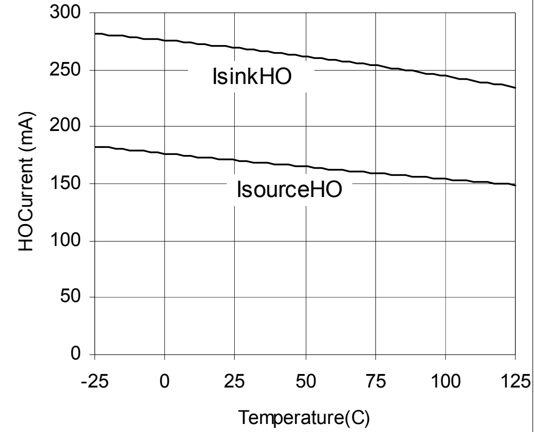

100
98
96
94
92
90
-25
0
25
50
75
100
125
Frequency (kHz)
Temperature(C)
FREQ vs TEMP


1.4
1.3
1.2
1.1
1
0.9
11
12
13
14
15
16
DT(uS)
VCC(V)
DT vs VCC

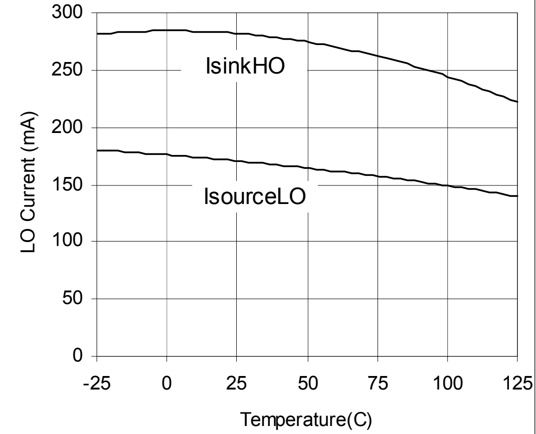

1.25
1.15
1.05
0.95
0.85
0.75
-25
0
25
50
75
100
125
DT(uS)
Temperature(C)
DT vs TEMP


90
80
70
60
50
40
30
20
10
0
20
70
120
Temperature(C)
Frequency(kHz)
Tj vs. Frequency (SOIC)

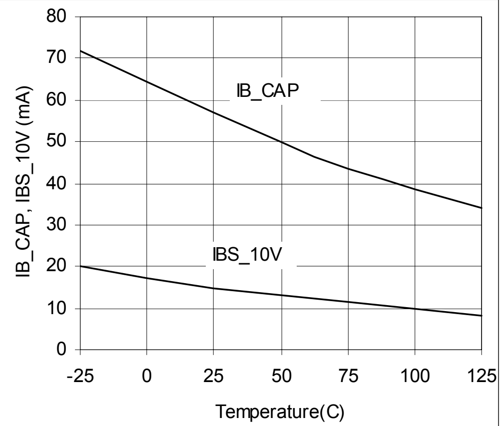

17
16
15
-25
0
25
50
75
100
125
VCC (V)
Temperature (°C)
VCC CLAMP vs TEMP



IsourceHO,IsinkHO vs Temp

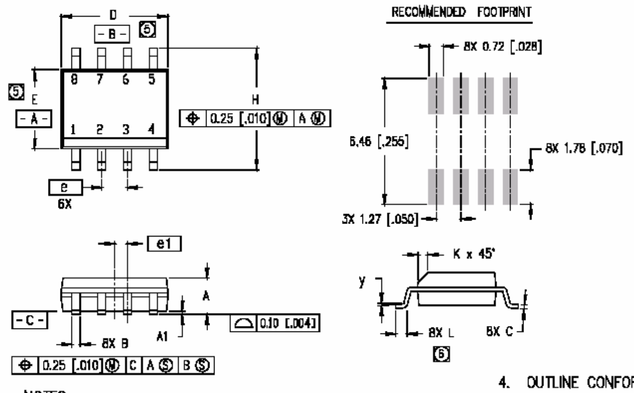


IsourceLO,IsinkLO vs Temp



IBCAP, IBS10V vs TEMP

IRS2153DSPbF

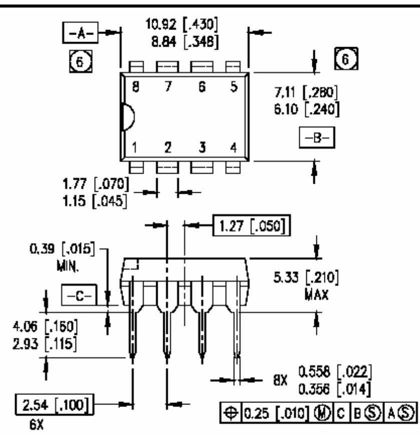


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

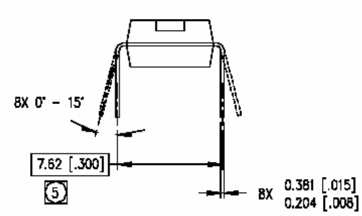
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

IRS2153DPbF



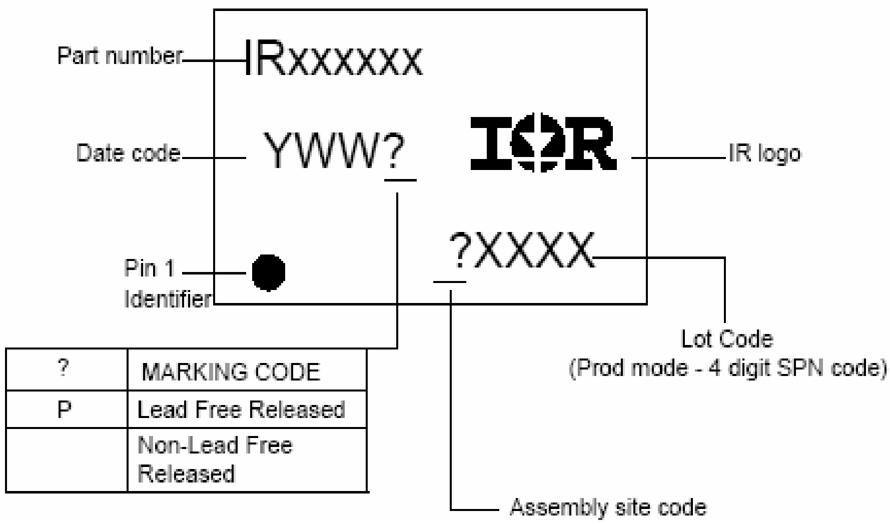
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Leadfree Part

8-Lead PDIP IRS2153D order IRS2153DPbF

8-Lead SOIC IRS2153DS order IRS2153DSPbF

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