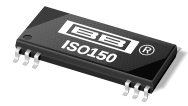
Burr-Brown Products from Texas Instruments

ISO150



SBOS032A – SEPTEMBER 2000 – REVISED FEBRUARY 2003

Dual, Isolated, Bidirectional DIGITAL COUPLER

FEATURES

- REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
- DATA RATE: 80M Baud, typ
- LOW POWER CONSUMPTION: 25mW Per Channel, max
- TWO CHANNELS, EACH BIDIRECTIONAL, PROGRAMMABLE BY USER
- PARTIAL DISCHARGE TESTED: 2400Vrms
- CREEPAGE DISTANCE OF 7.2mm
- LOW COST PER CHANNEL
- SO PACKAGE

APPLICATIONS

- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- ISOLATED UART INTERFACE
- MULTIPLEXED DATA TRANSMISSION
- ISOLATED PARALLEL TO SERIAL INTERFACE
- TEST EQUIPMENT
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED LINE RECEIVER
- GROUND LOOP ELIMINATION

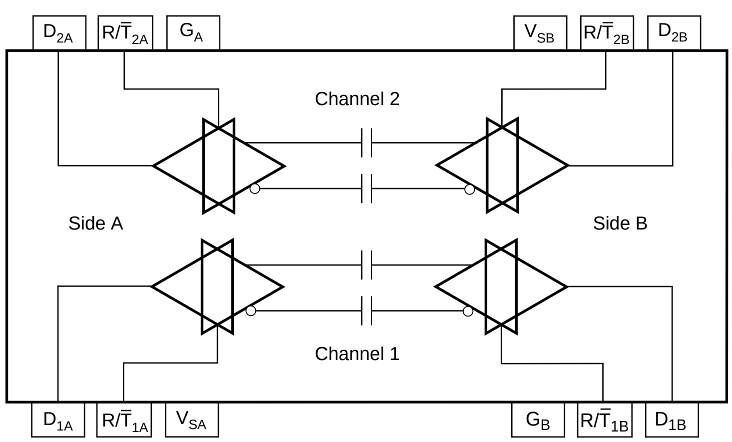
DESCRIPTION

The ISO150 is a 2-channel, galvanically-isolated data coupler capable of data rates of 80M Baud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/µs.

The ISO150 avoids problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

The ISO150 is available in an SO-28 and is specified for operation from –40°C to +85°C.



ABSOLUTE MAXIMUM RATINGS[1]

Storage Temperature	–40°C to +125°C
Supply Voltages, V_S	–0.5 to 6V
Transmitter Input Voltage, V_I	–0.5 to V_S + 0.5V
Receiver Output Voltage, V_O	–0.5 to V_S + 0.5V
$R/\overline{T}_X$ Inputs	–0.5 to V_S + 0.5V
Isolation Voltage dV/dt, V_{ISO}	500kV/µs
D_X Short to Ground	Continuous
Junction Temperature, T_J	175°C
Lead Temperature (soldering, 10s)	260°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

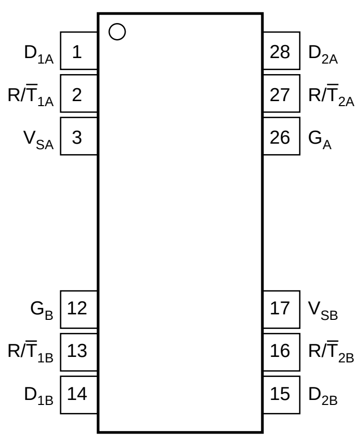
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ISO150AU	SO-28	DVB	–40°C to +85°C	ISO150AU	ISO150AU	Rails, 28
"	"	"	"	"	ISO150AU/1K	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION

Top View SO



PIN DESCRIPTIONS

NAME	FUNCTION
D_{1A}	Data in or data out for transceiver 1A. $R/\overline{T}_{1A}$ held LOW makes D_{1A} an input pin.
$R/\overline{T}_{1A}$	Receive/Transmit switch controlling transceiver 1A.
V_{SA}	+5V supply pin for side A, which powers transceivers 1A and 2A.
G_B	Ground pin for transceivers 1B and 2B.
$R/\overline{T}_{1B}$	Receive/Transmit switch controlling transceiver 1B.
D_{1B}	Data in or data out for transceiver 1B. $R/\overline{T}_{1B}$ held LOW makes D_{1B} an input pin.
D_{2B}	Data in or data out for transceiver 2B. $R/\overline{T}_{2B}$ held LOW makes D_{2B} an input pin.
$R/\overline{T}_{2B}$	Receive/Transmit switch controlling D_{2B}.
V_{SB}	+5V supply pin for side B, which powers transceivers 1B and 2B.
G_A	Ground pin for transceivers 1A and 2A.
$R/\overline{T}_{2A}$	Receive/Transmit switch controlling transceiver 2A.
D_{2A}	Data in or data out for transceiver 2A. $R/\overline{T}_{2A}$ held LOW makes D_{2A} in input pin.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_S = +5V, unless otherwise noted.

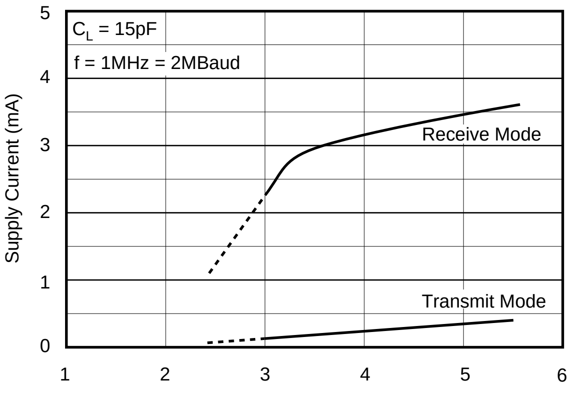
PARAMETER	CONDITION	ISO150AU MIN	TYP	MAX	UNITS
ISOLATION PARAMETERS					
Rated Voltage, Continuous	60Hz	1500			Vrms
Partial Discharge, 100% Test(1)	1s, 5pC	2400			Vrms
Creepage Distance (External)					
SO—“U” Package			7.2		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity(2)			1.6		kV/µs
Barrier Impedance			$> 10^{14} \parallel 7$		Ω ∥ pF
Leakage Current	240Vrms, 60Hz		0.6		µArms
DC PARAMETERS					
Logic Output Voltage, HIGH, V_{OH}	I_{OH} = 6mA	V_S – 1		V_S	V
LOW, V_{OL}	I_{OL} = 6mA	0		0.4	V
Logic Output Short-Circuit Current	Source or Sink		30		mA
Logic Input Voltage, HIGH(3)		2		V_S	V
LOW(3)		0		0.8	V
Logic Input Capacitance			5		pF
Logic Input Current			< 1		nA
Power-Supply Voltage Range(3)		3	5	5.5	V
Power-Supply Current(4)					
Transmit Mode	DC		0.001	100	µA
	50M Baud		14		mA
Receive Mode	DC		7.2	10	mA
	50M Baud		16		mA
AC PARAMETERS					
Data Rate, Maximum(5)	C_L = 50pF	50	80		M Baud
Data Rate, Minimum		DC			
Propagation Time(6)	C_L = 50pF		27	40	ns
Propagation Delay Skew(7)	C_L = 50pF		0.5	2	ns
Pulse Width Distortion(8)	C_L = 50pF		1.5	6	ns
Output Rise-and-Fall Time, 10% to 90%	C_L = 50pF		9	14	ns
Mode Switching Time					
Receive-to-Transmit			13		ns
Transmit-to-Receive			75		ns
TEMPERATURE RANGE					
Operating Range		–40		85	°C
Storage		–40		125	°C
Thermal Resistance, θ_{JA}			75		°C/W

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power-supply voltage with approximately 0.4V hysteresis—see text. (4) Supply current measured with both transceivers set for the indicated mode. Supply current varies with data rate—see typical characteristics. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from V_{IN} = 1.5V to V_O = 2.5V. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between propagation time of a rising edge and a falling edge.

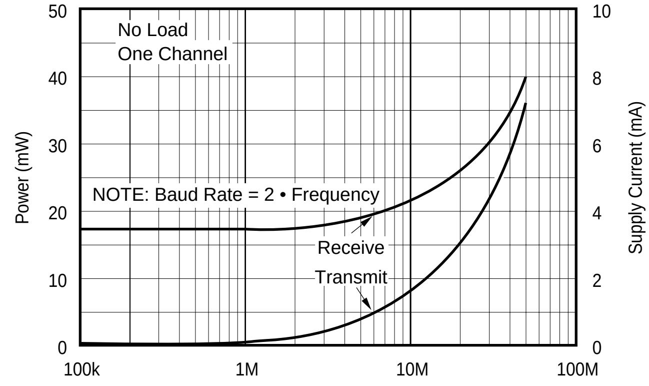
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = +5V, unless otherwise noted.

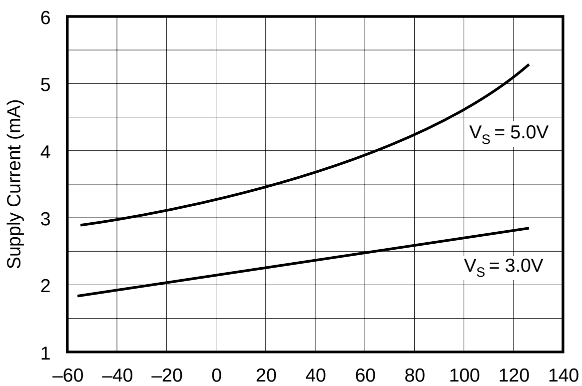
SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE



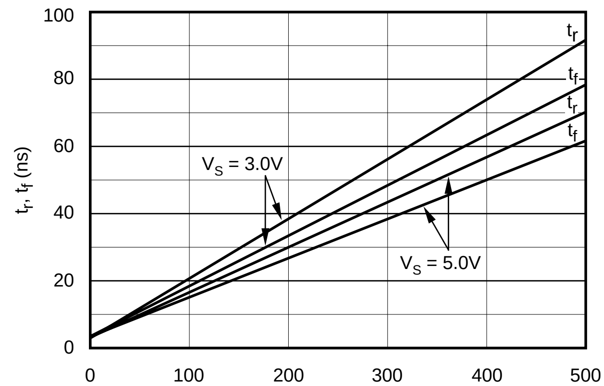
POWER CONSUMPTION PER CHANNEL vs FREQUENCY



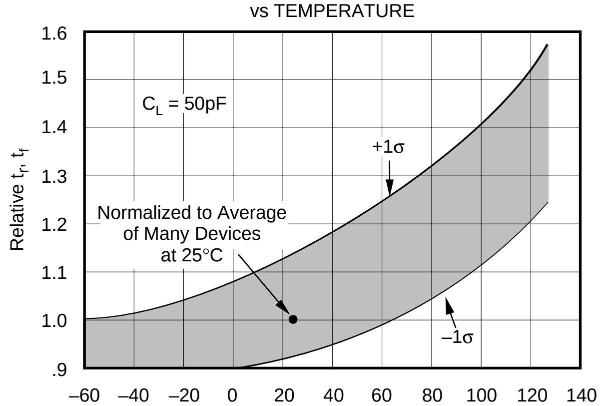
SUPPLY CURRENT PER CHANNEL vs TEMPERATURE



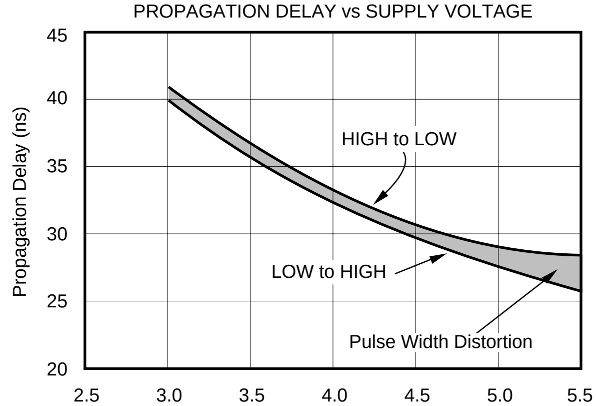
TYPICAL RISE-AND-FALL TIMES vs CAPACITIVE LOAD vs SUPPLY VOLTAGE



NORMALIZED RISE-AND-FALL TIME vs TEMPERATURE

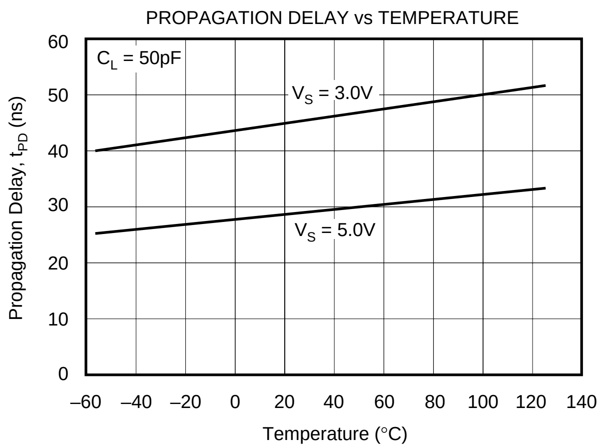


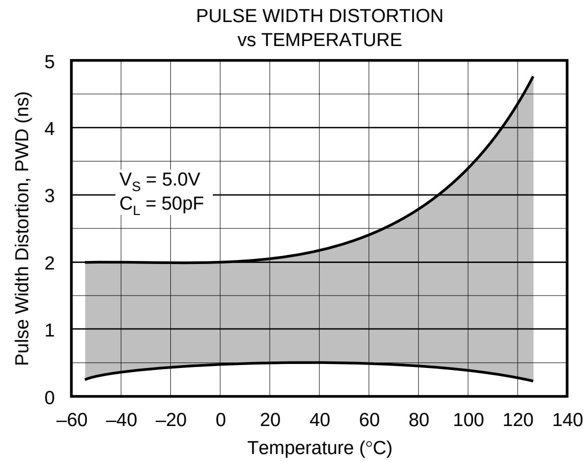
PROPAGATION DELAY vs SUPPLY VOLTAGE

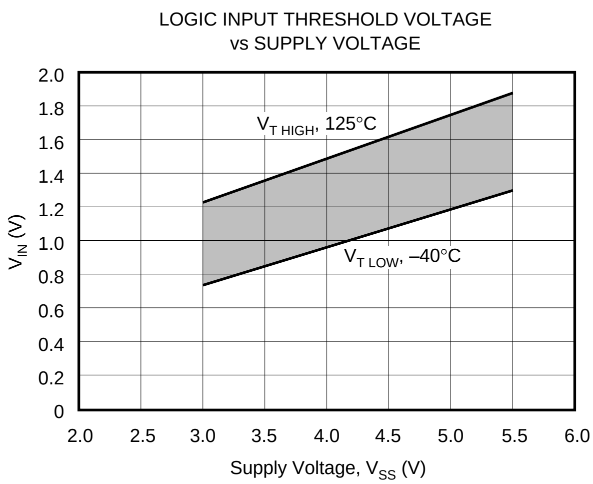


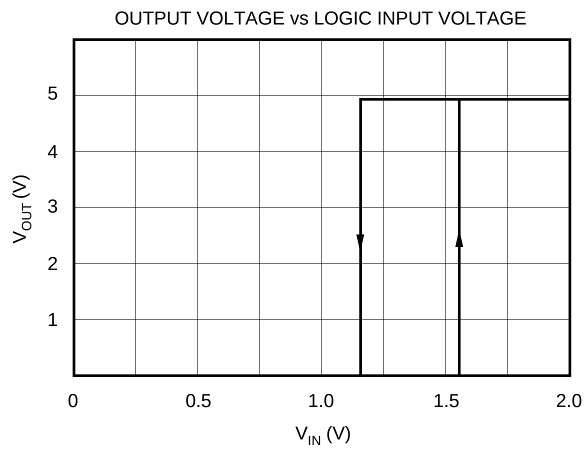
TYPICAL CHARACTERISTICS (Cont.)

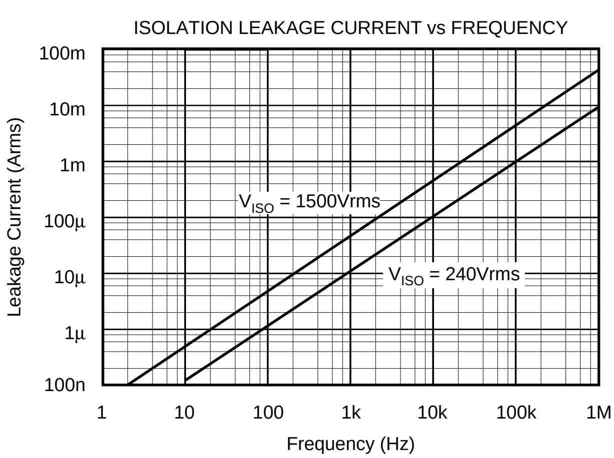
At T_A = +25°C and V_S = +5V, unless otherwise noted.

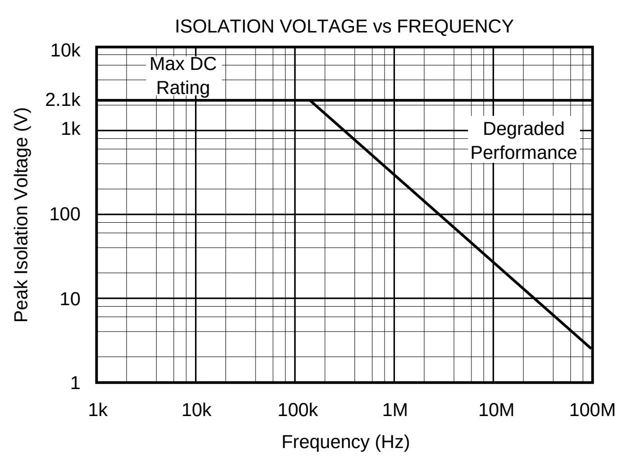


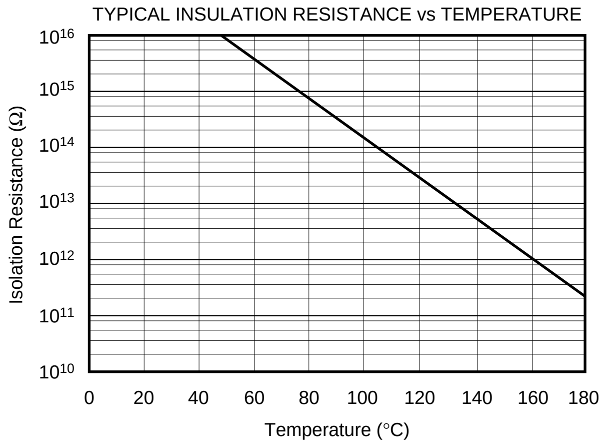












ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO150 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO150 is verified by partial discharge testing: 2400Vrms, 60Hz, is applied across the barrier for one second while measuring any tiny discharge currents that might flow through the barrier. These current pulses are produced by localized ionization within the barrier; this is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATIONS INFORMATION

Figure 1 shows the ISO150 connected for basic operation; Channel 1 is configured to transmit data from side B to A, whereas Channel 2 is set for transmission from side A to B. The $R/\overline{T}$ pins for each of the four transceivers are shown connected to the required logic level for the transmission direction shown. The transmission direction can be controlled by logic signals applied to the $R/\overline{T}$ pins. Channel 1 and 2 can be independently controlled for the desired transmission direction. See Figures 2 and 3 for application examples using the ISO150.

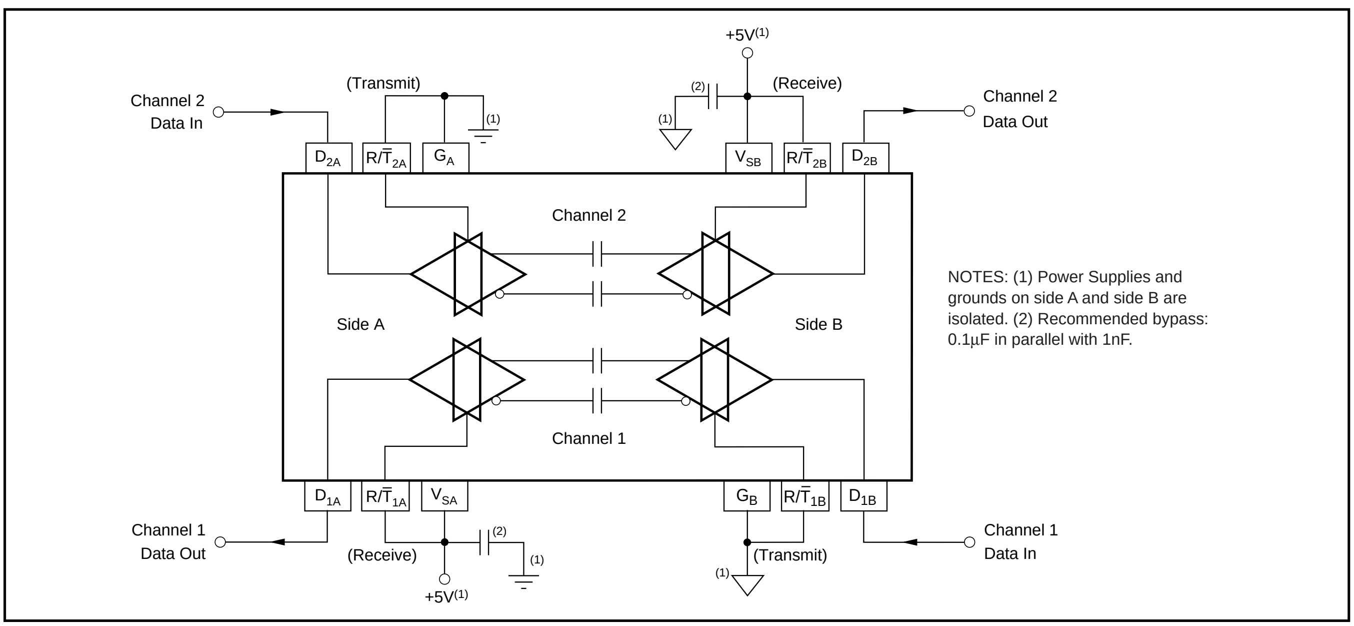


FIGURE 1. Basic Operation Diagram.

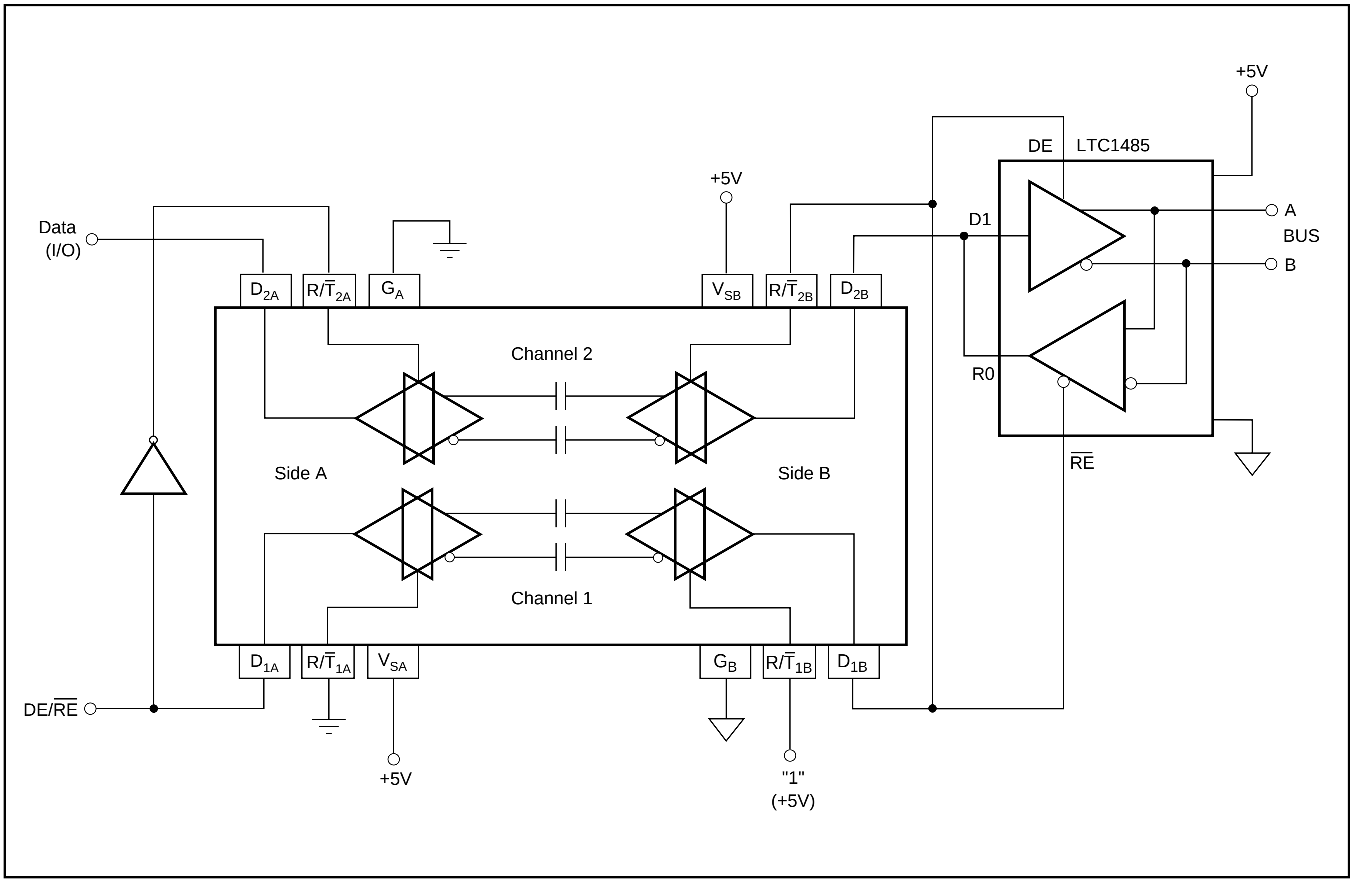


FIGURE 2. Isolated RS-485 Interface.

LOGIC LEVELS

A single pin serves as a data input or output, depending on the mode selected. Logic inputs are CMOS with thresholds set for TTL compatibility. The logic threshold is approximately 1.3V with 5V supplies with approximately 400mV of hysteresis. Input logic thresholds vary with the power-supply voltage. Drive the logic inputs with signals that swing the full logic voltage swing, note that the ISO150 will use somewhat greater quiescent current if logic inputs do not swing within 0.5V of the power-supply rails.

In receive mode, the data output can drive 15 standard LS-TTL loads. It will also drive CMOS loads. The output drive circuits are CMOS.

POWER SUPPLY

Separate, isolated power supplies must be connected to side A and side B to provide galvanic isolation. Nominal rated supply voltage is 5V. Operation extends from 3V to 5.5V. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier.

The V_S pin for each side powers the transceivers for both channel 1 and 2. The specified supply current is the total of both transceivers on one side, both operating in the indicated mode. Supply current for one transceiver in transmit mode and one in receive mode can be estimated by averaging the specifications for transmit and receive operation. Supply current varies with the data transmission rate—see the typical characteristics.

POWER-UP STATE

The ISO150 transmits information across the barrier only when the input-side data changes logic state. When a transceiver is first programmed for receive mode, or is powered-up in receive mode, its output is initialized HIGH. Subsequent changes of data applied to the input side will cause the output to properly reflect the input side data.

SIGNAL LOSS

The ISO150's differential-mode signal transmission and careful receiver design make it highly immune to voltage across the isolation barrier (isolation-mode voltage). Rapidly changing isolation-mode voltage can cause data errors. As the rate of change of isolation voltage is increased, there is a very sudden increase in data errors. Approximately 50% of all ISO150s will begin to produce data errors with isolation-mode transients of 1.6kV/µs. This may occur as low as 500V/µs in some devices. In comparison, a 1000Vrms, 60Hz isolation-mode voltage has a rate of change of approximately 0.5V/µs.

Still, some applications with large, noisy isolation-mode voltage can produce data errors by causing the receiver output to change states. After a data error, subsequent changes in input data will produce correct output data.

PROPAGATION DELAY AND SKEW

Logic transitions are delayed approximately 27ns through the ISO150. Some applications are sensitive to data skew—the difference in propagation delay between channel 1 and channel 2. Skew is less than 2ns between channel 1 and channel 2. Applications using more than one ISO150 must allow for somewhat greater skew from device to device. As all devices are tested for delay times of 20ns min to 40ns max, 20ns is the largest device-to-device data skew.

MODE CHANGES

The transmission direction of a channel can be changed *on the fly* by reversing the logic levels at the R/$\overline{T}$ pins of the channel on both side A and side B. Approximately 75ns after the transceiver is programmed to receive mode it's output is initialized HIGH, and will respond to subsequent input-side changes in data.

STANDBY MODE

Quiescent current of each transceiver circuit is very low in transmit mode when input data is not changing (1nA typical). To conserve power when data transmission is not required, program both side A and B transceivers for transmit mode. Input data applied to either transceiver is ignored by the other side. High-speed data applied to either transceiver will increase quiescent current.

CIRCUIT LAYOUT

The high speed of the ISO150 and its isolation barrier require careful circuit layout. Use good high speed logic layout techniques for the input and output data lines. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier. Use low inductance connections. Ground planes are recommended.

Maintain spacing between side 1 and side 2 circuitry equal or greater than the spacing between the missing pins of the ISO150 (approximately 7mm).

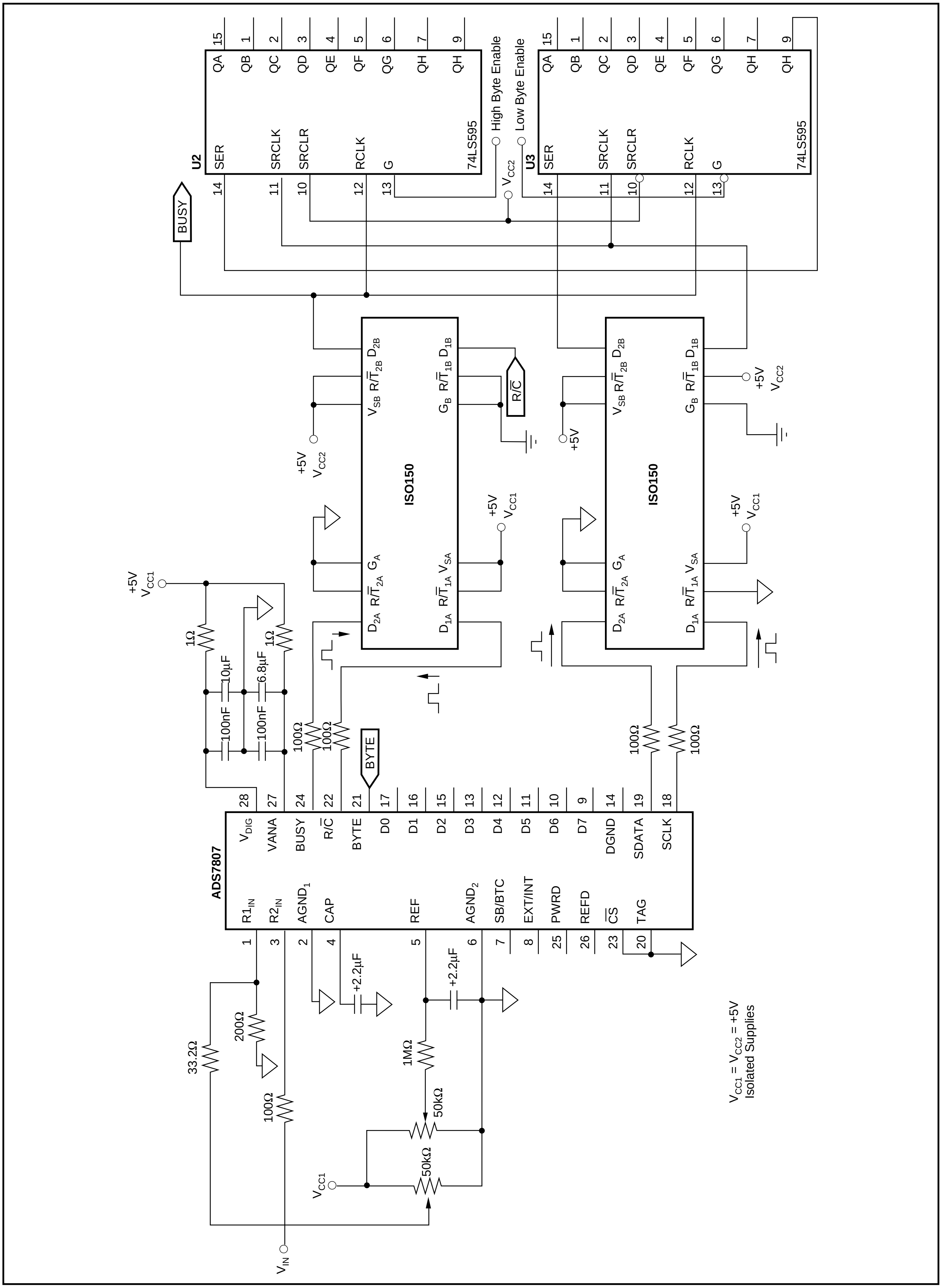
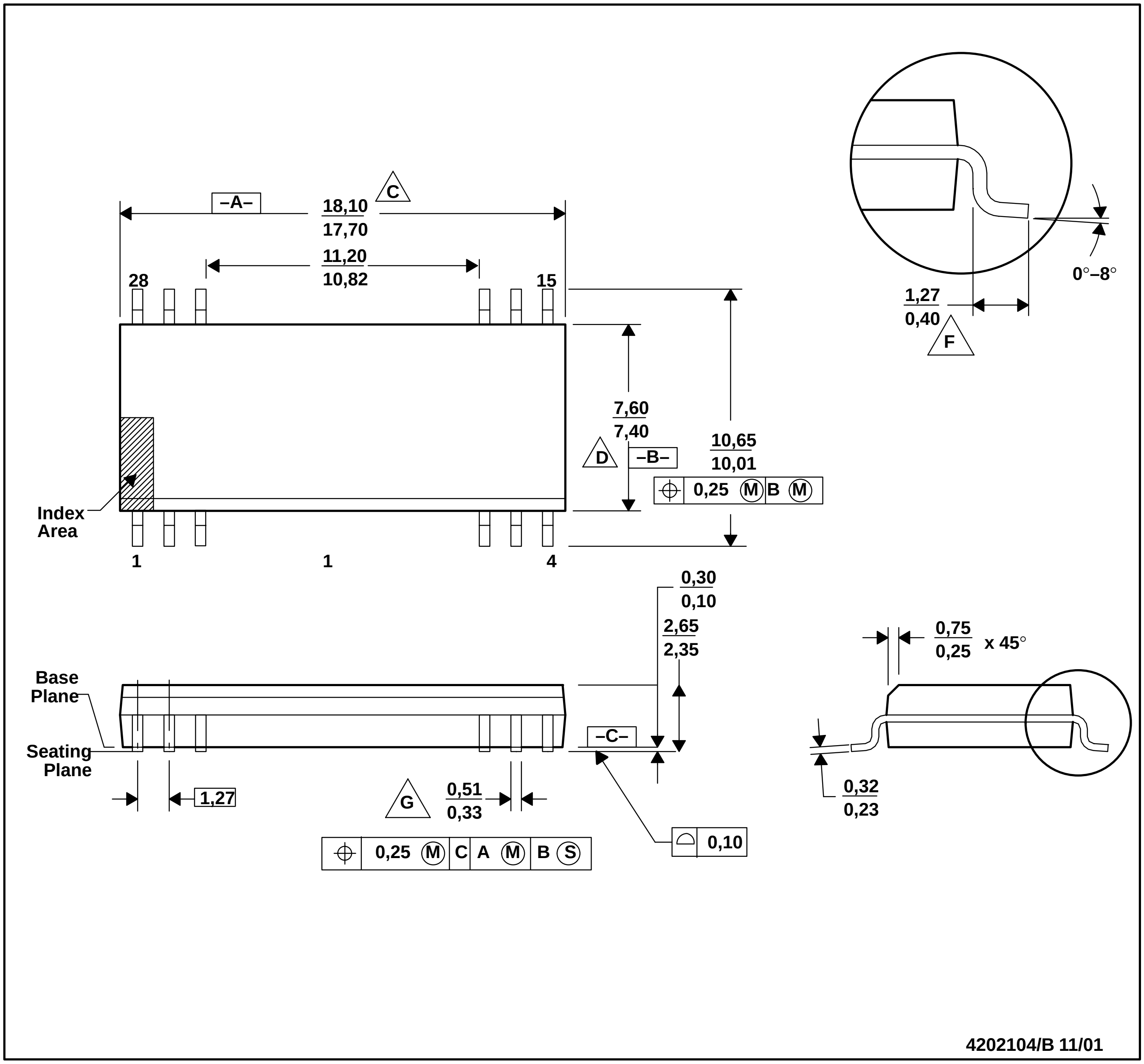


FIGURE 3. The ISO150 and the ADS7807 are Used to Reduce Circuit Noise in a Mixed-Signal Application.

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
ISO150AP	OBSOLETE	PDIP	NVG	12	
ISO150AU	ACTIVE	SOP	DVA	8	28
ISO150AU/1K	ACTIVE	SOP	DVA	8	1000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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