

No. 4476A

LB1854M

Three-Phase Brushless Motor Driver IC

Overview

The LB1854M is a three-phase brushless motor driver IC and is optimal, in particular, for driving VCR capstan and drum motors.

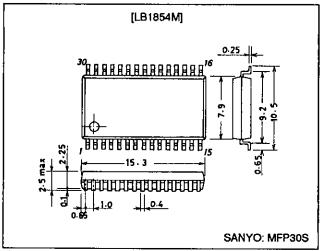
Features

- 120° voltage linear drive technique
- The LB1854M soft switching scheme allows smaller external capacitors to be used (e.g., chip capacitors).
- · Built-in thermal-shutdown function
- · Built-in overcurrent protection circuit
- Built-in FG amplifiers (operational amplifier and Schmitt amplifier)
- · Control start voltage set by an external voltage
- The output current feedback level can be changed by changing the control gain to one of two levels.

Package Dimensions

unit: mm

3073A-MFP30S



Note: The package dimensions are the same for the domestic Japanese products and the import access products.

The mark "MT" is displayed on the package of import access products for identification.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Administration of the second	V _{CC} 1 max		20	V
Maximum supply voltage	V _{CC} 2 max		7.0	V
Applied output voltage	V _{OU, V, W}		22	V
Maximum output current	I _{OUT} max		1.5	A
Allowable power dissipation	Pd max		1.05	w
Operating temperature	Topr		-20 to +75	•c
Storage temperature	Tstg		-55 to +150	-

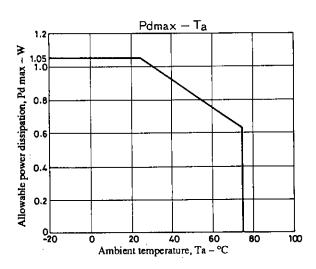
Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} 1	,	5 to 18	٧
Supply Voltage	V _{CC} 2		4.3 to 6.5	٧

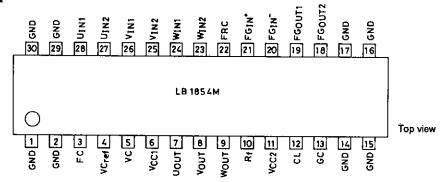
Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 12 V, $V_{CC}2$ = 5 V

Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Current drain		V _C = 0 V, R _L = ∞		17	30	mA	
I _{CC} 2		V _C =0V		6.5	9.5	mA	
[Drive Block]							
Output saturation voltage	V _O (sat) 1	I _{OUT} = 0.5 A, sink + source	·	1.6	2.2	٧	
Compar satisfation voitage	V _O (sat) 2	I _{OUT} = 1.0 A, sink + source		2.0	3.0	٧	
Output TRS breakdown voltage	V _O (sus)	l _{OUT} = 20 mA	20			>	*
Output resting potential	Voa	V _C = 0 V	5.7	6.0	6.3	>	
Hall amplifier Input offset voltage	V _H offset		- 5		+5	mV	
Hall amplifier input bias current	I _H bias			1	5	μA	
Hall amplifier common mode input voltage range	V _H ch	·	1.3		2.2	٧	
Hall input/output voltage gain	GV _{HO}		43	46	49	dB	
[Control Block]							
Control output drive gain	GV _{CO} 1	High gain	37	40	43	dB	
Control output drive gain	GV _{CO} 2	Low gain	31	34	37	dB	
Control output CH difference	∆GV _{CO}		-2		+2	dB	
Control start voltage	V _{CTH}	When V _{OUT} p-p = 2 V		2.5		V	
Gain control switching high level	,		4		5	V	
Gain control switching middle level		Middle level when the input is open	2		3	٧	
Gain control switching low level			0		1	V	
[FG Amplifier]			•				
FG amplifier input offset voltage	V _{FG} offset		-8		+8	mV	
Open-loop voltage gain	GV _{FG}	f = 1 kHz		60		dB	
Source output saturation voltage	V _{FG OU}	I _O = 2 mA	37			٧	
Sink output saturation voltage	V _{FG OD}	I _O = -2 mA			1.3	٧	
Common-mode signal rejection ratio	CHR			80		dB	
FG amplifier common-mode input voltage range	V _{FG CH}		0		3.5	٧	
Phase margin				20		Deg	*
Schmitt hysteresis	∆Vsh1	FG _{OUT} 2: High to low		22		m۷	
	∆Vsh2	FG _{OUT} 2: Low to high		22		mV	
Schmitt input voltage range	Vsh _{CH}		0.7		3.5	V	
[Thermal Shutdown]				-	•		
Operating temperature	TSD		150	180	210	°C	•
Hysteresis	ΔTSD			15		°C	*

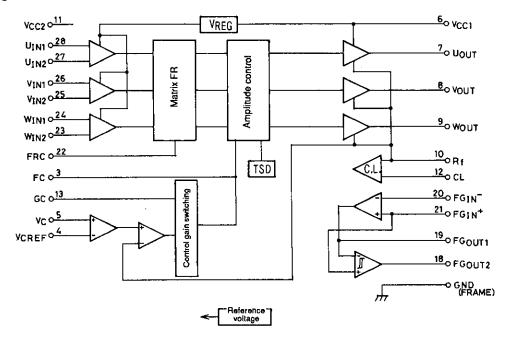
Note: * Items marked with an asterisk are design target values and are not measured.



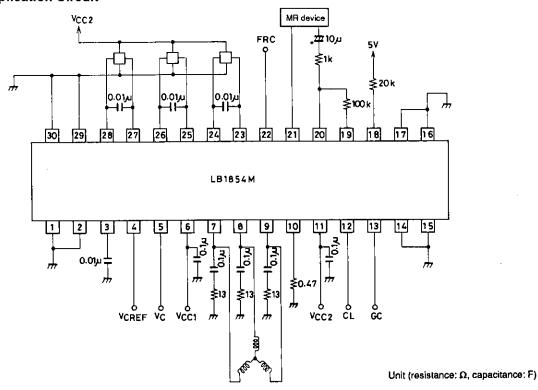
Pin Assignment



Block Diagram



Sample Application Circuit



Truth Table

abla	Source	Input			Forward and reverse control
	Sink	υ	V	W	F/RC
•	W phase → V phase	н	н		L
'	V phase → W phase	П			Н
2	W phase → U phase	н	L	,	L
^	U phase → W phase	-			н
3	V phase → W phase			н	L
	W phase → V phase	L .		-	Н
4	U phase → V phase		Н	,	L
*	V phase → U phase	L .	"		н
· 5	V phase → U phase	Н	L		L
	U phase → V phase			н	Н
6	U phase → W phase	L	Н	ш	L
	W phase → U phase	┖		H	н

Input high: Phase 1 is 0.2 V or more higher than the corresponding phase 2 for each phase input. Low: Phase 1 is 0.2 V or more lower than the corresponding phase 2 for each phase input. Forward and reverse control high: 2.3 V to V_{CC}1 Low: 0 V to 0.7 V

Pin Functions

Unit (resistance: Ω)

Pin No.	Sumbal	Din voltage	Equivalent circuit	Onit (resistance: 12)
1, 2, 14, 15, 16, 17, 29, 30	Symbol FRAME (GND)	Pin voltage	Equivalent dicuit	Ground for all circuits except the outputs
3	FC		VCC2 3.9k ₹	The gain frequency characteristics can be lowered by connecting a capacitor between this pin and ground to prevent oscillation.
4 5	VC REF	1.5 V min V _{CC} 2 max 0 V min V _{CC} 2 max	VCC2 50,µ 200,µ 50,µ 50,µ 200,8 200,	Speed control The LB1854M implements a voltage control scheme in which the output voltage is controlled by the pin 5 voltage. The pin 4 voltage determines the control start voltage.
6	V _{CC} 1	5 to 18 V		Power supply that provides the drive outputs

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Unit (resistance: Ω)

				Unit (resistance: Ω)
Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
7 8 9	U _{OUT} Vout Wout		V _{CC1} 7 8 9 777 0Rf	Output pins
10	P ₄			Output transistor ground Feedback can be applied to the control amplifier by inserting resistor between this pin and GND and detecting the output current as a voltage. The overcurrent protection circuit (current limiter) operates by detecting the voltage on this pin.
11	V _{CC} 2	4.3 to 6.5 V		Power supply provided to all blocks other than the output block This voltage must be stabilized so that no ripple or other noise is present.
12	CL	0 V min V _{CC} 2 max	VCC2	The current limiter operates when the R _f pin reaches the same potential as pin 12. The pin 12 potential is set up externally.
13	GC	0 V min V _{CC} 2 max	VCC2 50k ₹ 10k 50k ₹	Control input to output gain switching pin High level (4 to 5 V): 34 dB Middle level (2 to 3 V) or open: 40 dB (low speed): 34 dB (high speed) Low level (0 to 1 V): 40 dB However, note that this applies when V _{CC} 2 is 5 V.
18	FG _{OUT} 2		Vcc2	FG Schmitt amplifier output
19	FG _{OUT} 1		V _{CC2} 38 ₹ 30 ₹ 19	FG amplifier output

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Unit (resistance: Ω) Pin No. Pin voltage Equivalent circuit Symbol Function VCC2 0 V min FG_{IN} 20 3.5 V max FG signal input FG_{IN+} (when V_{CC}2 is 21 5 V) **VREG** Motor forward/reverse control pin High: 2.3 V min 22 FRC Low level (0.7 V or lower): forward Low: 0.7 V max High level (2.3 V or higher): reverse W_{IN}2 23 W phase Hall sensor input $W_{IN}1$ 24 Logic high is the WIN1 > WIN2 state. 25 $V_{IN}2$ V phase Hall sensor input 1.4 V min (25) Logic high is the $V_{1N}1 > V_{1N}2$ state. 26 $V_{IN}1$ 2.0 V max 27 U phase Hall sensor input 27 $U_{\text{IN}}2$ Logic high is the $U_{IN}1 > U_{IN}2$ state. U_{IN}1 28

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