November 2004

National Semiconductor

LP3878
Micropower 800mA Low Noise "Ceramic Stable" Voltage Regulator for Low Voltage Applications
Designed for Use with Very Low ESR Output Capacitors

General Description

The LP3878 is a 800 mA fixed-output voltage regulator designed to provide high performance and low noise in applications requiring output voltages between 1.0V and 1.2V.

Output noise can be reduced to 18µV (typical) by connecting an external 10 nF capacitor to the bypass pin.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP3878 delivers superior performance:

Ground Pin Current: Typically 5 mA @ 800 mA load, and 180 µA @ 100 µA load.

Sleep Mode: The LP3878 draws less than 2.0 µA quiescent current when shutdown pin is pulled low.

Precision Output: Guaranteed output voltage accuracy is 1% at room temperature.

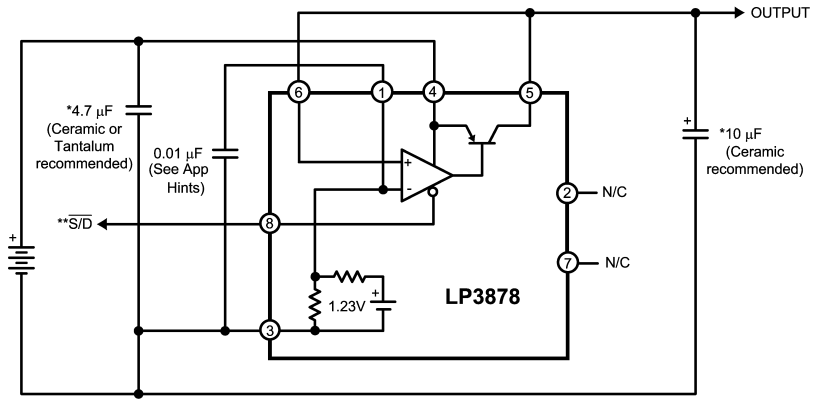
Features

- Standard output voltage: 1.00V
- Custom voltages available from 1.0V to 1.2V (50 mV increments)
- Input voltage: 2.2 to 6.0V
- 1% initial output accuracy
- Guaranteed 800 mA continuous output current
- Designed for use with low ESR ceramic capacitors
- Very low output noise with external capacitor
- Sense option improves load regulation
- 8 Lead LLP surface mount package
- <2.0 µA quiescent current in shutdown
- Low ground pin current at all loads
- High peak current capability (1200 mA typical)
- Overtemperature/overcurrent protection
- 0˚C to +125˚C junction temperature range

Applications

- ASIC Power Supplies In:
  - Desktops, Notebooks and Graphic Cards
  - Set Top Boxes, Printers and Copiers
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

Basic Application Circuit



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*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response. Output capacitor must meet ESR requirements (see Application Hints).

**Shutdown must be actively terminated (see App. Hints). Tie to INPUT (Pin4) if not used.

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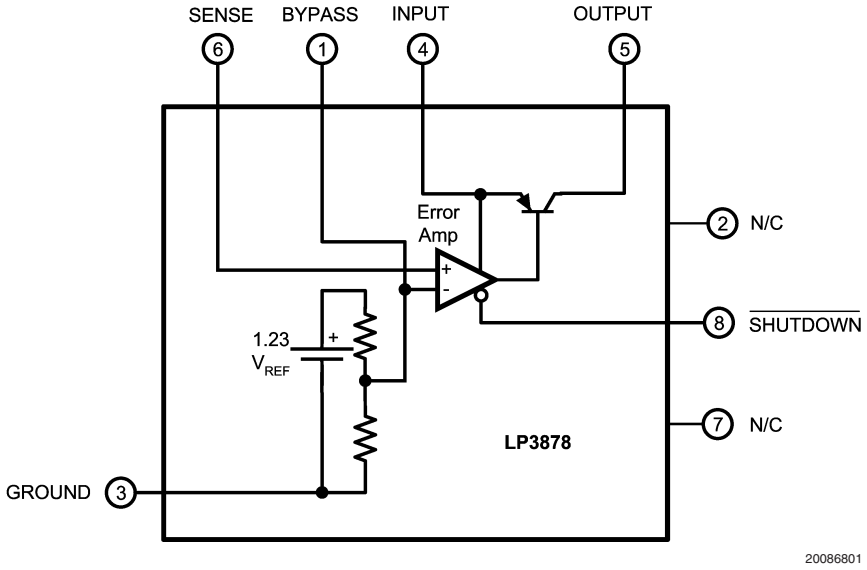
Block Diagram



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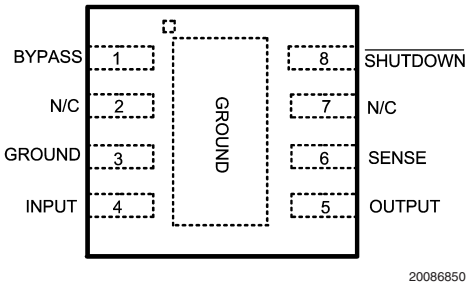
Connection Diagram

8 Lead LLP Surface Mount Package (SD)



Top View
See NS Package Number SDC08A

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage*	Grade	Order Information	Supplied as:
8 Lead LLP			
1.0	STD	LP3878SD-1.0	1000 Units on Tape and Reel
1.0	STD	LP3878SDX-1.0	4500 Units on Tape and Reel

* For other voltages between 1.0V and 1.2V, contact National Semiconductor sales office.

Pin Description

PIN	NAME	APPLICATION INFORMATION
1	BYPASS	Optional low noise feature. A small value capacitor connected between BYPASS and GROUND lowers output noise voltage level (100pF - 10nF).
2	N/C	DO NOT CONNECT. This pin is used for post package test and should be left floating.
3	GROUND	Device ground.
4	INPUT	Input source voltage.
5	OUTPUT	Regulated output voltage.
6	SENSE	Remote sense. Tie directly to output or remotely at point of load for best regulation.
7	N/C	No internal connection.
8	SHUTDOWN	Enabled above turn-on threshold voltage. Pull to ground to disable.
LLP DAP	SUBSTRATE	The exposed die attach pad should be connected to a thermal pad at ground potential. For additional information on using National Semiconductor's No Pull Back LLP package, please refer to LLP application note AN-1187.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	–65˚C to +150˚C
Operating Junction Temperature Range	-40˚C to +125˚C
Lead Temperature (Soldering, 5 seconds)	260˚C
ESD Rating (Note 2)	2 kV
Power Dissipation (Note 3)	Internally Limited
Input Supply Voltage (Survival)	–0.3V to +16V
Input Supply Voltage (Operating)	2.2V to 6V
Sense Pin	–0.3V to 6V
Output Voltage (Survival) (Note 4)	–0.3V to 6V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival) (Note 5)	–0.3V to +16V

Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the junction temperature range of 0˚C to 125˚C. Unless otherwise specified: V_{IN} = 3.3V, I_L = 1 mA, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Min (Note 6)	Typical (Note 7)	Max (Note 6)	Units
V_O	Output Voltage Tolerance		–1.0		1.0	$\%V_{NOM}$
		1 mA < I_L < 800 mA 3.0V ≤ V_{IN} ≤ 6V	–2.0		2.0	
			–3.0		**3.0**	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output Voltage Line Regulation	3.0V ≤ V_{IN} ≤ 6V		0.005	0.014	%/V
					0.032	
V_{IN} (min)	Minimum Input Voltage Required To Maintain Output Regulation	I_L = 800 mA $V_{OUT} \geq V_{OUT(NOM)}$ - 1%		2.2	**2.75**	V
I_{GND}	Ground Pin Current	I_L = 100 µA		180	200	µA
					225	
		I_L = 200 mA		1	2	mA
					2.5	
		I_L = 800 mA		5	8	
					10	
I_O(PK)	Peak Output Current	$V_{OUT} \geq V_O$(NOM) – 5%		1200		mA
I_O(MAX)	Short Circuit Current	R_L = 0 (Steady State) (Note 8)		1400		
e_n	Output Noise Voltage (RMS)	BW = 100 Hz to 100 kHz C_{BYPASS} = 10 nF C_{BYPASS} = 0		18 85		µV(RMS)
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	f = 1 kHz		70		dB
SHUTDOWN INPUT						
$V_{S/D}$	S/D Input Voltage	V_H = O/P ON		1.4	**1.6**	V
		V_L = O/P OFF I_{IN} ≤ 2 µA	**0.1**	0.50		
$I_{S/D}$	S/D Input Current	$V_{S/D}$ = 0		0.001	**–1**	µA
		$V_{S/D}$ = 5V		5	**15**	

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: ESD testing was performed using Human Body Model, a 100 pF capacitor discharged through a 1.5 kΩ resistor. The ESD rating of pin 8 is 1kV.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

The value θ_{J-A} for the LLP (SD) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 4: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP3878 output must be diode-clamped to ground.

Note 5: The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see Application Hints).

Note 6: Limits are guaranteed through testing, statistical correlation, or design.

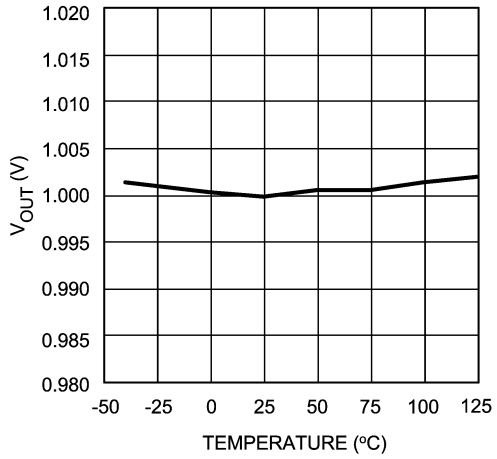
Note 7: Typical numbers reperesent the most likely parametric norm for 25˚C operation.

Note 8: See Typical Performance Characteristics curves.

Typical Performance Characteristics

Unless otherwise specified: T_A = 25˚C, C_{IN}= 4.7 µF, C_{OUT} = 10 µF, S/D is tied to V_{IN}, V_{IN} = 3.3V, I_L = 1 mA, V_{OUT} = 1.0V, C_{BYP} = 0.

V_{OUT} vs Temperature



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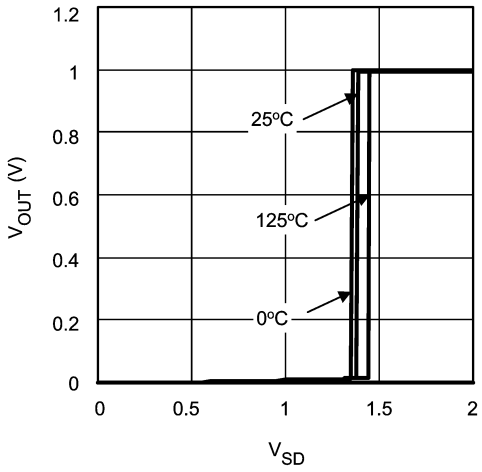
Turn-On Characteristics



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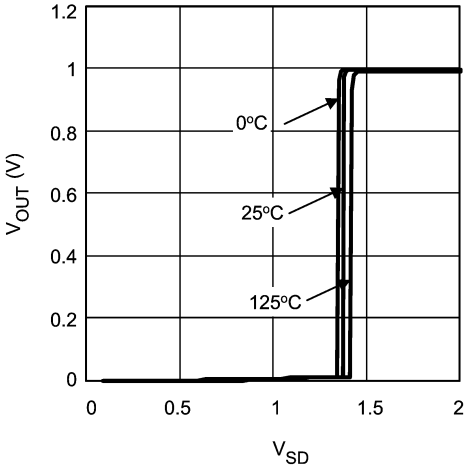
Turn-Off Characteristics



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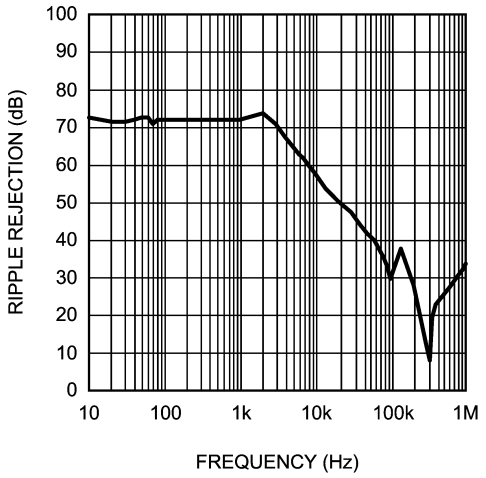
Ripple Rejection



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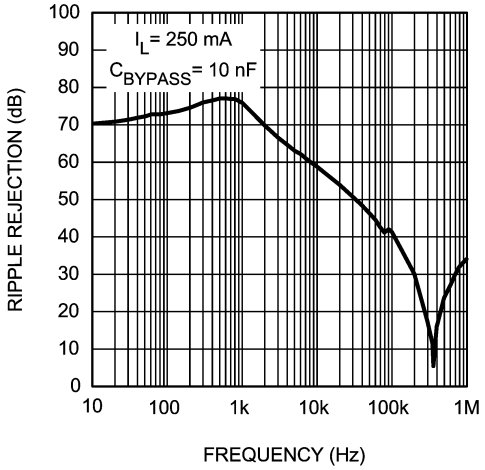
Ripple Rejection



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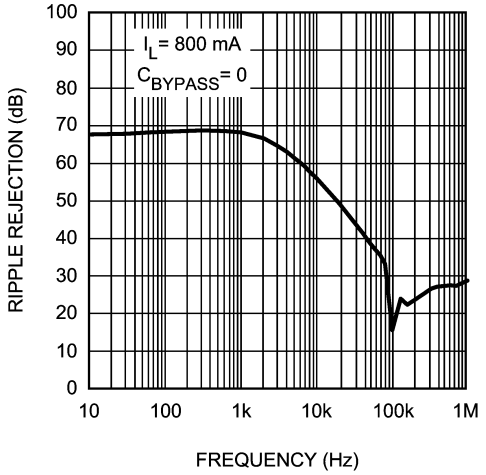
Ripple Rejection



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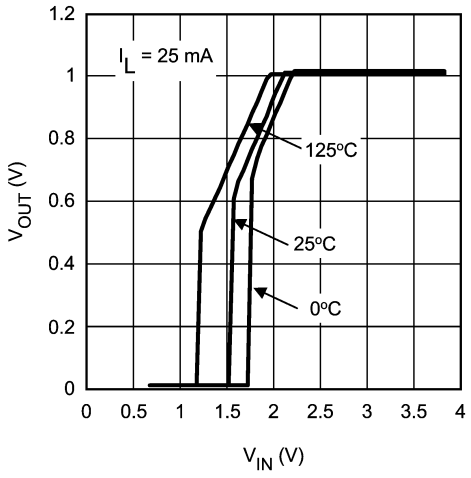
Typical Performance Characteristics

Unless otherwise specified: T_A = 25˚C, C_{IN}= 4.7 µF, C_{OUT} = 10 µF, S/D is tied to V_{IN}, V_{IN} = 3.3V, I_L = 1 mA, V_{OUT} = 1.0V, C_{BYP} = 0. (Continued)

MIN V_{IN} Over Temperature



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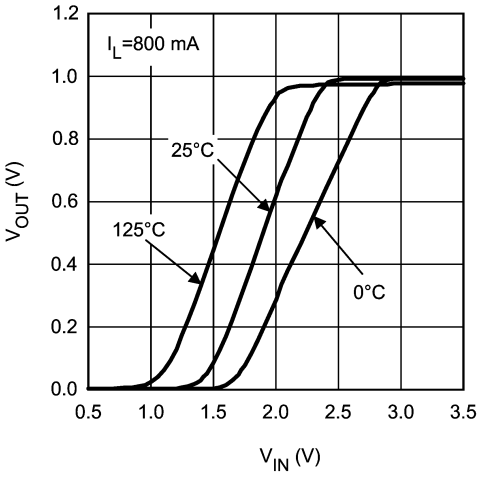
Min V_{IN} Over Temperature



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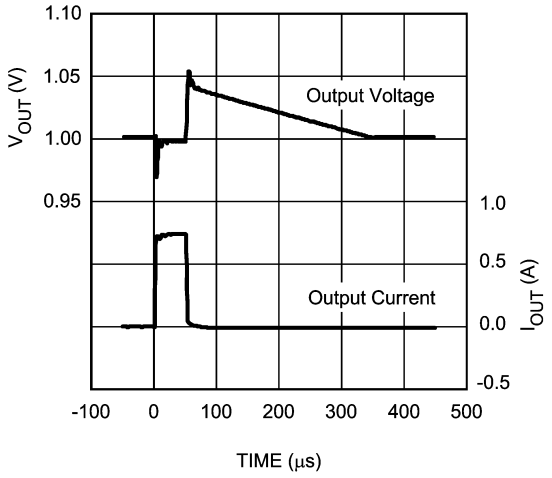
Load Transient Response (1mA to 800mA)



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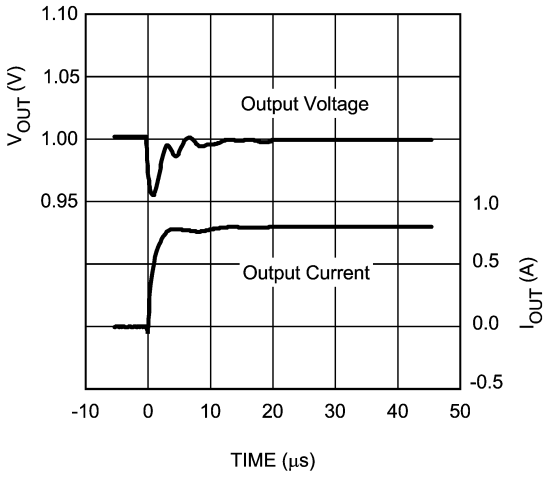
Load Transient Response (Expanded) (1mA to 800mA)



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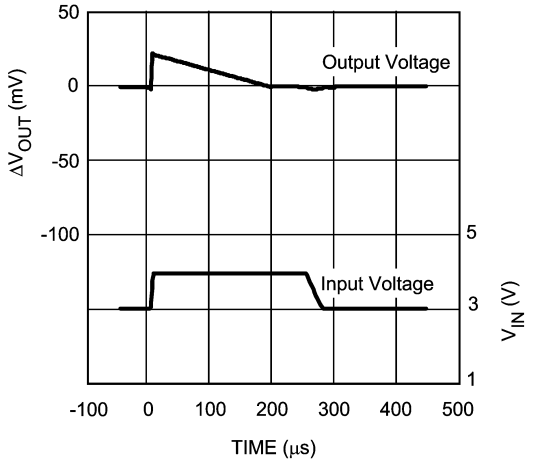
Line Transient Response



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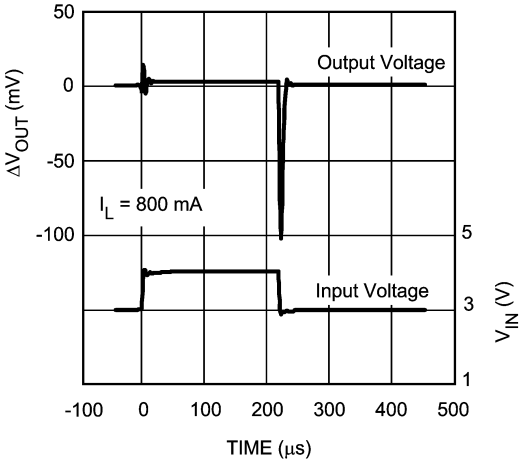
Line Transient Response



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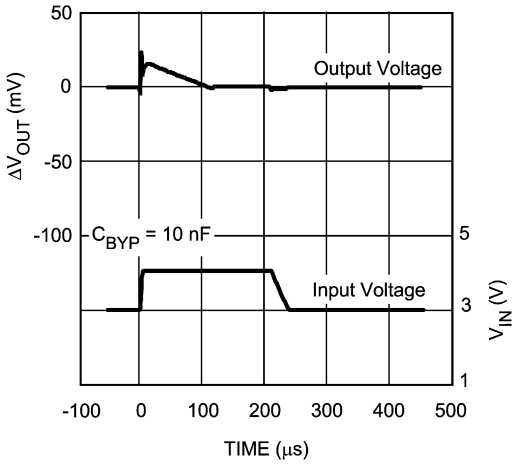
Typical Performance Characteristics Unless otherwise specified: T_A = 25˚C, C_{IN}= 4.7 µF, C_{OUT} = 10 µF, S/D is tied to V_{IN}, V_{IN} = 3.3V, I_L = 1 mA, V_{OUT} = 1.0V, C_{BYP} = 0. (Continued)

Line Transient Response



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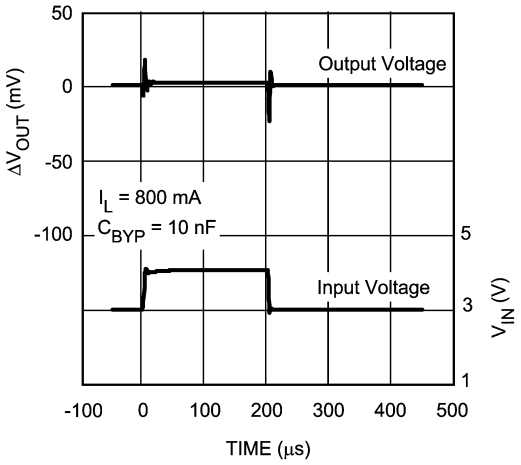
Line Transient Response



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Application Hints

LLP PACKAGE DEVICES

The LP3878 is offered in the 8 lead LLP surface mount package to allow for increased power dissipation compared to the SO-8 and Mini SO-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3878 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor whose capacitance is at least 4.7 µF is required between the LP3878 input and ground (the amount of capacitance may be increased without limit).

Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see **Capacitor Characteristics** section) to assure the minimum requirement of input capacitance is met over all operating conditions.

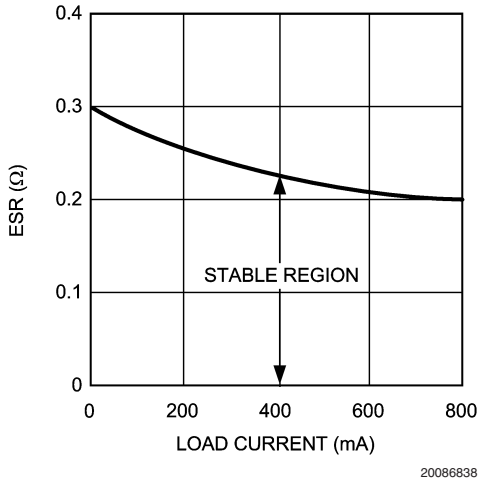
The input capacitor must be located at a distance of not more than 0.5" from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor, assuming the minimum capacitance requirement is met.

Output Capacitor

The LP3878 requires a ceramic output capacitor whose size is at least 10 µF. Capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor.

The LP3878 is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an ultra low ESR output capacitor.

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (equivalent series resistance) value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see ESR graph below). Because an internal zero is built into the error amplifier, the LP3878 is stable with output capacitor ESR values down to zero ohms.



Stable Region For Output Capacitor ESR

Important: The output capacitor must maintain its ESR within the stable region *over the full operating temperature range of the application* to assure stability.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range (See Capacitor Characteristics section).

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground.

Noise Bypass Capacitor

Connecting a 10 nF capacitor to the Bypass pin significantly reduces noise on the regulator output. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10 nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Capacitor Characteristics

Ceramic

The LP3878 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 10 µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 10 µF ceramic capacitor is in the range of 5 mΩ to 10 mΩ, which meets the ESR limits required for stability by the LP3878.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25˚C to 85˚C.

Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP3878.

SHUTDOWN INPUT OPERATION

The LP3878 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to V_{IN} to keep the regulator output on at all times.

Application Hints (Continued)

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the Electrical Characteristics section under $V_{ON/OFF}$.

REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP3878 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

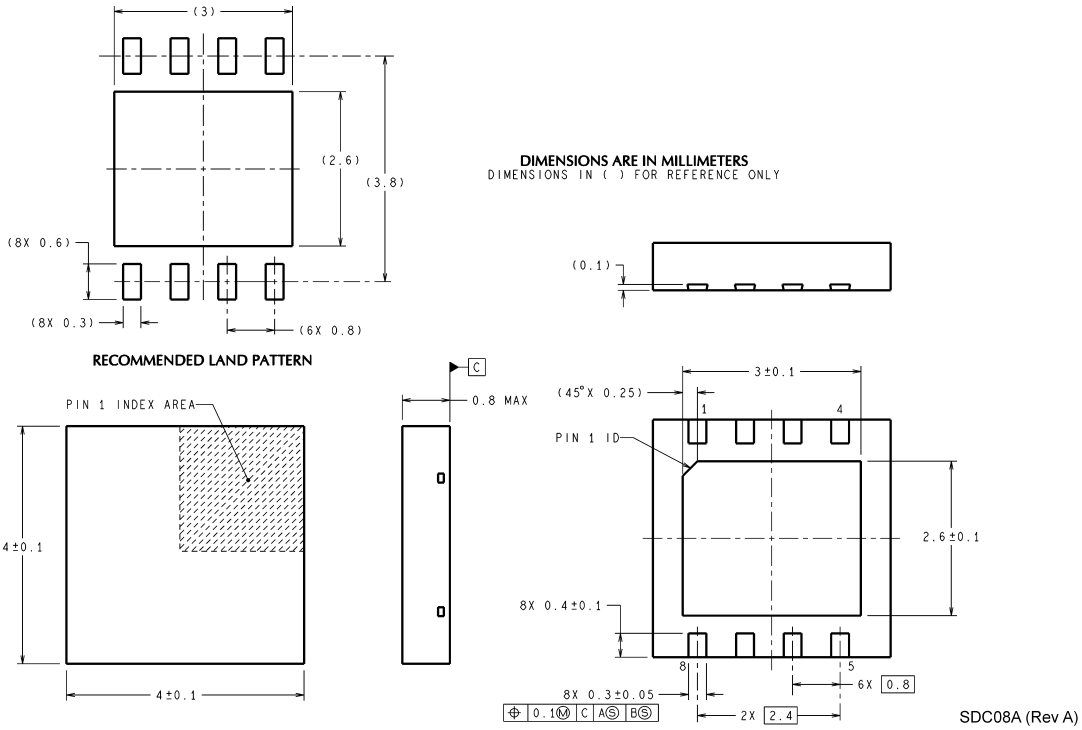
However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP3878 to 0.3V (see Absolute Maximum Ratings).

Physical Dimensions inches (millimeters)

unless otherwise noted



8 Lead LLP Surface Mount Package
NS Package Number SDC08A

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