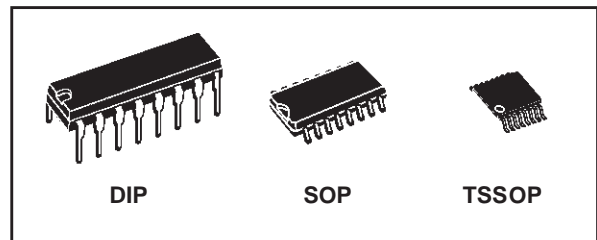




M74HC4316

QUAD BILATERAL SWITCH

- HIGH SPEED:
 $t_{PD} = 13\text{ns}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 1\mu\text{A}$ (MAX.) at $V_{CC} = 5\text{V}$
- LOW "ON" RESISTANCE:
 120Ω TYP. ($V_{CC} - V_{EE} = 2\text{V}$)
 50Ω TYP. ($V_{CC} - V_{EE} = 4.5\text{V}$)
 35Ω TYP. ($V_{CC} - V_{EE} = 9\text{V}$)
- WIDE ANALOG INPUT VOLTAGE RANGE $\pm 6\text{V}$
- LOW CROSSTALK BETWEEN SWITCHES
- FAST SWITCHING
- SINE WAVE DISTORTION:
 0.020 at $V_{CC} - V_{EE} = 9\text{V}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 4316



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC4316B1R	
SOP	M74HC4316M1R	M74HC4316RM13TR
TSSOP		M74HC4316TTR

DESCRIPTION

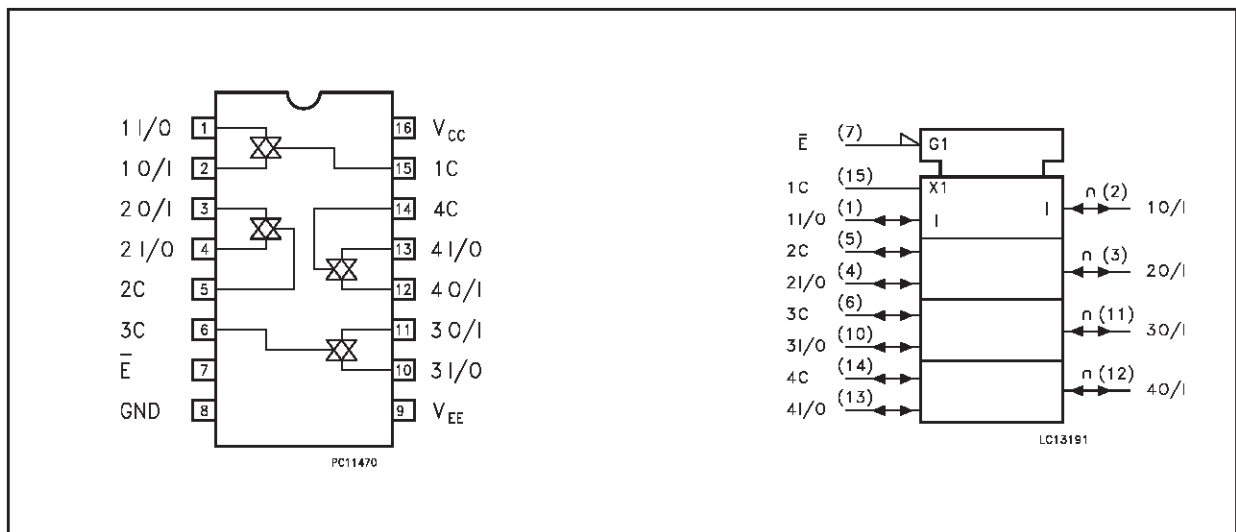
The M74HC4316 is an high speed CMOS QUAD BILATERAL SWITCH fabricated with silicon gate C²MOS technology.

This device has four independent analogue switches. Each switch has two input/output terminals (nI/O, nO/I) and an active high select input (nC).

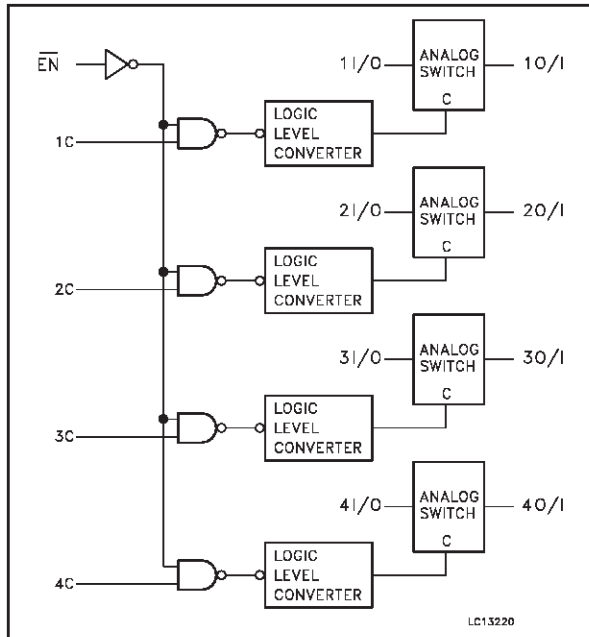
When the enable input is high, all four analog switches are off. The supply voltage for the digital signals applied to V_{CC} and GND must be within the range 0 to 6 V. The voltage swing on the analogue Inputs/Outputs can be between V_{CC} (positive limit) and V_{EE} (negative limit). The voltage between V_{CC} and V_{EE} must not exceed 12V.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1 to 4 I/O	Independent Inputs/Outputs
2, 3, 11, 12	1 to 4 O/I	Independent Outputs/Inputs
7	\bar{E}	Enable Inputs (Active LOW)
15, 5, 6, 14	1C to 4C	Enable Inputs (Active High)
9	V_{EE}	Negative Supply Voltage
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

\bar{E}	C	SWITCH FUNCTION
L	H	ON
L	L	OFF
H	X	OFF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
$V_{CC} - V_{EE}$	Supply Voltage	-0.5 to +13	V
V_I	Control Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_{I/O}$	Switch Input/Output Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 $^{\circ}C$; derate to 300mW by 10mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 85 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 12	V	
V_{EE}	Supply Voltage	-6 to 0	V	
$V_{CC} - V_{EE}$	Supply Voltage	2 to 12	V	
V_I	Input Voltage	0 to V_{CC}	V	
$V_{I/O}$	Switch I/O Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	
		$V_{CC} = 6.0V$	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)	V_{EE} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V_{IHC}	High Level Control Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{ILC}	Low Level Control Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
R_{ON}	ON Resistance	4.5	GND	$V_I = V_{IHC}$ $V_{I/O} = V_{CC} \text{ to } V_{EE}$ $I_{I/O} = 0.1\text{mA}$		70	170		200			Ω
		4.5	-4.5			50	85		105			
		6.0	-6.0			30	70		85			
		2.0	GND	$V_I = V_{IHC}$ $V_{I/O} = V_{CC} \text{ or } V_{EE}$ $I_{I/O} = 0.1\text{mA}$		120	180		215			
		4.5	GND			50	80		100			
		4.5	-4.5			35	60		75			
		6.0	-6.0			20	40		60			
ΔR_{ON}	Difference of ON Resistance between switches	4.5	GND	$V_{IN} = V_{IHC} \text{ or } V_{ILC}$		10	15		20			Ω
		4.5	-4.5	$V_{I/O} = V_{CC} \text{ to } V_{EE}$		5	10		15			
		6.0	-6.0	$I_{I/O} = 0.1\text{mA}$		5	10		15			
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	6.0	GND	$V_{OS} = V_{CC} \text{ or } GND$			± 0.06		± 0.6		± 2	μA
		6.0	-6.0	$V_{IS} = V_{CC} \text{ or } GND$ $V_{IN} = V_{IHC} \text{ or } V_{ILC}$			± 0.1		± 1		± 2	
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	6.0	GND	$V_{OS} = V_{CC} \text{ or } GND$			± 0.06		± 0.6		± 2	μA
		6.0	-6.0	$V_{IN} = V_{IHC} \text{ or } V_{ILC}$			± 0.1		± 1		± 2	
I_{IN}	Control Input Current	6.0		$V_I = V_{CC} \text{ or } GND$		10^{-5}	± 0.1		± 1		± 1	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)	V_{EE} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$\Phi_{I/O}$	Phase Difference Between Input and Output	2.0	GND			12	30		40			ns
		4.5	GND			3	6		8			
		6.0	GND			3	5		7			
		4.5	-4.5			2	4		5			
		6.0	-6.0			2	4		5			
t_{PZL} t_{PZH}	Output Enable Time (E, C - OUT)	2.0	GND	$R_L = 1\text{K}\Omega$		56	115		145			ns
		4.5	GND			14	23		29			
		6.0	GND			12	20		25			
		4.5	-4.5			13	21		26			
		6.0	-6.0			11	18		23			
t_{PLZ} t_{PHZ}	Output Disable Time (E, C - OUT)	2.0	GND	$R_L = 1\text{K}\Omega$		112	205		255			ns
		4.5	GND			28	41		51			
		6.0	GND			24	35		43			
		4.5	-4.5			24	34		43			
		6.0	-6.0			21	29		36			
f_{MAX}	Maximum Control Input Frequency	2.0	GND	$R_L = 1\text{K}\Omega$ $C_L = 15 \text{ pF}$ $V_{OUT} = 1/2 V_{CC}$		2						MHz
		4.5	GND			9						
		6.0	GND			11						

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)			$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance					5	10		10		10	pF
$C_{I/O}$	Switch Terminal Capacitance	4.5	-4.5			5						pF
C_{IOS}	Feed Through Capacitance	4.5	-4.5			1						pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	GND			16						pF

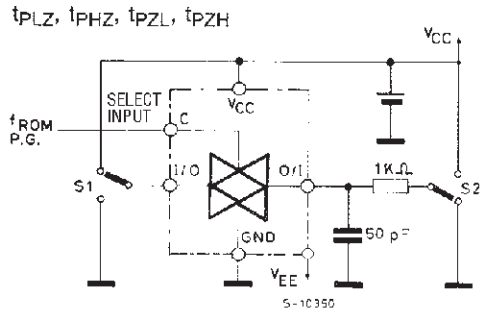
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

ANALOG SWITCH CHARACTERISTICS (GND = 0V; T_A = 25°C)

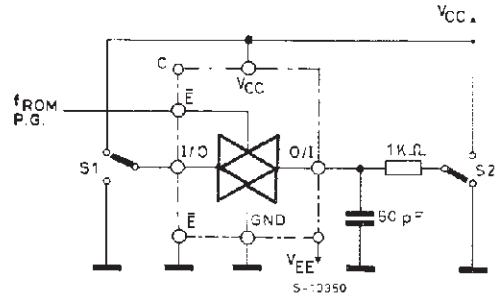
Symbol	Parameter	Test Condition			Value	Unit
		V _{CC} (V)	V _{EE} (V)	V _{IN} (V _{p-p})		
	Sine Wave Distortion (THD)	2.25	2.25	4	f _{IN} = 1 KHz R _L = 10 KΩ, C _L = 50 pF	0.025
		4.5	4.5	8		0.020
		6.0	6.0	11		0.018
f _{MAX}	Frequency Response (Switch ON)	2.25	2.25	Adjust f _{IN} voltage to obtain 0 dBm at V _{OS} . Increase f _{IN} Frequency until dB meter reads -3dB R _L = 50Ω, C _L = 10 pF, f _{IN} = 1MHz sine wave	28	MHz
		4.5	4.5		42	
		6.0	6.0		43	
	Feed through Attenuation (Switch OFF)	2.25	2.25	V _{IN} is centered at V _{CC} /2. Adjust input for 0 dBm R _L = 600Ω, C _L = 50 pF, f _{IN} = 1MHz sine wave	-50	dB
		4.5	4.5		-50	
		6.0	6.0		-50	
	Crosstalk (Control Input to Signal Output)	2.25	2.25	R _L = 600Ω, C _L = 50 pF, f _{IN} = 1MHz square wave (t _r = t _f = 6ns)		mV
		4.5	4.5		5	
		6.0	6.0			
	Crosstalk (Between Any Switches)	2.25	2.25	Adjust V _{IN} to Obtain 0 dBm at input R _L = 600Ω, C _L = 50 pF, f _{IN} = 1MHz sine wave	-50	dB
		4.5	4.5		-50	
		6.0	6.0		-50	

SWITCHING CHARACTERISTICS TEST CIRCUIT

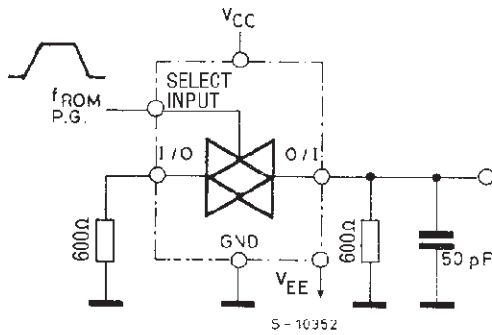
CONTROL



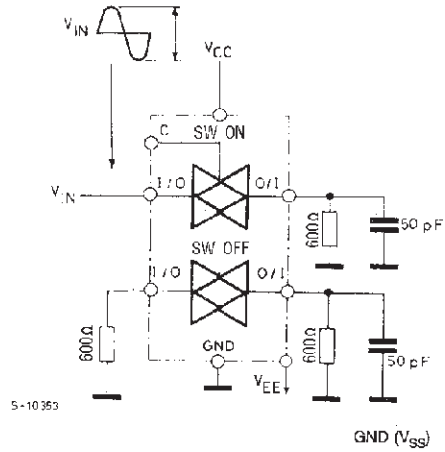
ENABLE



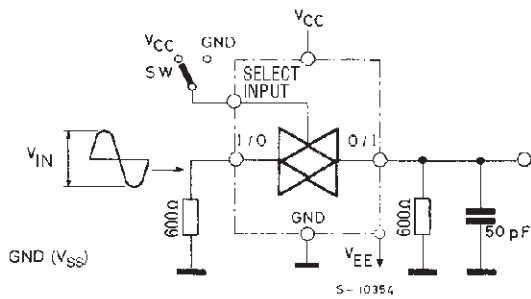
CROSSTALK (control to output)



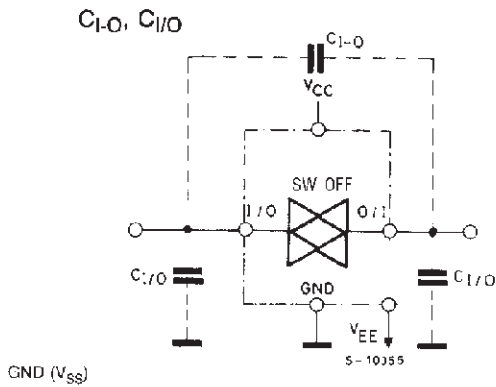
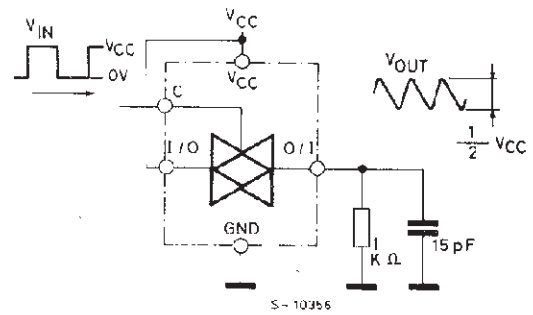
CROSSTALK BETWEEN ANY TWO SWITCHES



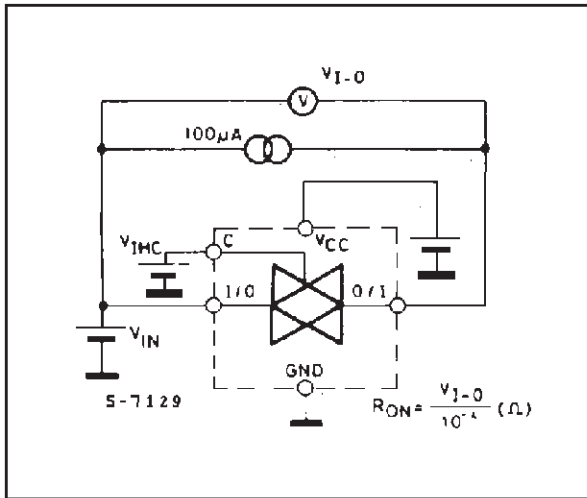
BANDWIDTH AND FEEDTHROUGH ATTENUATION



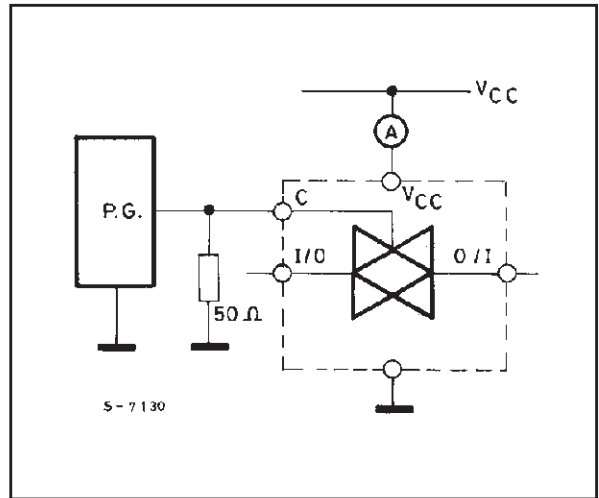
MAXIMUM CONTROL FREQUENCY



CHANNEL RESISTANCE (R_{ON})

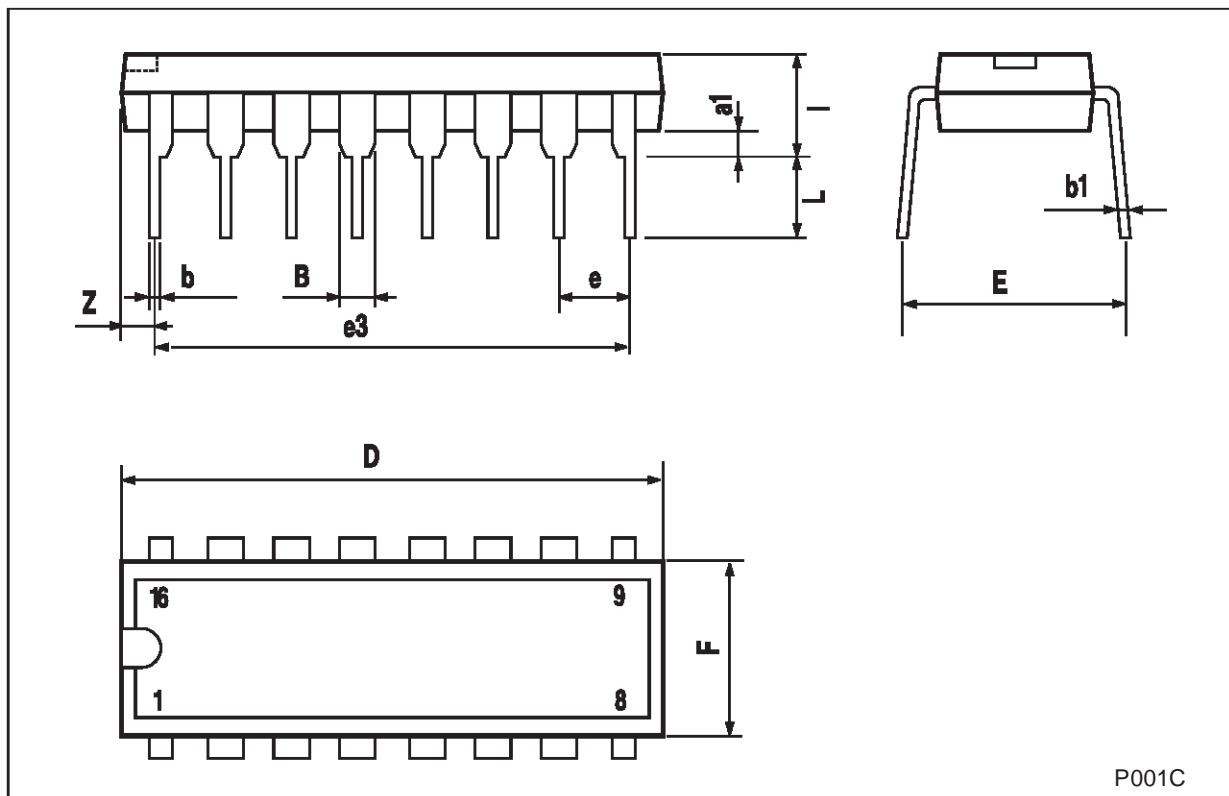


I_{CC} (Opr.)



Plastic DIP-16 (0.25) MECHANICAL DATA

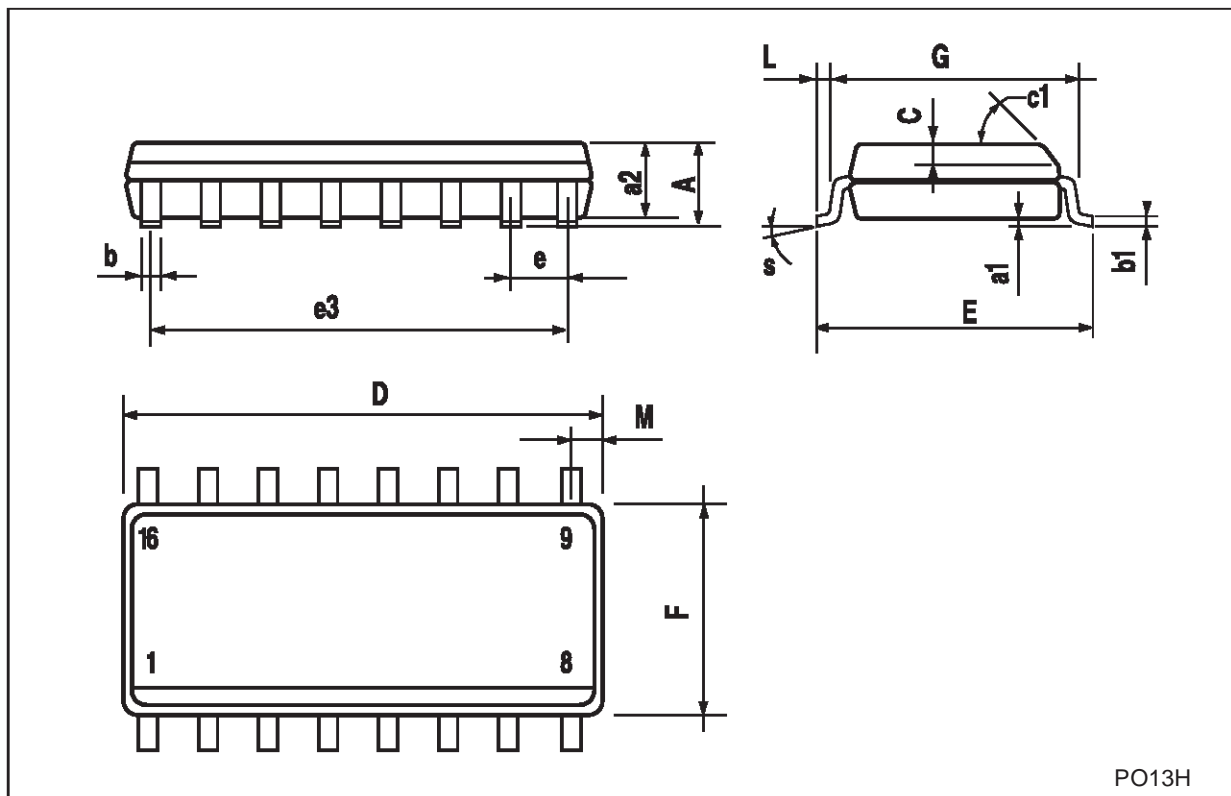
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

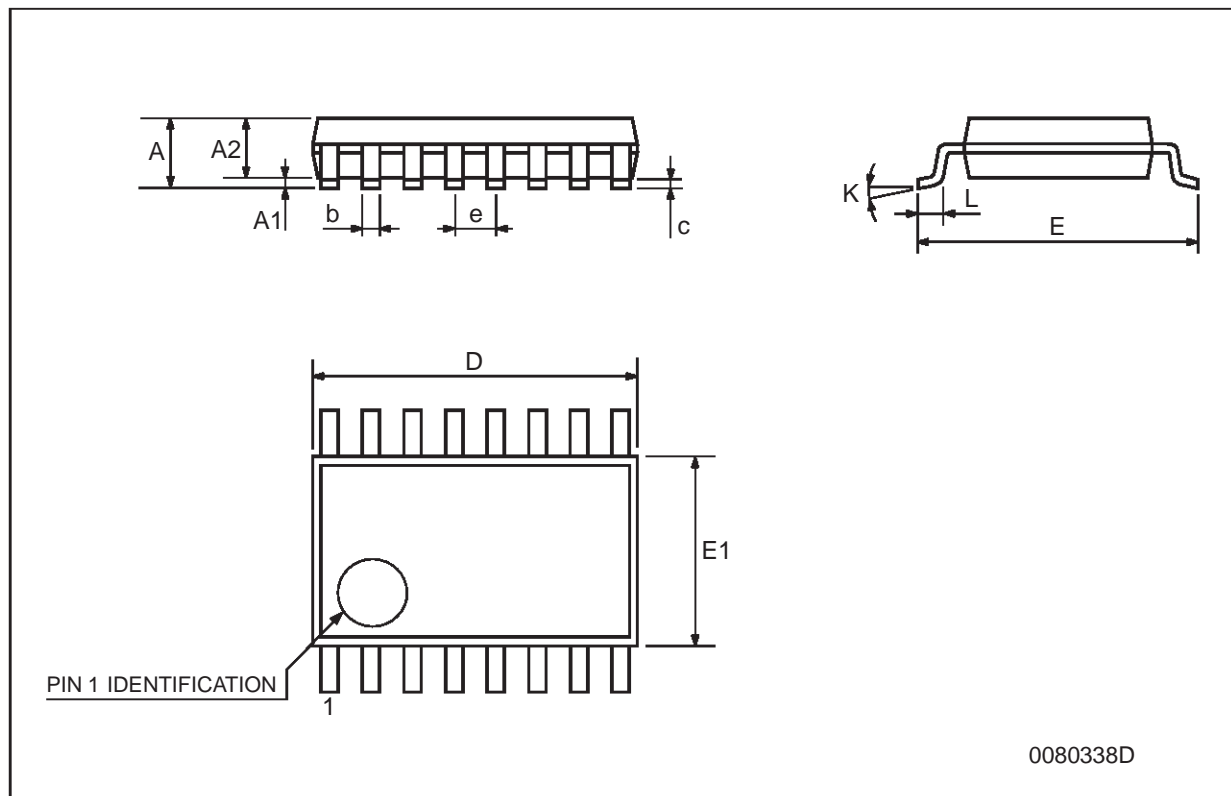
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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