19-2409; Rev 1; 9/02

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

General Description

The MAX9600/MAX9601/MAX9602 ultra-high-speed comparators feature extremely low propagation delay (500ps). These dual and quad comparators minimize propagation delay skew (10ps) and are designed for low propagation delay dispersion (30ps). These features make them ideal for applications where high-fidelity tracking of narrow pulses and low timing dispersion is critical.

The differential input stage accepts a wide range of signals in the common-mode range from (V_{EE} + 3V) to (V_{CC} - 2V). The outputs are complementary digital signals, compatible with ECL and PECL systems, and provide sufficient current to directly drive transmission lines terminated in 50Ω.

The MAX9600/MAX9601 dual-channel ECL and dual-channel PECL output comparators incorporate latch enable (LE_, $\overline{LE\_}$), and hysteresis (HYS_). The complementary latch-enable control permits tracking, track-hold, or sample-hold mode of operations. The latch enables can be driven with standard ECL logic for MAX9600 and PECL logic for MAX9601. The MAX9602 quad-channel PECL output comparator is ideal for high-density packaging in limited board space.

The MAX9600/MAX9601 are available in 20-pin TSSOP packages, and the MAX9602 is offered in a 24-pin TSSOP package. The MAX9600/MAX9601/MAX9602 are specified for operation from -40°C to +85°C.

Applications

VLSI and High-Speed Memory ATE

High-Speed Instrumentation

Scope/Logic Analyzer Front Ends

High-Speed Triggering

Threshold and Peak Detection

Line Receiving/Signal Restoration

Features

- ♦ 500ps Propagation Delay
- ♦ 30ps Propagation Delay Dispersion
- ♦ 4Gbps Tracking Frequency
- ♦ -2.2V to +3V Input Range with +5V/-5.2V Supplies
- ♦ -1.2V to +4V Input Range with +6V/-4.2V Supplies
- ♦ Differential ECL Outputs (MAX9600)
- ♦ Differential PECL Outputs (MAX9601/MAX9602)
- ♦ Latch Enable (MAX9600/MAX9601)
- ♦ Adjustable Hysteresis (MAX9600/MAX9601)

Ordering Information

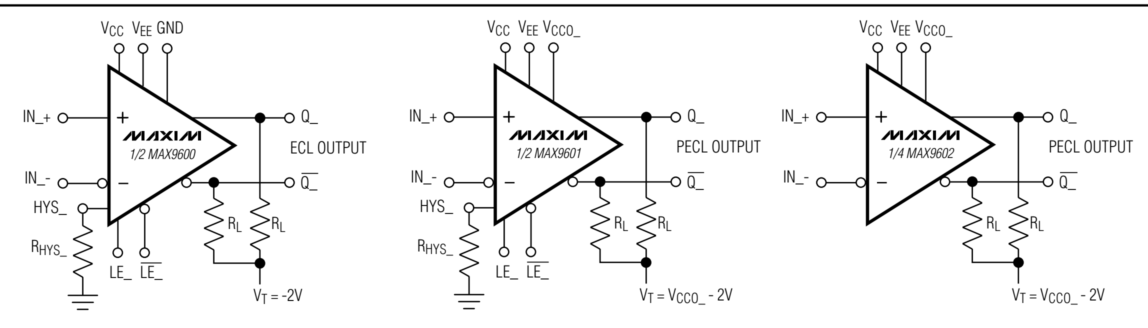
PART	TEMP RANGE	PIN-PACKAGE
MAX9600EUP	-40°C to +85°C	20 TSSOP
MAX9601EUP	-40°C to +85°C	20 TSSOP
MAX9602EUG	-40°C to +85°C	24 TSSOP

Selector Guide

PART	PIN-PACKAGE	SELECTION
MAX9600EUP	20 TSSOP	Dual ECL Output Comparator with Latch Enable and Hysteresis
MAX9601EUP	20 TSSOP	Dual PECL Output Comparator with Latch Enable and Hysteresis
MAX9602EUG	24 TSSOP	Quad PECL Output Comparator

Pin Configurations appear at end of data sheet.

Functional Diagrams



THE OPEN-EMITTER OUTPUTS REQUIRE EXTERNAL PULLDOWN RESISTORS (R_L). USE RESISTORS IN THE RANGE OF 50Ω TO 75Ω CONNECTED TO V_T.
CURRENT-CONTROLLED HYSTERESIS REQUIRES A SINGLE EXTERNAL RESISTOR ($R_{HYS\_}$) FROM HYS_ TO GND IN THE RANGE OF 10kΩ TO 35kΩ.

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

ABSOLUTE MAXIMUM RATINGS

$V_S = V_{CC} - V_{EE}$ 12.0V
V_{CC} to GND (MAX9600) 6.8V
V_{EE} to GND (MAX9600) ....-6.5V
Differential Input Voltage ....±6.5V
Latch Differential Voltage ....±4V
Common-Mode Input Voltage (V_{CM}) ....V_{EE} to V_{CC}
$V_{CCO\_}$ to V_{EE}
(MAX9601/MAX9602)....................(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
LE_, $\overline{LE}$_ to GND
MAX9600 ....(V_{EE} - 0.3V) to 0.3V
MAX9601 ....(V_{EE} - 0.3V) to ($V_{CCO\_}$ + 0.3V)

Input Current to Any Input Pin....................10mA
HYS_ Current (MAX9600/MAX9601) ....-1mA
Continuous Output Current 50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
24-Pin TSSOP (derate 12.2mW/°C above +70°C) 975mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE}$_ = high (MAX9600/MAX9601), GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT (IN_+, IN_-)							
Input Differential Voltage Range	V_{ID}	Guaranteed by input bias current tests		-5.2		+5.2	V
Input Common-Mode Voltage	V_{CM}	Guaranteed by input bias current tests		V_{EE} + 3		V_{CC} - 2	V
Input Offset Voltage	V_{OS}	T_A = +25°C			±1	±5	mV
		$T_{MIN} \le T_A \le T_{MAX}$				±9	
Input Offset-Voltage Tempco	TCV_{OS}				8		µV/°C
Input Offset-Voltage Channel Matching					1		mV
Input Bias Current	I_B	V_{ID} = ±5.2V			6	20	µA
Input Bias-Current Tempco	TCI_B				10		nA/°C
Input Offset Current	I_{OS}				0.3	±5	µA
Input Resistance	R_{IN}	Differential mode (V_{ID} ≤ 10mV)			10		kΩ
		Common mode (V_{EE} + 3V) ≤ V_{CM} ≤ (V_{CC} - 2V)			100		MΩ
LATCH INPUT (LE_, $\overline{LE}$_)							
Latch Differential Input Voltage	V_{LD}	Guaranteed by latch input current	MAX9600	0.4		2.0	V
			MAX9601	0.25		3.50	
Latch Input Voltage Range	V_{LR}	MAX9600		-2		0	V
		MAX9601	$V_{CCO\_}$ ≥ 3.5V	$V_{CCO\_}$ - 3.5		$V_{CCO\_}$	
			$V_{CCO\_}$ < 3.5V	0		$V_{CCO\_}$	
Latch Input Current	I_{LE}, $I_{\overline{LE}}$	MAX9600			5	20	µA
		MAX9601			5	20	
HYSTERESIS INPUT (HYS_)							
Input-Referred Hysteresis		MAX9600/MAX9601	R_{HYS} = ∞		0		mV
			R_{HYS} = 16.4kΩ		30		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT (Q_, $\overline{Q\_}$)							
Logic Output High Voltage	V_{OH}	T_A = +25°C	MAX9600	-1.10	-0.94	-0.75	V
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.10	$V_{CCO\_}$ - 0.94	$V_{CCO\_}$ - 0.75	
		T_A = T_{MIN}	MAX9600	-1.2	-1.02	-0.8	
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.2	$V_{CCO\_}$ - 1.02	$V_{CCO\_}$ - 0.8	
		T_A = T_{MAX}	MAX9600	-1.05	-0.87	-0.70	
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.05	$V_{CCO\_}$ - 0.87	$V_{CCO\_}$ - 0.70	
Logic Output Low Voltage	V_{OL}	T_A = +25°C	MAX9600	-1.95	-1.72	-1.55	V
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.95	$V_{CCO\_}$ - 1.72	$V_{CCO\_}$ - 1.55	
		T_A = T_{MIN}	MAX9600	-2.0	-1.78	-1.6	
			MAX9601/MAX9602	$V_{CCO\_}$ - 2.0	$V_{CCO\_}$ - 1.78	$V_{CCO\_}$ - 1.6	
		T_A = T_{MAX}	MAX9600	-1.9	-1.66	-1.50	
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.9	$V_{CCO\_}$ - 1.66	$V_{CCO\_}$ - 1.5	
SUPPLY							
Positive Supply Voltage	V_{CC}	Guaranteed by output swing tests		4.3	5	6.3	V
Negative Supply Voltage	V_{EE}	Guaranteed by output swing tests		-6	-5.2	-4	V
Supply Voltage Difference	V_S	V_S = (V_{CC} - V_{EE}), guaranteed by output swing tests		9.5		11.5	V
Logic Supply Voltage	$V_{CCO\_}$	MAX9601/MAX9602		2.4		V_{CC}	V
Positive Supply Current	I_{CC}	(Note 2)	MAX9600		16	24	mA
			MAX9601		19	27	
			MAX9602		28	39	
Negative Supply Current	I_{EE}	(Note 2)	MAX9600		21	28	mA
			MAX9601		24	33	
			MAX9602		38	49	
Power-Supply Dissipation	P_{DISS}	(Note 2)	MAX9600		190	266	mW
			MAX9601		220	307	
			MAX9602		338	450	
Common-Mode Rejection Ratio	CMRR	(V_{EE} + 3V) ≤ V_{CM} ≤ (V_{CC} - 2V)			70		dB
Power-Supply Rejection Ratio	PSRR	4.3V ≤ V_{CC} ≤ 6.3V, -6V ≤ V_{EE} ≤ -4V, 9.5V ≤ V_S ≤ 11.5V			65		dB

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

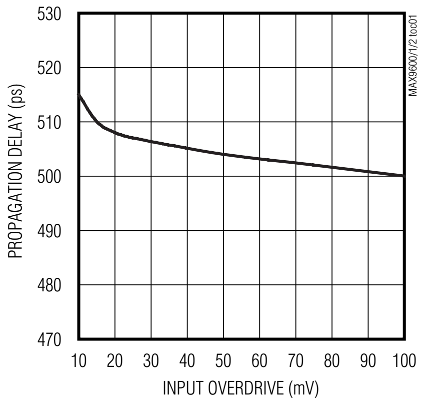
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tracking Frequency Toggle Rate	f_{MAX}	V_{OUT} = 550mV_{P-P}, input overdrive = 100mV		4		Gbps
Minimum Pulse Width	t_{PW}	V_{OUT} = 550mV_{P-P}, input overdrive = 100mV		250		ps
Propagation Delay	t_{PD-}, t_{PD+}	Input overdrive = 100mV, Figure 1, (Note 3)		500	700	ps
Propagation Delay Tempco	TCt_{PD}			0.5		ps/°C
Propagation Delay Skew	t_{PDSKEW}	Input overdrive = 100mV (Note 4)		10		ps
Propagation Delay Match		Input overdrive = 100mV (Note 5)		40		ps
Propagation Delay Dispersion Overdrive		10mV to 100mV		15		ps
		100mV to 2V		40		ps
Propagation Delay Dispersion Common-Mode Voltage		V_{IN} = 1V_{P-P} input overdrive = 100mV; (V_{EE} + 3V) ≤ V_{CM} ≤ (V_{CC} - 2V)		10		ps
Propagation Delay Dispersion Input Slew Rate		V_{IN} = 1V_{P-P} input overdrive = 100mV; 0.2V/ns to 10V/ns		40		ps
Propagation Delay Dispersion Duty Cycle		V_{IN} = 1V_{P-P} input overdrive = 100mV; 10% to 90% at 250MHz		30		ps
Propagation Delay Dispersion Pulse Width		V_{IN} = 1V_{P-P} input overdrive = 100mV; 350ps to 1ns		20		ps
Unit-to-Unit Propagation Delay Match		Input overdrive = 100mV		50		ps
Output Jitter		V_{IN} = 2V_{P-P}; 50MHz		300		fs
Input Capacitance	C_{IN}	IN_+ or IN_, with respect to GND		2		pF
Latch Setup Time	t_{LS}	Figure 1, (Notes 3, 6)	250	80		ps
Latch Hold Time	t_{LH}	Figure 1, (Notes 3, 6)	300	85		ps
Minimum Pulse Width	t_{LPW}	Figure 1		250		ps
Latch to Output Delay	t_{LPD}	Figure 1		200		ps
Rise Time and Fall Time	t_R, t_F	20% to 80%, Figure 1		200		ps

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Does not include output state current in Q_, $\overline{Q\_}$.
Note 3: Guaranteed by design.
Note 4: Propagation delay skew (t_{PDSKEW}) is for a single channel and is the difference between the propagation delay to the high-to-low output transition vs. the low-to-high output transition.
Note 5: Propagation delay match is the difference of t_{PD-} or t_{PD+} of one channel to the t_{PD-} or t_{PD+} of another channel of the same device.
Note 6: Latch setup and hold-timing specifications are for a differentially driven latch signal.

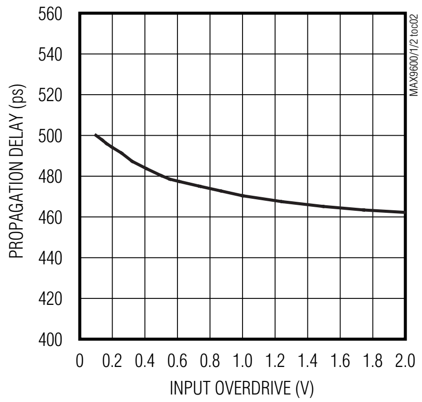
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS _ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), input slew rate = 2V/ns, duty cycle = 50%, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

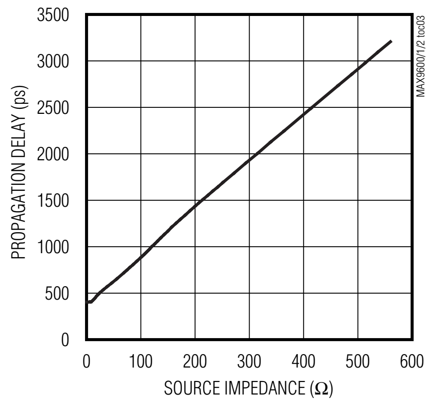
PROPAGATION DELAY vs. INPUT OVERDRIVE (V_{CC} = 10mV TO 100mV)



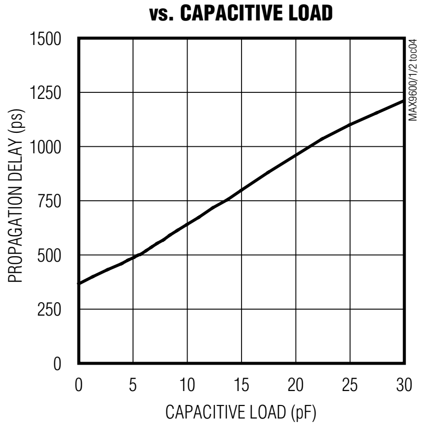
PROPAGATION DELAY vs. INPUT OVERDRIVE (V_{OD} = 0.1V TO 2V)



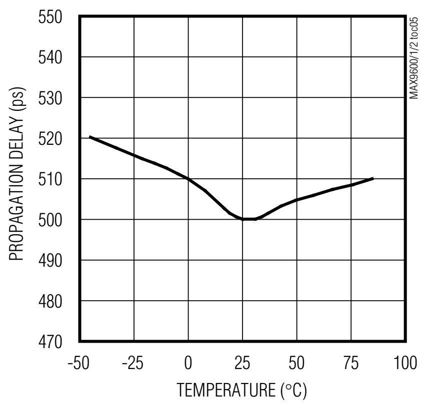
PROPAGATION DELAY vs. SOURCE IMPEDANCE



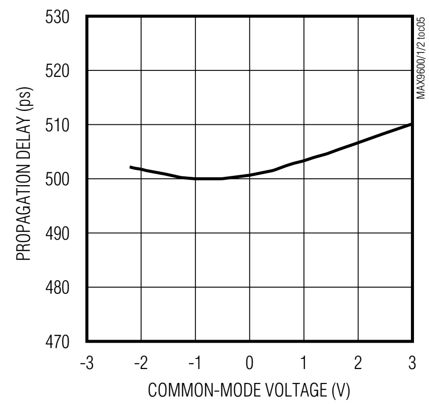
PROPAGATION DELAY vs. CAPACITIVE LOAD



PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. COMMON-MODE VOLTAGE

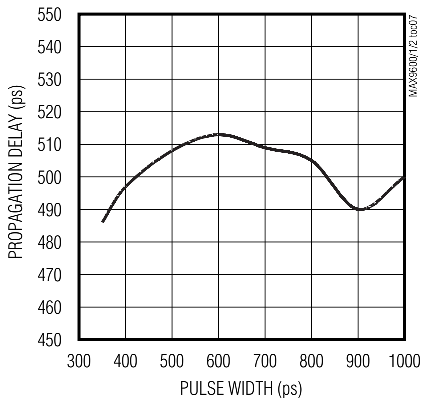


Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

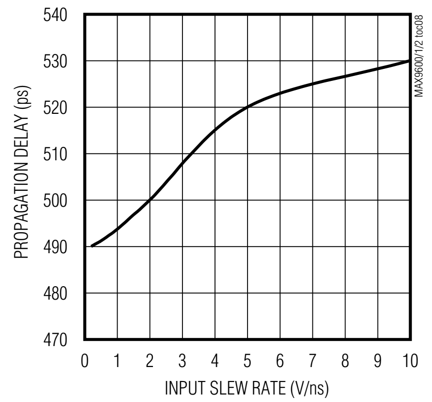
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS _ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), input slew rate = 2V/ns, duty cycle = 50%, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

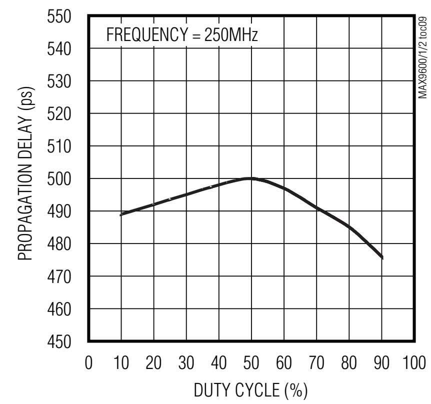
PROPAGATION DELAY vs. PULSE WIDTH



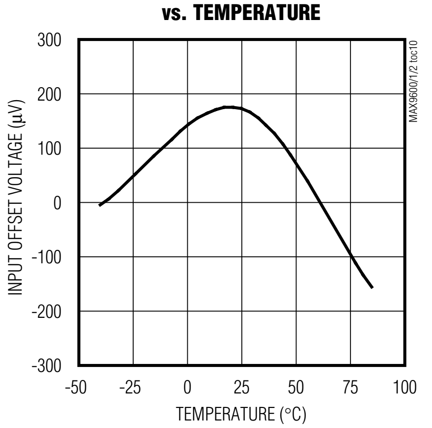
PROPAGATION DELAY vs. INPUT SLEW RATE



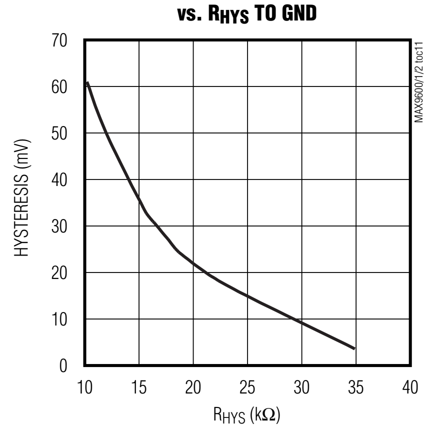
PROPAGATION DELAY vs. DUTY CYCLE



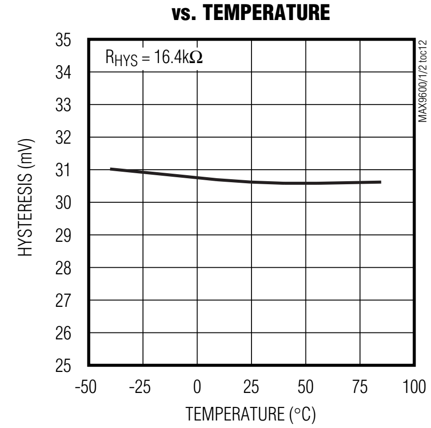
INPUT OFFSET VOLTAGE vs. TEMPERATURE



HYSTERESIS vs. R_{HYS} TO GND



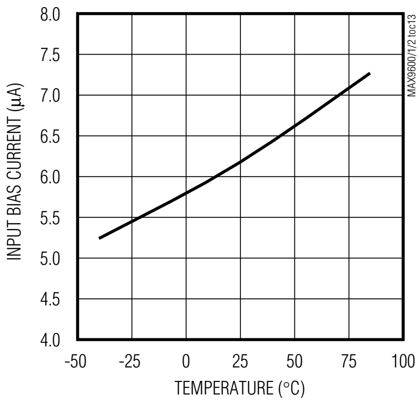
HYSTERESIS vs. TEMPERATURE



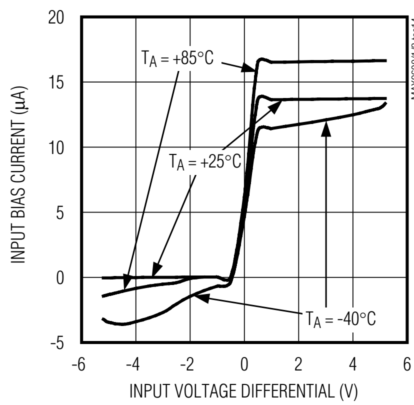
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS _ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE}$_ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), input slew rate = 2V/ns, duty cycle = 50%, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

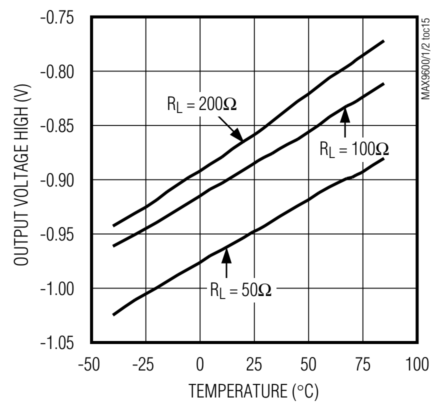
INPUT BIAS CURRENT vs. TEMPERATURE



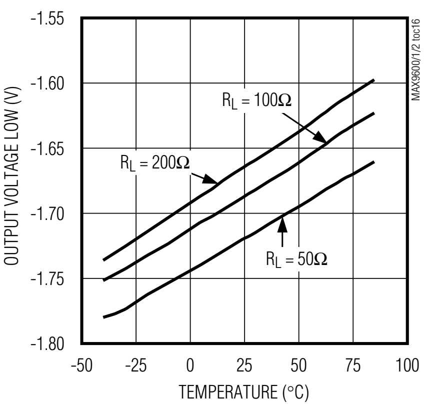
INPUT BIAS CURRENT vs. INPUT VOLTAGE DIFFERENTIAL



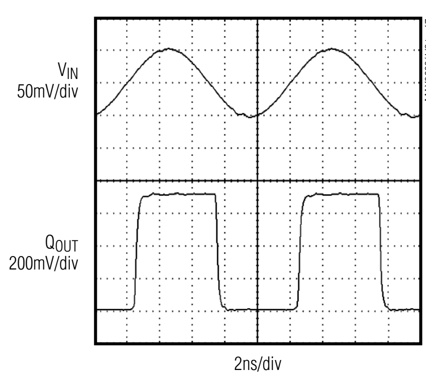
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



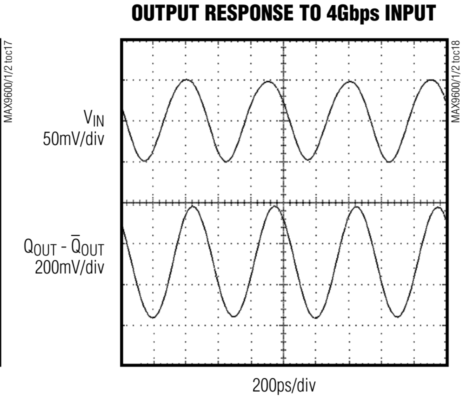
OUTPUT VOLTAGE LOW vs. TEMPERATURE



OUTPUT RESPONSE TO 100MHz INPUT



OUTPUT RESPONSE TO 4Gbps INPUT



Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

Timing Diagram

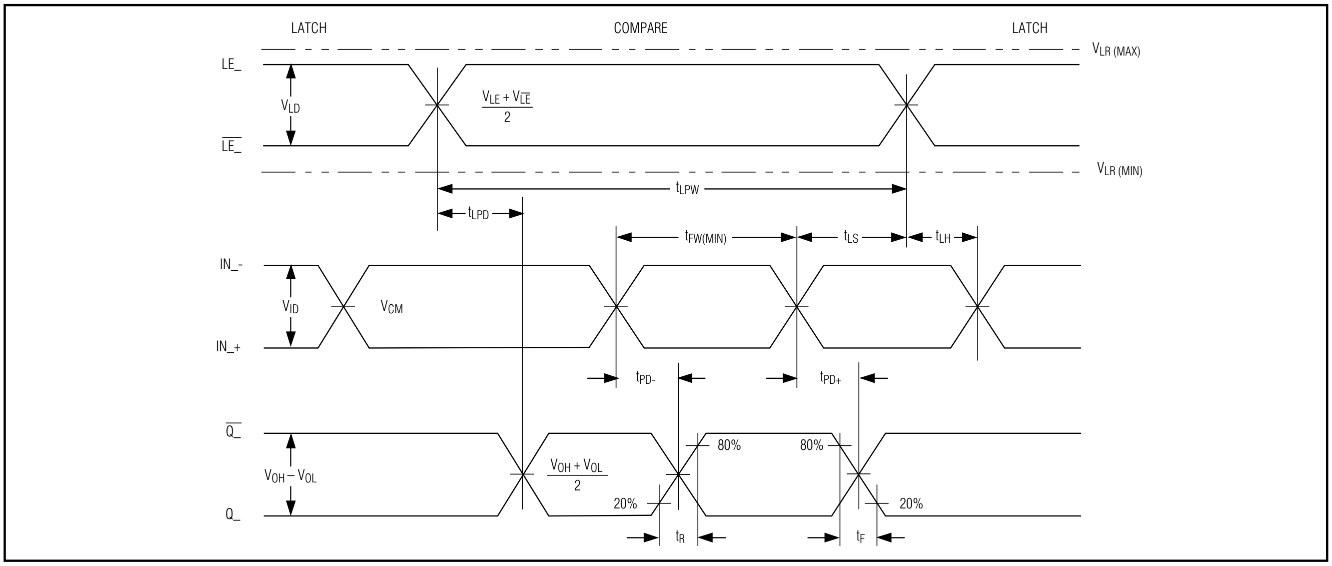


Figure 1. MAX9600/MAX9601/MAX9602 Timing Diagram

Pin Descriptions

MAX9600/MAX9601

PIN		NAME	FUNCTION
MAX9600	MAX9601		
1	1	QA	Channel A Output
2	2	$\overline{QA}$	Channel A Complementary Output
3	—	GND	Channel A Output Ground
—	3	V_{CCOA}	Channel A Output Driver Positive Supply
4	4	LEA	Channel A Latch-Enable Input
5	5	$\overline{LEA}$	Channel A Latch-Enable Complementary Input
6, 15	6, 15	V_{EE}	Negative Supply Voltage
7, 14	7, 14	V_{CC}	Positive Supply Voltage
8	8	HYSA	Channel A Hysteresis Input
9	9	INA-	Channel A Minus Input
10	10	INA+	Channel A Plus Input
11	11	INB+	Channel B Plus Input
12	12	INB-	Channel B Minus Input
13	13	HYSB	Channel B Hysteresis Input
16	16	$\overline{LEB}$	Channel B Latch-Enable Complementary Input
17	17	LEB	Channel B Latch-Enable Input
18	—	GND	Channel B Output Ground
—	18	V_{CCOB}	Channel B Output Driver Positive Supply
19	19	$\overline{QB}$	Channel B Complementary Output
20	20	QB	Channel B Output

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

Pin Descriptions (continued)

MAX9602

PIN	NAME	FUNCTION
1	INA+	Channel A Plus Input
2	INA-	Channel A Minus Input
3, 9	V_{EE}	Negative Supply Voltage
4	INB+	Channel B Plus Input
5	INB-	Channel B Minus Input
6, 12	V_{CC}	Positive Supply Voltage
7	INC+	Channel C Plus Input
8	INC-	Channel C Minus Input
10	IND+	Channel D Plus Input
11	IND-	Channel D Minus Input
13	$\overline{QD}$	Channel D Complementary Output
14	QD	Channel D Output
15	V_{CCOD}	Channel D Output Driver Positive Supply
16	$\overline{QC}$	Channel C Complementary Output
17	QC	Channel C Output
18	V_{CCOC}	Channel C Output Driver Positive Supply
19	$\overline{QB}$	Channel B Complementary Output
20	QB	Channel B Output
21	V_{CCOB}	Channel B Output Driver Positive Supply
22	$\overline{QA}$	Channel A Complementary Output
23	QA	Channel A Output
24	V_{CCOA}	Channel A Output Driver Positive Supply

Detailed Description

The MAX9600/MAX9601/MAX9602 ultra-high-speed comparators feature extremely low propagation delay (500ps). These dual and quad comparators minimize channel-to-channel skew (10ps) and are designed for low propagation delay dispersion. These features make them ideal for applications where high-fidelity tracking of narrow pulses and low timing dispersion is critical. The devices operate from either standard supply levels of -5.2V/+5V or shifted levels of -4.2V/+6V.

The differential input stage accepts a wide range of signals in the common-mode range from (V_{EE} + 3V) to (V_{CC} - 2V) with a CMRR of 70dB (typ). The outputs are complementary digital signals, compatible with ECL and PECL systems, and provide sufficient current to directly drive transmission lines terminated in 50Ω. The ultra-fast operation makes signal processing possible at a data rate up to 4Gbps. Figure 2 shows a 1Gbps (500MHz) example with an input-signal level of $100mV_{P-P}$.

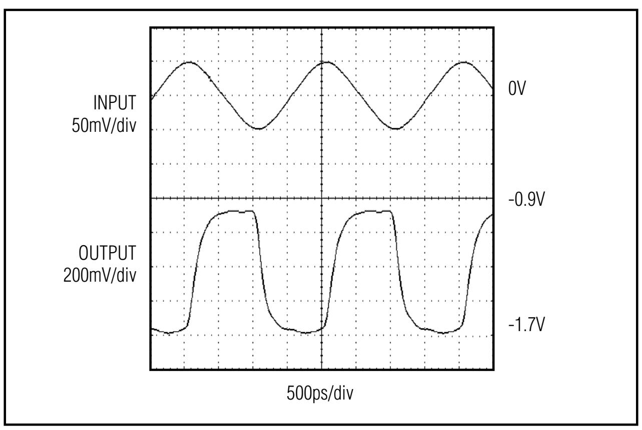


Figure 2. Signal Processed at 500MHz with Input-Signal Level of $100mV_{RMS}$.

The MAX9600/MAX9601 incorporate latch-enable and hysteresis control. Hysteresis rejects noise and prevents oscillations on low-slew input signals. The latch-enable control permits tracking or sampling mode of operations. Drive the complementary latch enable with standard ECL logic for MAX9600 and PECL logic for MAX9601. The MAX9602 quad-channel PECL output comparator does not include the latch-enable or hysteresis control functions.

Applications Information

Layout

Special layout precautions exist due to the large gain-bandwidth characteristic of the MAX9600/MAX9601/MAX9602. Use a printed circuit board with a good, low-inductance ground plane. Mount 0.01µF ceramic decoupling capacitors as close to the power-supply inputs as possible. Minimize lead lengths on the inputs and outputs to avoid unwanted parasitic feedback around the comparators. Use surface-mount chip components to minimize lead inductance. Pay close attention to the bandwidth of the decoupling and terminating components.

Use microstrip layout and terminations at the input and output. Avoid discontinuities in differential impedance. Maximize common-mode noise immunity by maintaining the distance between differential traces and avoid sharp corners. Minimize the number of vias to prevent impedance discontinuities. Match the electrical length of the traces to minimize skew.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices can create oscillation problems when the input goes through the threshold region. This is typically due to parasitic paths, which cause positive feedback to occur. For clean switching without oscillation or steps in the output waveform for the MAX9600/MAX9601, use an input with a slew rate of 5V/µs or faster. For the MAX9602, use a slew rate of 25V/µs or faster. The tendency of the part to oscillate is a function of the layout and source impedance of the circuit employed. Poor layout and larger source impedance increases the minimum slew-rate requirement. Adding hysteresis accommodates slower inputs (see the *Hysteresis* section).

Hysteresis (MAX9600/MAX9601)

Hysteresis can be introduced to prevent oscillation or multiple transitions due to noise. The MAX9600/MAX9601 feature current-controlled hysteresis, which is set by placing a resistor between HYS_ and GND. The value of the current-setting resistor is determined by the output voltage of 2.5V at HYS_ divided by the desired hysteresis current level in the range of 0 to 200µA. R_{HYS} of 10kΩ to 35kΩ resistors provides hysteresis of 60mV to 5mV (see the Hysteresis vs. R_{HYS} to GND graph in the *Typical Operating Characteristics* section). For a zero hysteresis (0µA hysteresis current), leave HYS_ open or connect it to V_{CC}.

Propagation Delay Dispersion

Propagation delay dispersion is defined as a variation in propagation delay as a function of change in input conditions. In an automatic test system pin-driver electronics, for example, the dispersion determines the maximum edge resolution.

Many factors can affect the dispersion, such as common-mode voltage, overdrive, input slew rate, duty cycle, and pulse width. The typical propagation delay dispersions of the MAX9600/MAX9601/MAX9602 are less than 10ps to 40ps (see the *Typical Operating Characteristics* and *Electrical Characteristics* sections).

Comparators with Latch Enable (MAX9600/MAX9601)

The latch-enable function allows the comparator to be used in a sampling mode. When LE_ is low ($\overline{LE\_}$ is high), the comparator tracks the input signal. When LE_ is driven high ($\overline{LE\_}$ is low), the outputs are forced to an unambiguous logic state, dependent on the input conditions at the time of the latch input transition. If the latch-enable function is not used, connect the appropriate LE_ input to a low ECL/PECL logic, and its complementary $\overline{LE\_}$ input to a high ECL/PECL logic level (see Table 1).

The input range of the MAX9600 differential latch-enable inputs is 400mV to 2V. The logic-input swing excursion must fall within an input-voltage range (V_{LR}) of -2V to 0 to work properly. The input range of the MAX9601 differential latch-enable inputs is 250mV to 3.5V. The logic-input swing excursion must fall within an input-voltage range (V_{LR}) of 0 to 3.5V for ($V_{CCO\_}$ < 3.5V) or V_{LR} of ($V_{CCO\_}$ - 3.5V) to $V_{CCO\_}$ for ($V_{CCO\_} \geq$ 3.5V) to work properly.

Table 1. Latch-Enable Truth Table

LATCH-ENABLE INPUT		OPERATION
LE_	$\overline{LE\_}$	
0	1	Compare Mode. Output follows input state.
1	0	Latch Mode. Output latches to last known output state.
0	0	Invalid condition, output is in unknown state.
1	1	

Timing Information (MAX9600/MAX9601)

The timing diagram (Figure 1) illustrates the operation of a comparator with latch enable. The top line of the diagram illustrates a latch-enable pulse. Initially, the latch-enable input (LE, $\overline{LE\_}$) is differentially high, which places the comparator in latch mode. When the input signal (IN_+, IN_-) switches from low to high, the output (Q_, $\overline{Q\_}$) remains latched to the previous low state. When the latch-enable input goes differentially low, starting the compare function, the output responds to the input and transitions to high after a time (t_{LPD}). The leading edges of the subsequent input signal switch the comparator after time interval t_{PD+} or t_{PD-} (depending on the direction of the input transitions) until a high latch-enable pulse places the device in latch mode again. The input signal must occur at minimum time (t_{LS}) before the latch rising edge, and must maintain its state for at least t_{LH} after the rising edge. A minimum latch-pulse width (t_{LPW}) of 250ps (typ) is needed for proper latch operation.

ECL/PCL

The MAX9600/MAX9601/MAX9602 outputs are emitter followers that require external resistive connections to a voltage source (V_T) more negative than the lowest V_{OL} for proper static and dynamic operation. When properly terminated, the outputs provide appropriate levels, V_{OL} or V_{OH}, for ECL (MAX9600) or PECL (MAX9601/MAX9602). Output-current polarity always sinks into the termination scheme during proper operation.

ECL-output signal levels are referenced to GND, and PECL-output signals are referenced to $V_{CCO\_}$.

Chip Information

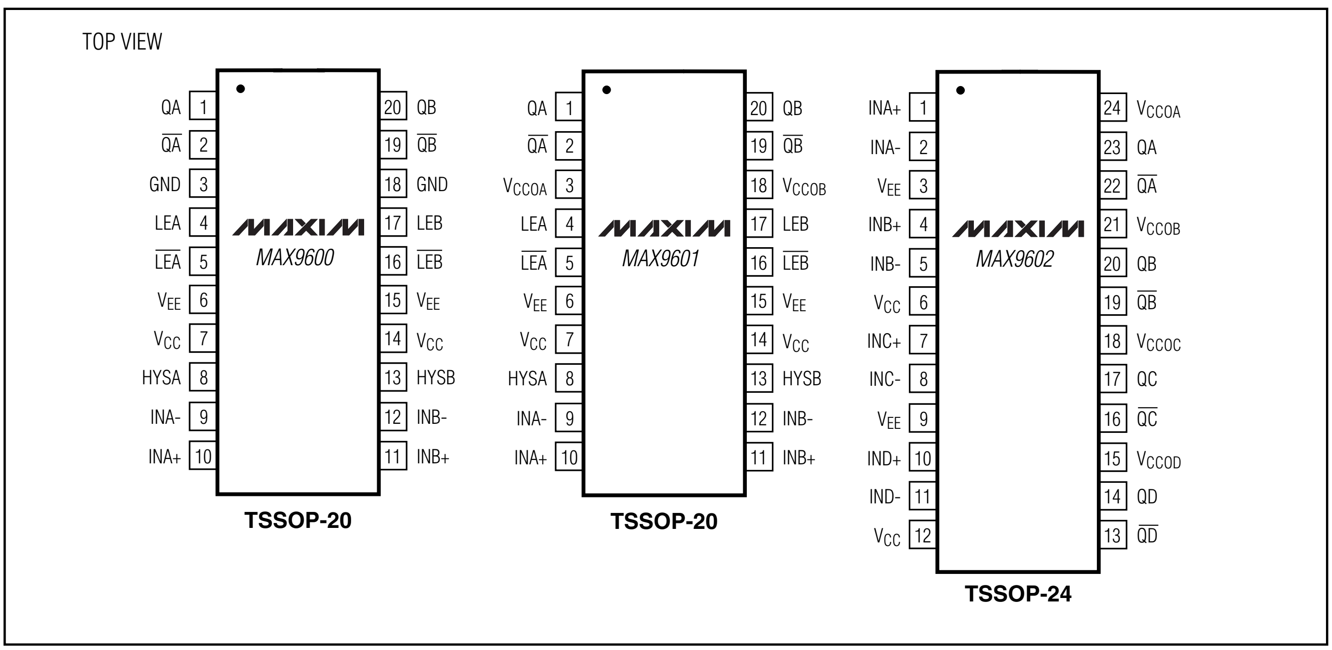
MAX9600 TRANSISTOR COUNT: 558

MAX9601 TRANSISTOR COUNT: 600

MAX9602 TRANSISTOR COUNT: 608

PROCESS: Bipolar

Pin Configurations

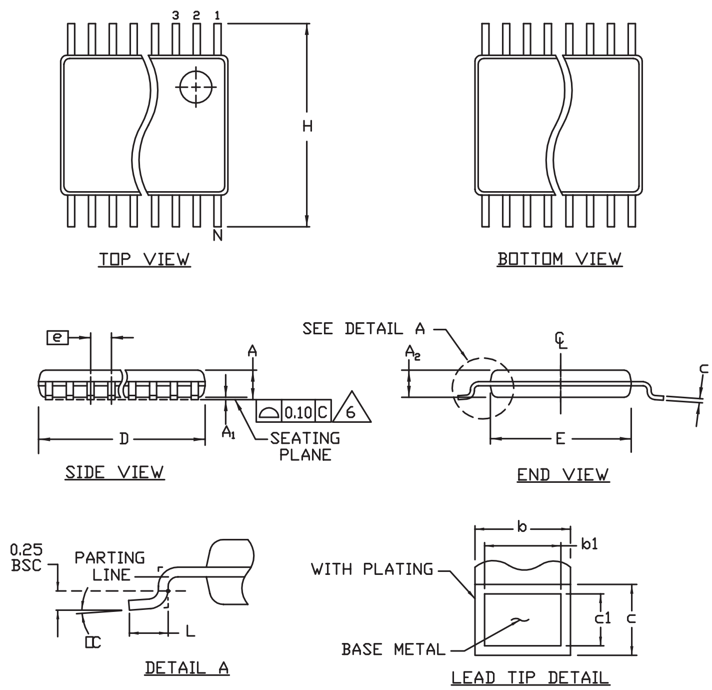


Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1