

MC10EP90, MC100EP90

-3.3V / -5V Triple ECL Input to LVPECL/PECL Output Translator

Description

The MC10/100EP90 is a TRIPLE ECL TO LVPECL/PECL translator. The device receives differential LVECL or ECL signals and translates them to differential LVPECL or PECL output signals.

A V_{BB} output is provided for interfacing with Single-Ended LVECL or ECL signals at the input. If a Single-Ended input is to be used the V_{BB} output should be connected to the \bar{D} input. The active signal would then drive the D input. When used the V_{BB} output should be bypassed to ground by a 0.01 μF capacitor. The V_{BB} output is designed to act as the switching reference for the EP90 under Single-Ended input switching conditions, as a result this pin can only source/sink up to 0.5 mA of current.

To accomplish the level translation the EP90 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} connected to the negative supply.

The 100 Series contains temperature compensation.

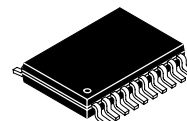
Features

- 260 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- Voltage Supplies $V_{CC} = 3.0\text{ V}$ to 5.5 V , $V_{EE} = -3.0\text{ V}$ to -5.5 V , $GND = 0\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- Fully Differential Design
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Output
- These are Pb-Free Devices*



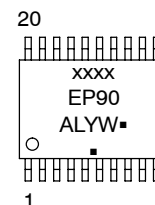
ON Semiconductor®

<http://onsemi.com>



TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAM*



xxxx = MC10 or 100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

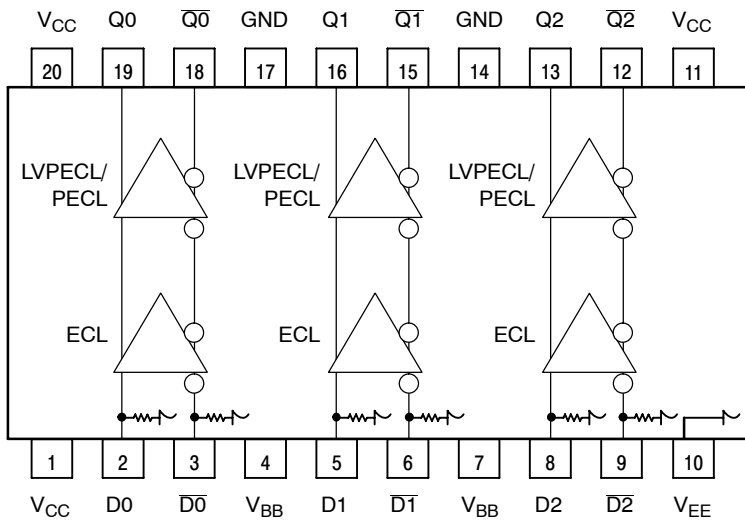
*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Warning: All V_{CC} , V_{EE} and GND pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. TSSOP-20 (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q(0:2), \bar{Q} (0:2)	Differential LVPECL or PECL Outputs
D(0:2)*, \bar{D} (0:2)*	Differential LVECL or ECL Inputs
V_{CC}	Positive Supply
GND	Ground
V_{EE}	Negative Supply
V_{BB}	Output Reference Supply

* Pins will default LOW when left open.

Table 2. FUNCTION TABLE

Function	V_{CC}	GND	V_{EE}
-5V ECL to 5V PECL	5 V	0 V	-5 V
-5V ECL to 3.3V PECL	3.3 V	0 V	-5 V
-3.3V ECL to 5V PECL	5 V	0 V	-3.3 V
-3.3V ECL to 3.3V PECL	3.3 V	0 V	-3.3 V

Table 3. ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	75 k Ω	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	TSSOP-20	Level 1
		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	350 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	GND = 0 V		6	V
V _{EE}	NECL Mode Power Supply	GND = 0 V		-6	V
V _I	PECL Mode Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	GND = 0 V	$V_I \geq V_{EE}$	-6	V
I _{out}	Output Current	Continuous Surge		50	mA
				100	mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	TSSOP-20	140	°C/W
		500 lfpm	TSSOP-20	100	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-20	23 to 41	°C/W
T _{sol}	Wave Solder	Pb	<2 to 3 sec @ 248°C	265	°C
		Pb-Free	<2 to 3 sec @ 260°C	265	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 5. 10EP DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $V_{EE} = -5.5\text{ V to }-3.0\text{ V}$; $GND = 0\text{ V}$ (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	5	13	20	5	13	20	5	13	20	mA
I_{CC}	Positive Power Supply Current	43	55	67	43	55	67	43	55	67	mA
V_{OH}	Output HIGH Voltage (Note 3)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 3)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC} .

3. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

4. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. 10EP DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.5\text{ V to }-3.0\text{ V}$; $GND = 0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	5	13	20	5	13	20	5	13	20	mA
I_{CC}	Positive Power Supply Current	43	55	67	43	55	67	43	55	67	mA
V_{OH}	Output HIGH Voltage (Note 6)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 6)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} .

6. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

7. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 7. 100EP DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $V_{EE} = -5.5\text{ V to } -3.0\text{ V}$; $GND = 0\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	5	13	20	5	13	20	5	13	20	mA
I_{CC}	Positive Power Supply Current	45	58	70	50	62	75	53	65	78	mA
V_{OH}	Output HIGH Voltage (Note 9)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 9)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-885	-1225		-885	-1225		-885	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with V_{CC} .

9. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

10. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. 100EP DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.5\text{ V to } -3.0\text{ V}$; $GND = 0\text{ V}$ (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	5	13	20	5	13	20	5	13	20	mA
I_{CC}	Positive Power Supply Current	45	58	70	50	62	75	53	65	78	mA
V_{OH}	Output HIGH Voltage (Note 12)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 12)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-885	-1225		-885	-1225		-885	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with V_{CC} .

12. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

13. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 9. AC CHARACTERISTICS $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$; $V_{CC} = 3.0\text{ V to }5.5\text{ V}$; $GND = 0\text{ V}$ (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2 $F_{max}/JITTER$)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	170	240	310	200	260	340	230	300	370	ps
t_{SKEW}	Duty Cycle Skew (Note 15)		5.0	20		5.0	20		5.0	20	ps
	Within Device Skew Q, \bar{Q} Device to Device Skew (Note 15)			80 140			80 140			80 140	
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2 $F_{max}/JITTER$)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times Q, \bar{Q} (20% - 80%)	70	120	170	80	130	180	100	150	230	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$.

15. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

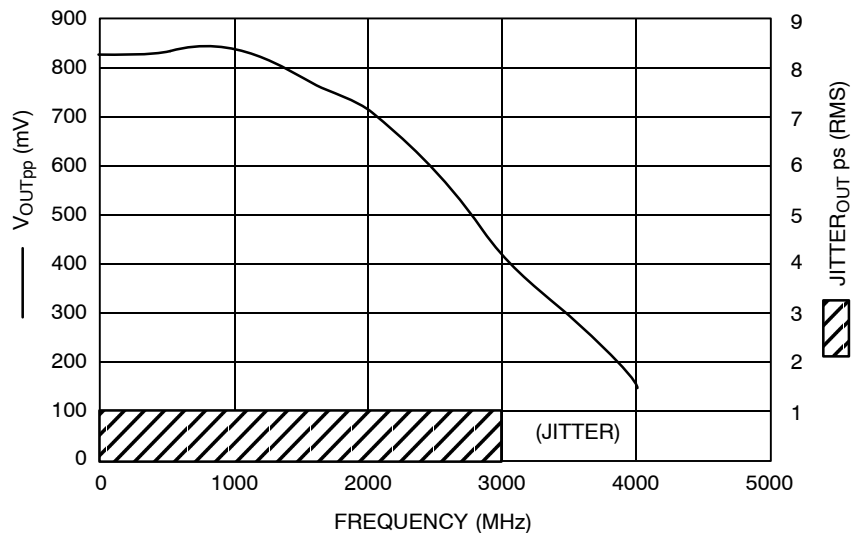


Figure 2. $F_{max}/Jitter$

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**Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10EP90DT	TSSOP-20*	75 Units / Rail
MC10EP90DTG	TSSOP-20*	75 Units / Rail
MC10EP90DTR2	TSSOP-20*	2500 / Tape & Rail
MC10EP90DTR2G	TSSOP-20*	2500 / Tape & Rail
MC100EP90DT	TSSOP-20*	75 Units / Rail
MC100EP90DTG	TSSOP-20*	75 Units / Rail
MC100EP90DTR2	TSSOP-20*	2500 / Tape & Rail
MC100EP90DTR2G	TSSOP-20*	2500 / Tape & Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

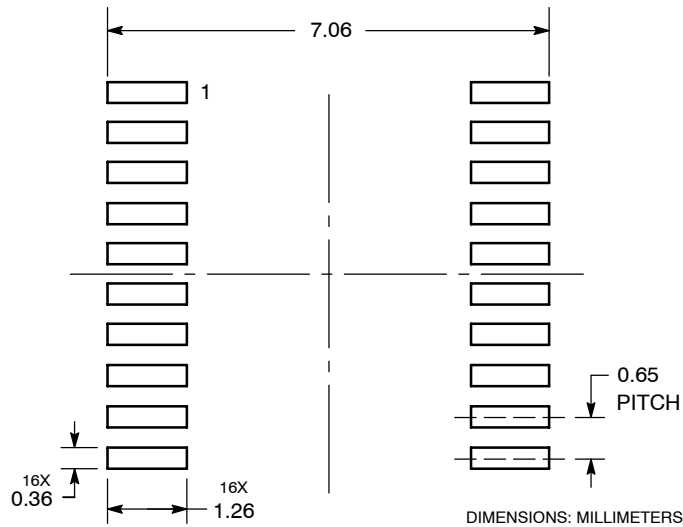


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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