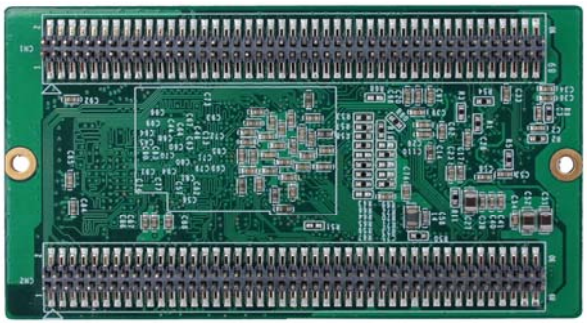
Embest Mini8510 Processor Card

Top-View



Bottom-View

Features

Mechanical Parameters

- Dimensions: 67 x 37 mm
- Working temperature: 0~70 Celsius
- Humidity Range: 20% ~ 90%
- Power Consumption: 1A @ 3.3V

Processor

- TI DM3730 DaVinci Digital Media Processor (pin-to-pin compatible with TI AM3715)

- Up to 1-GHz ARM® Cortex™-A8 Core, also supports 300, 600, and 800-MHz operation
- Up to 800-MHz TMS320C64x+™ DSP Core, also supports 260, 520 and 660-MHz operation (DM3730 only)
- NEON™ SIMD Coprocessor
- POWERVR SGX™ Graphics Accelerator
- ARM: 32KB I-Cache; 32KB D-Cache; 256KB L2 Cache
- Onchip 32KB ROM and 64KB Shared SDRAM

Memory

- 256MB DDR SDRAM, 32-bit
- 256MB NAND Flash, 16-bit

Onboard Headers and Signals Routed to Pins

- 12-bit Camera interface (30-pin FPC connector, support CCD or CMOS camera)
- 1-channal 4-wire JTAG interface (10-pin 1.0mm pitch connector)
- 6 LEDs (programmable status LEDs)
- 2-channel SPI
- GPMC bus (16-bit data bus, 10-bit address bus, 4 chip-selection signals and several control signals)
- 3-channel 5-wire UARTs
- 1-channel ULPI (USB1 HS)
- Audio in/out

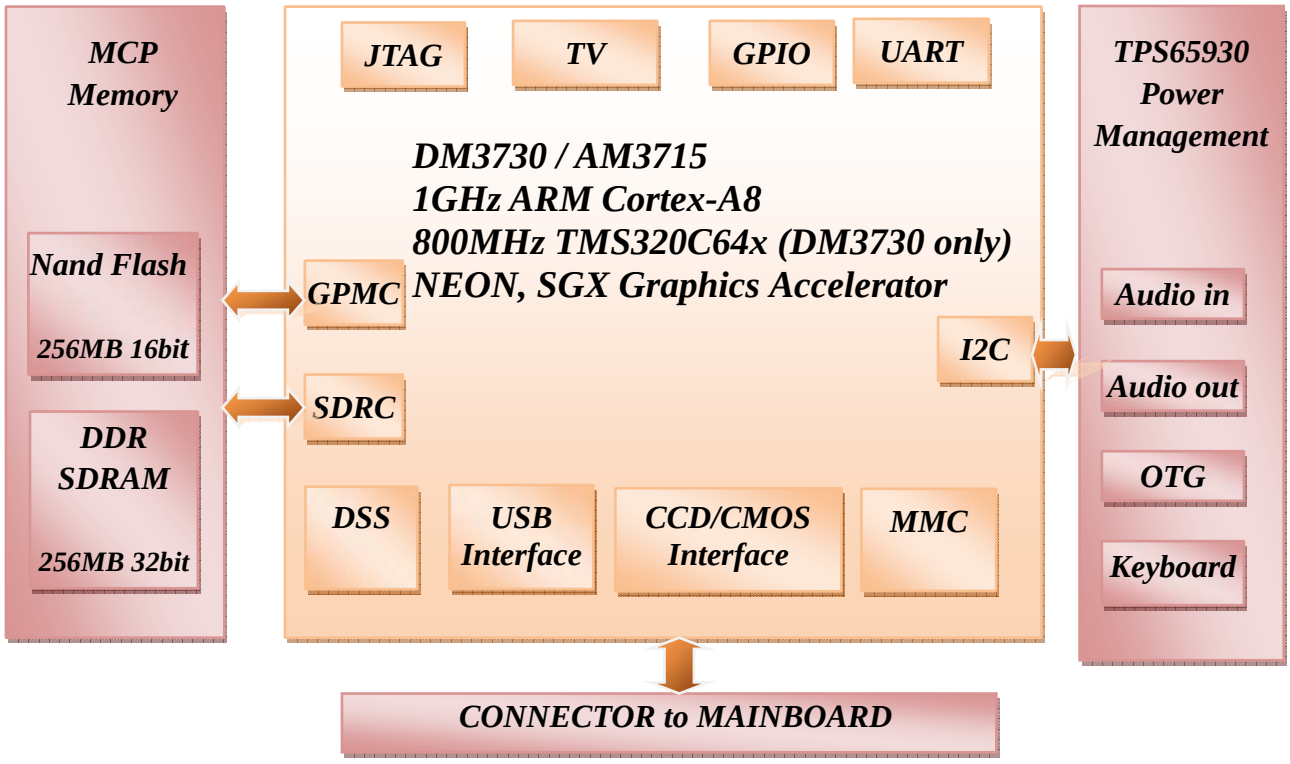
- 1-channel I2C
- 2-channel McBSP (McBSP1 and McBSP3, McBSP3 is multiplex with UART2)
- 2-channel SD/MMC: MMC1 (8-wire), MMC2 (4-wire)
- 24-bit DSS interface

General Description

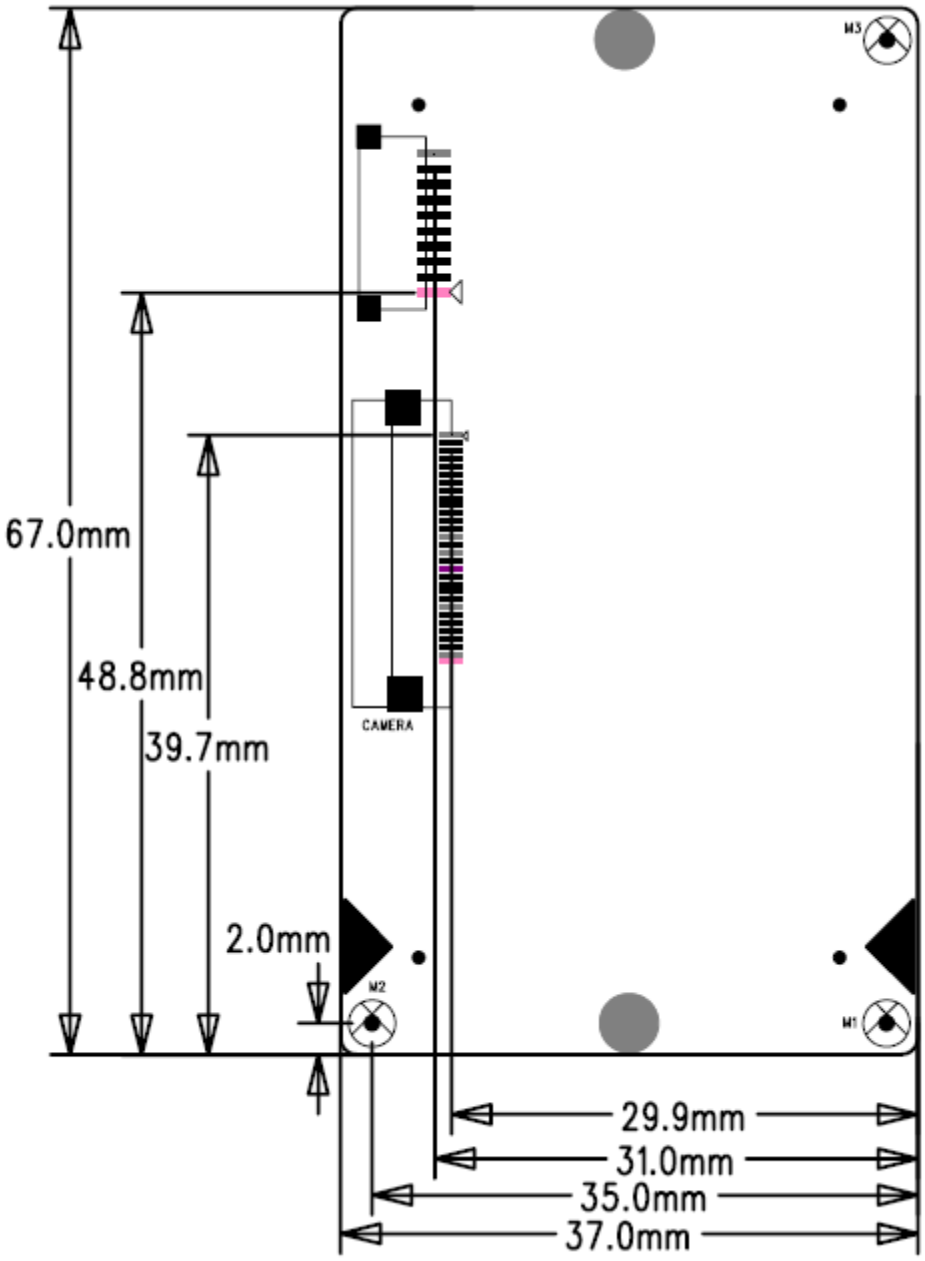
Embest Mini8510 processor card is based on TI's DM3730 DaVinci Digital Media processor which is powered by 1GHz ARM Cortex-A8 and 800MHz C64x+ DSP core. The Mini8510 hardware is compatible with Embest Mini8100 OMAP3530 processor card which is convenient for customers who used Mini8100 before to upgrade to Mini8510 so as to migrate from the OMAP3530 to DM3730 for their embedded designs.

The SBC8100 expansion board for integration of the Embest Mini8100 processor card can be also used for Mini8510. The processor card is connected with SBC8100 expansion board through two 1.27mm space 2*45-pin dip connectors. We call the upgraded DM3730 system SBC8100 Plus. Embest offers Linux 2.6.32 and WinCE6.0 BSP for this board. Customers can leverage our experience to increase your own productivity. The optimal embedded microprocessor solution provides users with a flexible development environment based on DM3730 and a shortened development timeframe.

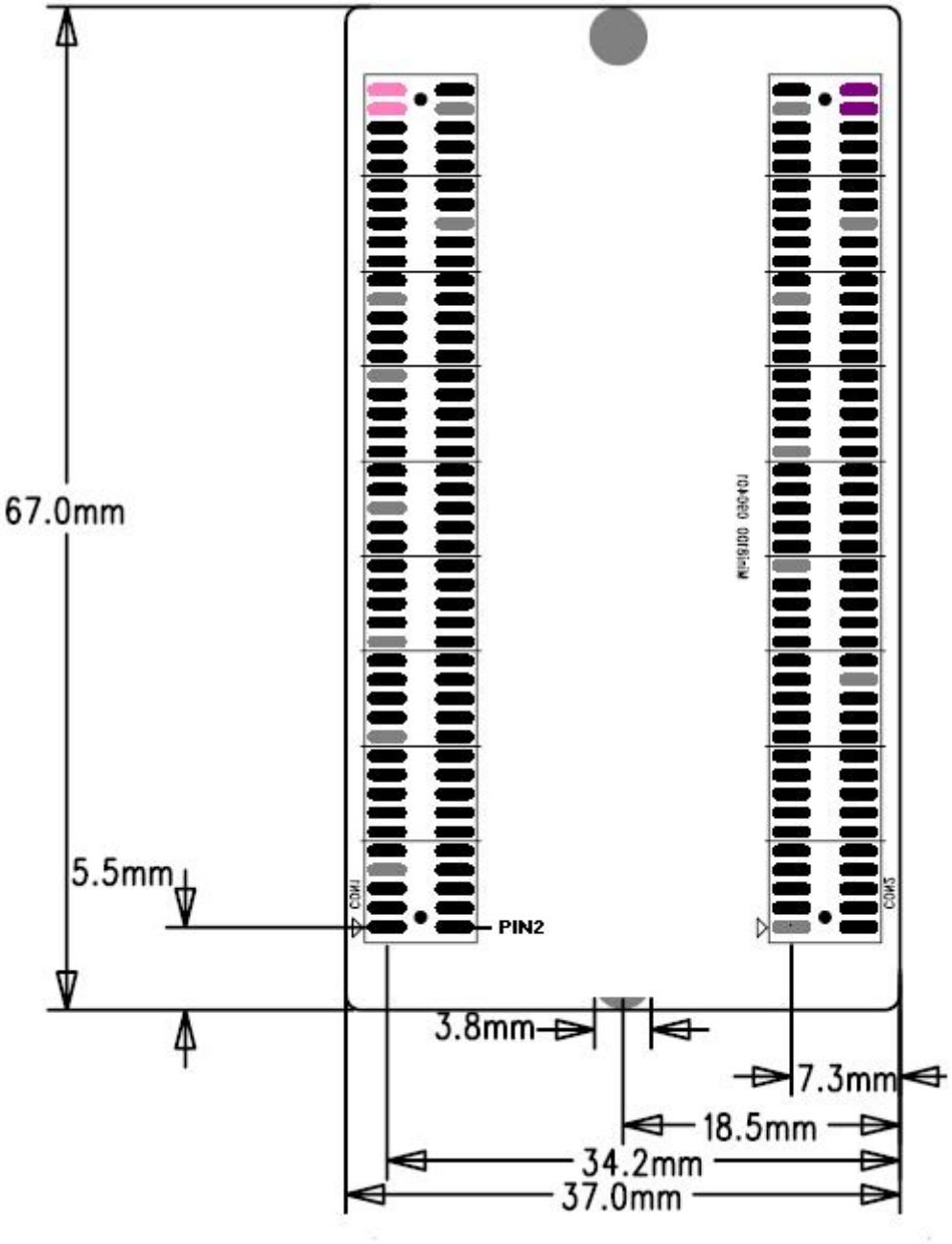
Layout and Functional Block Diagram



Dimensions



Mini8510 Top View



Mini8510 Top-View Perspective Drawing

Camera interface

Embest Mini8510 processor card uses a 30-pin FPC connector, supporting CCD or CMOS camera. Detailed pin explanation is as following:

Pin	Signal	Description
1	GND	GND
2	D0	Digital image data bit 0
3	D1	Digital image data bit 1
4	D2	Digital image data bit 2
5	D3	Digital image data bit 3
6	D4	Digital image data bit 4
7	D5	Digital image data bit 5
8	D6	Digital image data bit 6
9	D7	Digital image data bit 7
10	D8	Digital image data bit 8
11	D9	Digital image data bit 9
12	D10	Digital image data bit 10
13	D11	Digital image data bit 11
14	GND	GND
15	PCLK	Pixel clock
16	GND	GND
17	HS	Horizontal synchronization
18	VDD50	5V
19	VS	Vertical synchronization
20	VDD33	3.3V
21	XCLKA	Clock output a
22	XCLKB	Clock output b
23	GND	GND
24	FLD	Field identification
25	WEN	Write Enable
26	STROBE	Flash strobe control signal
27	SDA	IIC master serial clock
28	SCL	IIC serial bidirectional data
29	GND	GND
30	VDD18	1.8V

JTAG interface

Embest Mini8510 processor card has a 10-pin 1.0mm pitch JTAG connector on board. Detailed pin explanation is as following:

Pin	Signal	Description
1	VDD18	1.8V output
2	TMS	Test mode select
3	TD1	Test data input
4	NTRST	Test system reset
5	TD0	Test data output
6	RTCK	Receive test clock
7	TCK	Test clock
8	EMU0	Test emulation 0
9	EMU1	Test Emulation 1
10	GND	GND

Two 2*45-pin Expansion Connectors

Embest Mini8510 processor card is connected to carrierboard via two 1.27mm space 2*45-pin dip connectors.
Detailed pin explanation for **CON1** is as following:

Pin	Signal	Description
1	G_NWE	GPMC Write Enable
2	G_NOE	GPMC Read Enable
3	G_NCS7GPT8G_DIR	GPMC Chip Select bit 7PWM or event for GP timer 8GPMC IO direction control for use with external transceivers
4	G_NCS4GPT9DMAREQ1	GPMC Chip Select bit 7PWM or event for GP timer 9External DMA request 1
5	G_NCS6GPT11DMAREQ3	GPMC Chip Select bit 7PWM or event for GP timer 11 External DMA request 3
6	G_NCS3DMAREQ0	GPMC Chip Select bit 7External DMA request 0
7	GND	GND
8	G_WAIT0	External indication of wait
9	G_NBE0 / G_CLE	Lower Byte Enable. Also used for Command Latch Enable
10	G_NATV_ALE	Address Valid or Address Latch Enable
11	G_NBE1	Upper Byte Enable
12	HDQ_SIO	Bidirectional HDQ 1-Wire control and data
13	MMC1_D0	MMC/SD Card Data bit 0
14	MMC1_D1	MMC/SD Card Data bit 1
15	MMC1_D2	MMC/SD Card Data bit 2
16	MMC1_D6/IO128	MMC/SD Card Data bit 6
17	MMC1_D5/IO127	MMC/SD Card Data bit 5
18	MMC1_D4/IO126	MMC/SD Card Data bit 4
19	MMC1_D7/IO129	MMC/SD Card Data bit 7

20	MMC1_D3	MMC/SD Card Data bit 3
21	GND	GND
22	MMC1_CLK	MMC/SD Output Clock
23	MMC1_CMD	MMC/SD command signal
24	VMMC1	Power supply for SD/MMC1 (3.0 / 1.8V)
25	UART3_RX_IRRX	UART3 Receive data, IR and Remote RX
26	UART3_CTS_RCTX	UART3 Clear To Send, Remote TX
27	UART3_TX_IRTX	UART3 Transmit data, IR TX
28	UART3_RTS_SD	UART3 Request To Send, IR enable
29	DSS_ACBIAS	AC bias control (STN) or pixel data enable (TFT) output
30	DSS_VSYNC	LCD Vertical Synchronization
31	GND	GND
32	DSS_HSYNC	LCD Horizontal Synchronization
33	DSS_CLK	LCD Pixel Clock
34	DSS_D6	LCD Pixel Data bit 6
35	DSS_D8	LCD Pixel Data bit 8
36	DSS_D7	LCD Pixel Data bit 7
37	DSS_D9	LCD Pixel Data bit 9
38	DSS_D20	LCD Pixel Data bit 20
39	DSS_D17	LCD Pixel Data bit 17
40	DSS_D16	LCD Pixel Data bit 16
41	DSS_D18	LCD Pixel Data bit 18
42	DSS_D10	LCD Pixel Data bit 10
43	DSS_D5	LCD Pixel Data bit 5
44	DSS_D4	LCD Pixel Data bit 4
45	GND	GND
46	DSS_D2	LCD Pixel Data bit 2
47	DSS_D3	LCD Pixel Data bit 3
48	DSS_D0	LCD Pixel Data bit 0
49	DSS_D15	LCD Pixel Data bit 15
50	DSS_D11	LCD Pixel Data bit 11
51	DSS_D23	LCD Pixel Data bit 23
52	DSS_D22	LCD Pixel Data bit 22
53	DSS_D14	LCD Pixel Data bit 14
54	DSS_D19	LCD Pixel Data bit 19
55	DSS_D13	LCD Pixel Data bit 13
56	DSS_D21	LCD Pixel Data bit 21
57	DSS_D1	LCD Pixel Data bit 1
58	DSS_D12	LCD Pixel Data bit 12
59	GND	GND
60	MCBSP1_FSR/IO157	Receive frame synchronization
61	MCBSP1_CLKR/IO156	Receive Clock
62	MCBSP1_FSX/IO161	Transmit frame synchronization
63	MCBSP1_CLKS/IO160	External clock input
64	MCBSP1_CLKX/IO162	Transmit clock
65	MCBSP1_DR/IO159	Received serial data
66	MCBSP1_DX/IO158	Transmitted serial data
67	GND	GND

68	TV_OUTC	TV analog output S-VIDEO: TV_OUT2
69	TV_OUTY	TV analog output Composite: TV_OUT1
70	VDD33	Power supply for camera (3.3V 500mA)
71	IIC3_SCL	I2C Master Serial clock. Output is open drain
72	IIC3_SDA	I2C Serial Bidirectional Data. Output is open drain
73	IO25	General-purpose IO 183
74	IO27	General-purpose IO 183
75	BOOTJUMP	Boot configuration mode bit 5.
76	GND	GND
77	VBUS	VBUS power rail (5V 10mA)
78	USB_DN	USB Data N
79	USB_ID	USB ID
80	USB_DP	USB Data P
81	PWM0	Pulse width driver 0
82	KR0	Keypad row 0
83	KR1	Keypad row 1
84	KR2	Keypad row 2
85	KR3	Keypad row 3
86	KR4	Keypad row 4
87	VDD18	Power supply from TPS65930 (VIO 1.8V)
88	GND	GND
89	VDD18	Power supply from TPS65930 (VIO 1.8V)
90	BKBAT	Backup battery

Detailed pin explanation for **CON2** is as following:

Pin	**Signal**	**Description**
1	GND	GND
2	G_D14	GPMC data bit 14
3	G_D13	GPMC data bit 13
4	G_D10	GPMC data bit 10
5	G_D8	GPMC data bit 8
6	G_D9	GPMC data bit 9
7	G_D5	GPMC data bit 5
8	G_D7	GPMC data bit 7
9	G_D3	GPMC data bit 3
10	G_D6	GPMC data bit 6
11	G_D12	GPMC data bit 12
12	G_D2	GPMC data bit 2
13	G_D11	GPMC data bit 11
14	G_D1	GPMC data bit 1
15	G_D4	GPMC data bit 4
16	G_D0	GPMC data bit 0
17	G_A2	GPMC address bit 2
18	G_A3	GPMC address bit 3
19	G_A1	GPMC address bit 1
20	G_A6	GPMC address bit 6
21	G_A4	GPMC address bit 4

22	G_A7	GPMC address bit 7
23	G_A5	GPMC address bit 5
24	G_A8	GPMC address bit 8
25	G_A9	GPMC address bit 9
26	G_D15	GPMC data bit 15
27	G_A10	GPMC address bit 10
28	GND	GND
29	SPI2_CS1 GPT8	SPI Enable 1PWM or event for GP timer 8
30	SPI2_CS10 GPT11	SPI Enable 0PWM or event for GP timer 11
31	SPI2_SIMO GPT9	Slave data in, master data out PWM or event for GP timer 9
32	SPI2_CLK	SPI Clock
33	SPI2_SOMI GPT10	Slave data out, master data inPWM or event for GP timer 10
34	SPI1_CS3	SPI Enable 3
35	SPI1_CS0	SPI Enable 0
36	SPI1_SIMO	Slave data in, master data out
37	SPI1_SOMI	Slave data out, master data in
38	SPI1_CLK	SPI Clock
39	GND	GND
40	GPIO0	GPIO0 /card detection 1
41	MMC2_D2 SPI3_CS1	MMC/SD Card Data bit 2SPI Enable 1
42	MMC2_D3SPI3_CS0	MMC/SD Card Data bit 3SPI Enable 0
43	MMC2_D0SPI3_SOMI	MMC/SD Card Data bit 0Slave data out, master data in
44	MMC2_D1	MMC/SD Card Data bit 1
45	MMC2_CMDSPI3_SIMO	MMC/SD command signalSlave data in, master data out
46	MMC2_CLKSPI3_CLK	MMC/SD Output ClockSPI Clock
47	BSP3_DRUART2_RTS	Received serial dataUART2 Request To Send
48	BSP3_CLKUART2_TX	Combined serial clockUART2 Transmit data
49	BSP3_FSXUART2_RX	Combined frame synchronizationUART2 Receive data
50	BSP3_DXUART2_CTS	Transmitted serial dataUART2 Clear To Send
51	GND	GND
52	UART1_CTS	UART1 Clear To Send
53	UART1_TX	UART1 Transmit data
54	UART1_RX	UART1 Receive data
55	UART1_RTS	UART1 Request To Send
56	USB1HS_STP	Dedicated for external transceiver Stop signal
57	USB1HS_D3	Dedicated for external transceiver Bidirectional data bus
58	USB1HS_D5	Dedicated for external transceiver Bidirectional data bus
59	USB1HS_6	Dedicated for external transceiver Bidirectional data bus
60	USB1HS_D7	Dedicated for external transceiver Bidirectional data bus
61	USB1HS_D1	Dedicated for external transceiver Bidirectional data bus
62	USB1HS_D2	Dedicated for external transceiver Bidirectional data bus
63	USB1HS_D4	Dedicated for external transceiver Bidirectional data bus
64	USB1HS_D0	Dedicated for external transceiver Bidirectional data bus
65	USB1HS_NXT	Dedicated for external transceiver Next signal from PHY
66	USB1HS_CLK	Dedicated for external transceiver 60-MHz clock
67	GND	GND
68	USB1HS_DIR	Dedicated for external transceiver data form PHY
69	SYS_CLKOUT1	Configurable output clock1

70	LEDA	LED leg A
71	LEDB	LED leg B
72	ADCIN0	ADC input0 (Battery type)
73	NRESPWRON	Power On Reset
74	NRESWARM	Warm Boot Reset (open drain output)
75	SYSEN	System enable output
76	GND	GND
77	REGEN	Enable signal for external LDO
78	ADCIN1	ADC input1 (General-purpose ADC input)
79	KC0	Keypad column 0
80	KC1	Keypad column 0
81	KC2	Keypad column 0
82	KC3	Keypad column 0
83	AUDIO_IN	Analog microphone bias 1
84	AUDIO_OR	Predriver output right P for external class-D amplifier
85	AUXR	Auxiliary audio input right
86	AUDIO_OL	Predriver output left P for external class-D amplifier
87	GND	GND
88	VBAT	Power supply (3V - 4.2V 1.5A)
89	ON/OFF	Input; detect a control command to start or stop the systerm
90	VBAT	Power supply (3V - 4.2V 1.5A)

Order Information

Order No.	T400304
Item	Embest Mini8510 Processor Card
Options	Embest SBC8100 Plus Single Board Computer
Price	Please contact Embest

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