# MIXED SIGNAL MICROCONTROLLER

## FEATURES

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption**
  - **Active Mode: 220 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Five Power-Saving Modes**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs**
- **16-Bit RISC Architecture, up to 12-MHz System Clock**
- **Basic Clock Module Configurations**
  - **Internal Frequencies up to 12 MHz With Two Calibrated Frequencies**
  - **Internal Very-Low-Power Low-Frequency (LF) Oscillator**
  - **High-Frequency (HF) Crystal up to 16 MHz**
  - **Resonator**
  - **External Digital Clock Source**
- **Up to Three 24-Bit Sigma-Delta Analog-to-Digital (A/D) Converters With Differential PGA Inputs**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Serial Communication Interface (USART), Asynchronous UART or Synchronous SPI Selectable by Software**
- **16-Bit Hardware Multiplier**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor with Programmable Level Detection**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Module**
- **Family Members are Summarized in Table 1.**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*, Literature Number SLAU144**

## DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430AFE2x3 devices are ultra-low-power mixed signal microcontrollers integrating three independent 24-bit sigma-delta A/D converters, one 16-bit timer, one 16-bit hardware multiplier, USART communication interface, watchdog timer, and 11 I/O pins.

The MSP430AFE2x2 devices are identical to the MSP430AFE2x3, except that there are only two 24-bit sigma-delta A/D converters integrated.

The MSP430AFE2x1 devices are identical to the MSP430AFE2x3, except that there is only one 24-bit sigma-delta A/D converter integrated.

Available family members are summarized in Table 1.

**Table 1. Family Members(1)**

| Device | Flash (KB) | SRAM (Byte) | EEM | SD24_A Converters | 16-Bit MPY | Timer_A(2) | USART (UART/ SPI) | Clocks | I/O | Package Type(3) |
|---|---|---|---|---|---|---|---|---|---|---|
| MSP430AFE253IPW | 16 | 512 | 1 | 3 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE233IPW | 8 | 512 | 1 | 3 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE223IPW | 4 | 256 | 1 | 3 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE252IPW | 16 | 512 | 1 | 2 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE232IPW | 8 | 512 | 1 | 2 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE222IPW | 4 | 256 | 1 | 2 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE251IPW | 16 | 512 | 1 | 1 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE231IPW | 8 | 512 | 1 | 1 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |
| MSP430AFE221IPW | 4 | 256 | 1 | 1 | 1 | 3 | 1 | HF, DCO, VLO | 11 | 24-TSSOP |

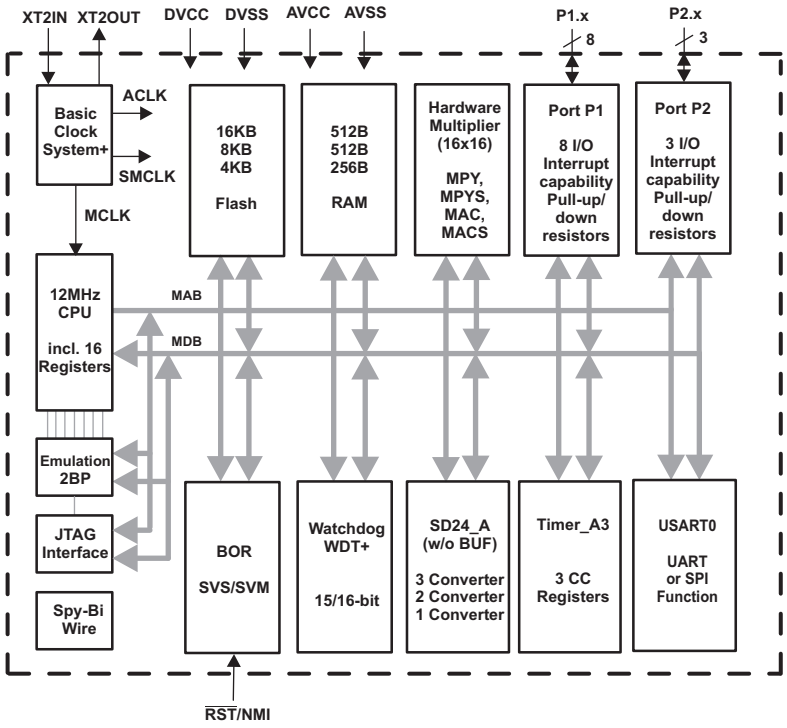
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## Development Tool Support

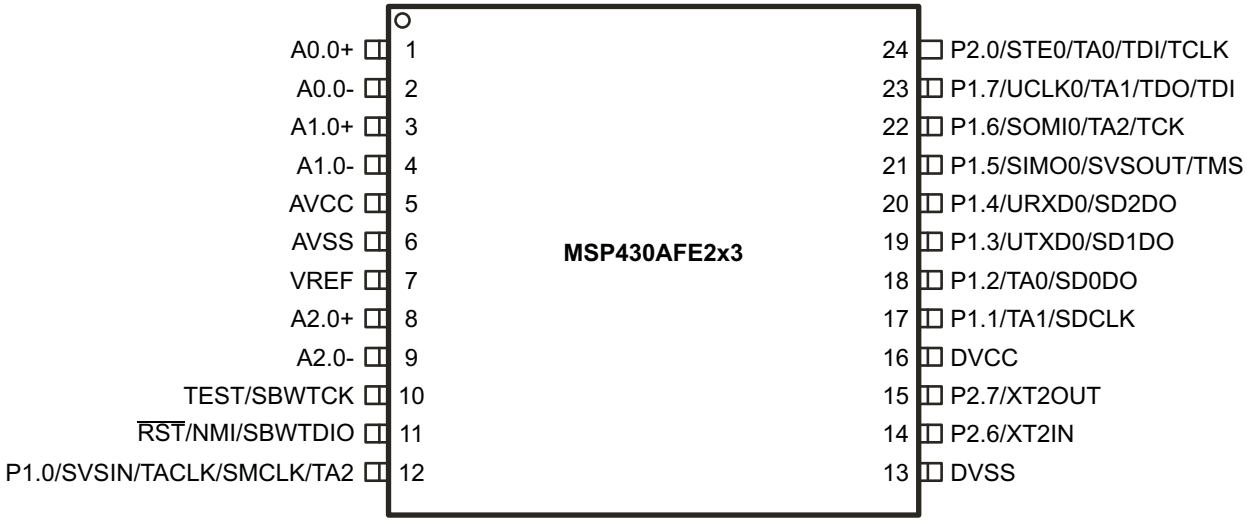
All MSP430™ microcontrollers include an Embedded Emulation Module (EEM) that allows advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-TS430PW24
- Production Programmer
  - MSP-GANG430

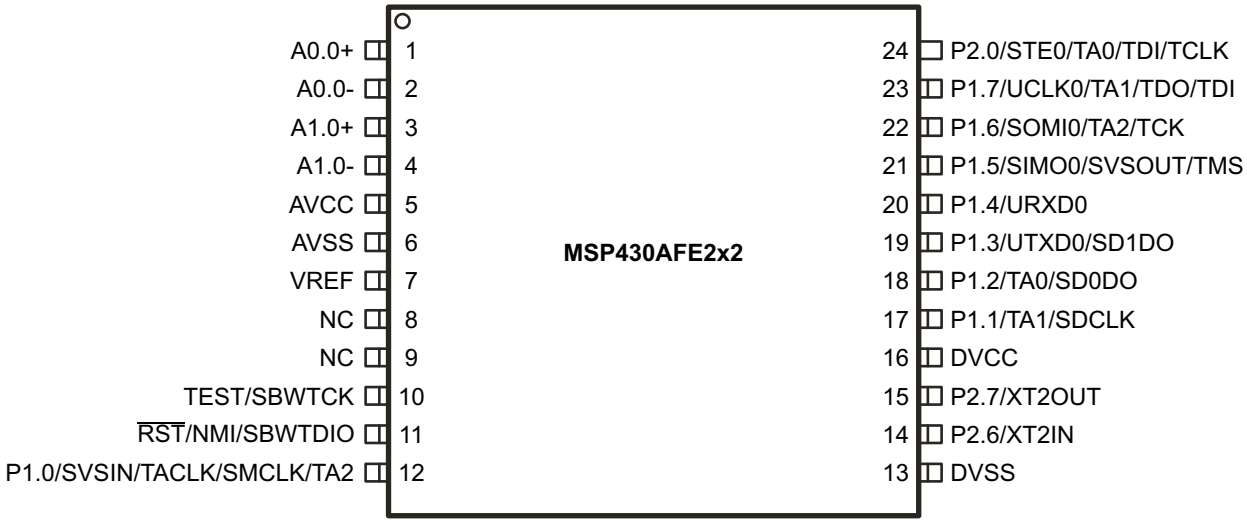
### Functional Block Diagram




### Pin Designation, MSP430AFE2x3IPW

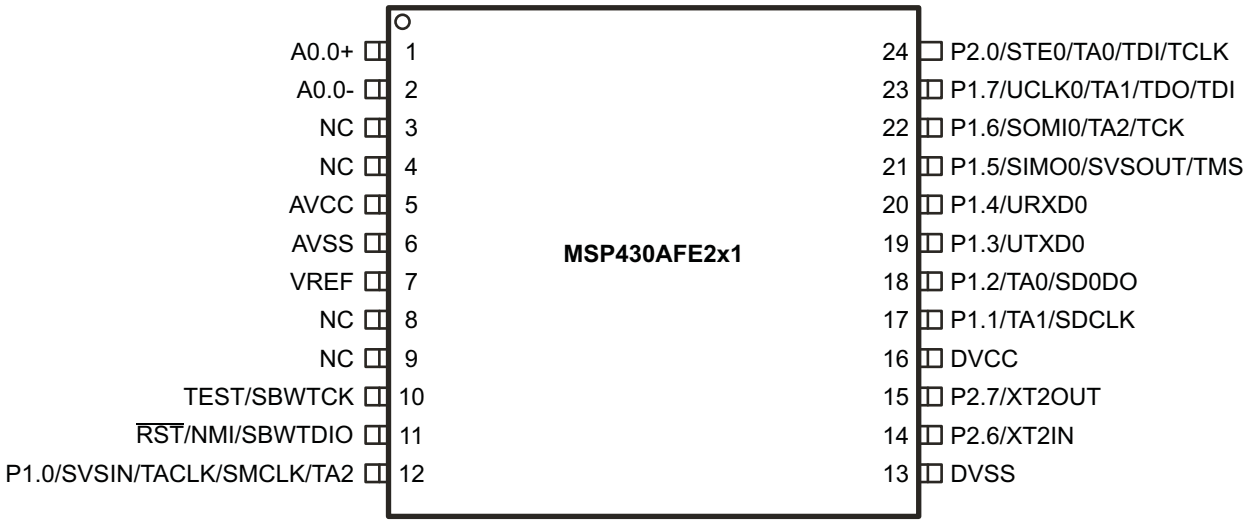


## Pin Designation, MSP430AFE2x2IPW




A. Connect NC pins to analog ground (AVSS)

## Pin Designation, MSP430AFE2x1IPW




B. Connect NC pins to analog ground (AVSS)

**Table 2. Terminal Functions**

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A0.0+ | 1 | I | SD24_A positive analog input A0.0 (1) |
| A0.0- | 2 | I | SD24_A negative analog input A0.0 (1) |
| A1.0+ | 3 | I | SD24_A positive analog input A1.0 (not available on MSP430AFE2x1) (1) |
| A1.0- | 4 | I | SD24_A negative analog input A1.0 (not available on MSP430AFE2x1) (1) |
| AVCC | 5 | | Analog supply voltage, positive terminal. Must not power up prior to DVCC. |
| AVSS | 6 | | Analog supply voltage, negative terminal |
| VREF | 7 | I/O | Input for an external reference voltage/<br>output for internal reference voltage (can be used as mid-voltage) |
| A2.0+ | 8 | I | SD24_A positive analog input A2.0 (not available on MSP430AFE2x2 and MSP430AFE2x1) (1) |
| A2.0- | 9 | I | SD24_A negative analog input A2.0 (not available on MSP430AFE2x2 and MSP430AFE2x1) (1) |
| TEST/SBWTCK | 10 | I | Selects test mode for JTAG pins on P1.5 to P1.7 and P2.0.<br>The device protection fuse is connected to TEST.<br>Spy-Bi-Wire test clock input for device programming and test. |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 11 | I | Reset or nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output for device programming and test. |
| P1.0/SVSIN/TACLK/SMCLK/TA2 | 12 | I/O | General-purpose digital I/O pin<br>Analog input to supply voltage supervisor<br>Timer_A3, clock signal TACLK input<br>SMCLK signal output<br>Timer_A3, compare: Out2 Output |
| DVSS | 13 | | Digital supply voltage, negative terminal |
| P2.6/XT2IN | 14 | I/O | Input terminal of crystal oscillator<br>General-purpose digital I/O pin |
| P2.7/XT2OUT | 15 | I/O | Output terminal of crystal oscillator<br>General-purpose digital I/O pin |
| DVCC | 16 | | Digital supply voltage, positive terminal. |
| P1.1/TA1/SDCLK | 17 | I/O | General-purpose digital I/O pin<br>Timer_A3, capture: CCI1A and CCI1B inputs, compare: Out1 output<br>SD24_A bit stream clock output |
| P1.2/TA0/SD0DO | 18 | I/O | General-purpose digital I/O pin<br>Timer_A3, capture: CCI0A and CCI0B inputs, compare: Out0 output<br>SD24_A bit stream data output for channel 0 |
| P1.3/UTXD0/SD1DO | 19 | I/O | General-purpose digital I/O pin<br>Transmit data out - USART0/UART mode<br>SD24_A bit stream data output for channel 1 (not available on MSP430AFE2x1) |
| P1.4/URXD0/SD2DO | 20 | I/O | General-purpose digital I/O pin<br>Receive data in - USART0/UART mode<br>SD24_A bit stream data output for channel 2 (not available on MSP430AFE2x2 and MSP430AFE2x1) |
| P1.5/SIMO0/SVSOUT/TMS | 21 | I/O | General-purpose digital I/O<br>Slave in/master out of USART0/SPI mode<br>SVS: output of SVS comparator<br>JTAG test mode select. TMS is used as an input port for device programming and test. |
| P1.6/SOMI0/TA2/TCK | 22 | I/O | General-purpose digital I/O pin<br>Slave out/master in of USART0/SPI mode<br>Timer_A3, compare: Out2 output<br>JTAG test clock. TCK is the clock input port for device programming and test. |
| P1.7/UCLK0/TA1/TDO/TDI | 23 | I/O | General-purpose digital I/O pin<br>External clock input - USART0/UART or SPI mode, clock output - USART0/SPI mode.<br>Timer_A3, compare: Out1 output<br>JTAG test data output port. TDO/TDI data output or programming data input terminal. |

(1) It is recommended to short unused analog input pairs and connect them to analog ground.

**Table 2. Terminal Functions (continued)**

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P2.0/STE0/TA0/TDI/TCLK | 24 | I/O | General-purpose digital I/O pin<br>Slave transmit enable - USART0/SPI mode.<br>Timer_A3, compare: Out0 output<br>JTAG test data input or test clock input for device programming and test. |

# SHORT-FORM DESCRIPTION

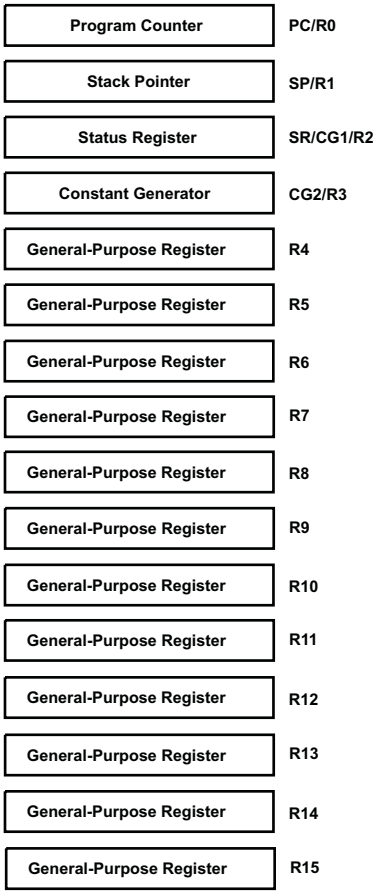
## CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.




## Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

**Table 3. Instruction Word Formats**

| INSTRUCTION FORMAT | EXAMPLE | OPERATION |
|---|---|---|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, unconditional/conditional | JNE | Jump-on-equal bit = 0 |

**Table 4. Address Mode Descriptions**

| ADDRESS MODE | S(1) | D(2) | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | ✓ | ✓ | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | ✓ | ✓ | MOV &MEM,&TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | ✓ | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect autoincrement | ✓ | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate | ✓ | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source
(2) D = destination

## Operating Modes

The MSP430 microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode ( AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
  - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - Crystal oscillator is stopped.

## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

**Table 5. Interrupt Vector Addresses**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| Power up<br>External reset<br>Watchdog<br>Flash key violation<br>PC out-of-range(1) | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV<br>(2) | Reset | 0FFFEh | 15, highest |
| NMI<br>Oscillator fault<br>Flash memory access violation | NMIIFG<br>OFIFG<br>ACCVIFG (2) (3) | (Non)maskable,<br>(Non)maskable,<br>(Non)maskable | 0FFFCh | 14 |
| | | | 0FFFAh | 13 |
| SD24_A | SD24CCTLx SD24OVIFG,<br>SD24CCTLx SD24IFG(2) (4) | Maskable | 0FFF8h | 12 |
| | | | 0FFF6h | 11 |
| Watchdog Timer | WDTIFG | Maskable | 0FFF4h | 10 |
| USART0 Receive | URXIFG0 | Maskable | 0FFF2h | 9 |
| USART0 Transmit | UTXIFG0 | Maskable | 0FFF0h | 8 |
| | | | 0FFEEh | 7 |
| Timer_A3 | TA0CCR0 CCIFG(4) | Maskable | 0FFECh | 6 |
| Timer_A3 | TA0CCR1 CCIFG,<br>TA0CCR2 CCIFG,<br>TA0CTL TAIFG (2) (4) | Maskable | 0FFEAh | 5 |
| I/O Port P1 (eight flags) | P1IFG.0 to P1IFG.7(2) (4) | Maskable | 0FFE8h | 4 |
| | | | 0FFE6h | 3 |
| | | | 0FFE4h | 2 |
| I/O Port P2 (three flags) | P2IFG.0 to P2IFG.2(2) (4) | Maskable | 0FFE2h | 1 |
| | | | 0FFE0h | 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address range.
(2) Multiple source flags
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.

## Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

**Legend**

| | |
|---|---|
| rw | Bit can be read and written. |
| rw-0, 1 | Bit can be read and written. It is Reset or Set by PUC. |
| rw-(0), (1) | Bit can be read and written. It is Reset or Set by POR. |
| | SFR bit is not present in device. |

**Table 6. Interrupt Enable 1**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 00h | UTXIE0 | URXIE0 | ACCVIE | NMIIE | | | OFIE | WDTIE |
| | rw-0 | rw-0 | rw-0 | rw-0 | | | rw-0 | rw-0 |

| | |
|---|---|
| WDTIE | Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode. |
| OFIE | Oscillator fault interrupt enable |
| NMIIE | (Non)maskable interrupt enable |
| ACCVIE | Flash access violation interrupt enable |
| URXIE0 | USART0: UART and SPI receive interrupt enable |
| UTXIE0 | USART0: UART and SPI transmit interrupt enable |

**Table 7. Interrupt Enable 2**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 01h | | | | | | | | |

**Table 8. Interrupt Flag Register 1**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 02h | UTXIFG0 | URXIFG0 | | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
| | rw-1 | rw-0 | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

| | |
|---|---|
| WDTIFG | Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on $V_{CC}$ power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode. |
| OFIFG | Flag set on oscillator fault |
| RSTIFG | External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on $V_{CC}$ power up. |
| PORIFG | Power-on reset interrupt flag. Set on $V_{CC}$ power up. |
| NMIIFG | Set via $\overline{RST}$/NMI-pin |
| URXIFG0 | USART0: UART and SPI receive interrupt flag |
| UTXIFG0 | USART0: UART and SPI transmit interrupt flag |

**Table 9. Interrupt Flag Register 2**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 03h | | | | | | | | |

**Table 10. Module Enable Register 1**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 04h | UTXE0 | URXE0<br>USPIE0 | | | | | | |
| | rw-0 | rw-0 | | | | | | |

URXE0 USART0: UART mode receive enable
UTXE0 USART0: UART mode transmit enable
USPIE0 USART0: SPI mode transmit and receive enable

**Table 11. Module Enable Register 2**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 05h | | | | | | | | |

## Memory Organization

**Table 12. Memory Organization**

| | | MSP430AFE22x | MSP430AFE23x | MSP430AFE25x |
|---|---|---|---|---|
| Memory<br>Main: interrupt vector<br>Main: code memory | Size<br>Flash<br>Flash | 4 KB<br>0xFFFF to 0xFFE0<br>0xFFFF to 0xF000 | 8 KB<br>0xFFFF to 0xFFE0<br>0xFFFF to 0xE000 | 16 KB<br>0xFFFF to 0xFFE0<br>0xFFFF to 0xC000 |
| Information memory | Size<br>Flash | 256 Byte<br>0x10FFh to 0x1000 | 256 Byte<br>0x10FFh to 0x1000 | 256 Byte<br>0x10FFh to 0x1000 |
| RAM | Size | 256 Byte<br>0x02FF to 0x0200 | 512 Byte<br>0x03FF to 0x0200 | 512 Byte<br>0x03FF to 0x0200 |
| Peripherals | 16-bit<br>8-bit<br>8-bit SFR | 0x01FF to 0x0100<br>0x00FF to 0x0010<br>0x000F to 0x0000 | 0x01FF to 0x0100<br>0x00FF to 0x0010<br>0x000F to 0x0000 | 0x01FF to 0x0100<br>0x00FF to 0x0010<br>0x000F to 0x0000 |

## Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

## Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

## Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for an internal digitally controlled oscillator (DCO), a high-frequency crystal oscillator, and an internal very-low-power low-frequency oscillator (VLO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from the VLO
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules

**Table 13. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)**

| DCO FREQUENCY | CALIBRATION REGISTER | SIZE | ADDRESS |
|---|---|---|---|
| 8 MHz | CALBC1_8MHZ | byte | 010FDh |
| | CALDCO_8MHZ | byte | 010FCh |
| 12 MHz | CALBC1_12MHZ | byte | 010FBh |
| | CALDCO_12MHZ | byte | 010FAh |

## Brownout, Supply Voltage Supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, $V_{CC}$ may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until $V_{CC}$ reaches $V_{CC(min)}$ . If desired, the SVS circuit can be used to determine when $V_{CC}$ reaches $V_{CC(min)}$.

## Digital I/O

There are two I/O ports implemented: 8-bit port P1 and 3-bit port P2.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and three bits of port P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Because there are only three I/O pins implemented from port P2, bits [5:1] of all port P2 registers read as 0, and write data is ignored.

## Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

## Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 14. Timer_A3 Signal Connections**

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---|---|---|---|---|---|
| 24-PIN PW | | | | | 24-PIN PW |
| 12 - P1.0 | TACLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 12 - P1.0 | $\overline{\text{TACLK}}$ | INCLK | | | |
| 18 - P1.2 | TA0 | CCI0A | CCR0 | TA0 | 18 - P1.2 |
| 18 - P1.2 | TA0 | CCI0B | | | 24 - P2.0 |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| 17 - P1.1 | TA1 | CCI1A | CCR1 | TA1 | 17 - P1.1 |
| 17 - P1.1 | TA1 | CCI1B | | | 23 - P1.7 |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| | DVSS | CCI2A | CCR2 | TA2 | 12 - P1.0 |
| | ACLK (internal) | CCI2B | | | 22 - P1.6 |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |

## USART0

The MSP430AFE2xx devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART0 module supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. The maximum operational frequency for the USART0 module is 8 MHz.

## Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

## SD24_A

The SD24_A module integrates up to three independent 24-bit sigma-delta A/D converters. Each channel is designed with fully differential analog input pair and programmable gain amplifier input stage. In addition to external analog inputs, an internal VCC sense and temperature sensor are also available.

## Peripheral File Map

### Table 15. Peripherals With Word Access

| | | | |
|---|---|---|---|
| **Timer_A3** | Capture/compare register 2 | TACCR2 | 0x0176 |
| | Capture/compare register 1 | TACCR1 | 0x0174 |
| | Capture/compare register 0 | TACCR0 | 0x0172 |
| | Timer_A register | TAR | 0x0170 |
| | Capture/compare control 2 | TACCTL2 | 0x0166 |
| | Capture/compare control 1 | TACCTL1 | 0x0164 |
| | Capture/compare control 0 | TACCTL0 | 0x0162 |
| | Timer_A control | TACTL | 0x0160 |
| | Timer_A interrupt vector | TAIV | 0x012E |
| **Hardware Multiplier** | Sum extend | SUMEXT | 0x013E |
| | Result high word | RESHI | 0x013C |
| | Result low word | RESLO | 0x013A |
| | Second operand | OP2 | 0x0138 |
| | Multiply signed + accumulate/operand 1 | MACS | 0x0136 |
| | Multiply + accumulate/operand 1 | MAC | 0x0134 |
| | Multiply signed/operand 1 | MPYS | 0x0132 |
| | Multiply unsigned/operand 1 | MPY | 0x0130 |
| **Flash Memory** | Flash control 3 | FCTL3 | 0x012C |
| | Flash control 2 | FCTL2 | 0x012A |
| | Flash control 1 | FCTL1 | 0x0128 |
| **Watchdog Timer+** | Watchdog/timer control | WDTCTL | 0x0120 |
| **SD24_A (also see Table 16)** | General Control | SD24CTL | 0x0100 |
| | Channel 0 Control | SD24CCTL0 | 0x0102 |
| | Channel 1Control | SD24CCTL1 | 0x0104 |
| | Channel 2 Control | SD24CCTL2 | 0x0106 |
| | Channel 0 conversion memory | SD24MEM0 | 0x0110 |
| | Channel 1 conversion memory | SD24MEM1 | 0x0112 |
| | Channel 2 conversion memory | SD24MEM2 | 0x0114 |
| | SD24 Interrupt vector word register | SD24IV | 0x01AE |

**Table 16. Peripherals With Byte Access**

| | | | |
|---|---|---|---|
| **SD24_A (also see Table 15)** | Channel 0 Input Control | SD24INCTL0 | 0x00B0 |
| | Channel 1 Input Control | SD24INCTL1 | 0x00B1 |
| | Channel 2 Input Control | SD24INCTL2 | 0x00B2 |
| | Channel 0 Preload | SD24PRE0 | 0x00B8 |
| | Channel 1 Preload | SD24PRE1 | 0x00B9 |
| | Channel 2 Preload | SD24PRE2 | 0x00BA |
| | Reserved (Internal SD24_A Configuration 1) | SD24CONF1 | 0x00BF |
| **USART0** | Transmit buffer | U0TXBUF | 0x0077 |
| | Receive buffer | U0RXBUF | 0x0076 |
| | Baud rate | U0BR1 | 0x0075 |
| | Baud rate | U0BR0 | 0x0074 |
| | Modulation control | U0MCTL | 0x0073 |
| | Receive control | U0RCTL | 0x0072 |
| | Transmit control | U0TCTL | 0x0071 |
| | USART control | U0CTL | 0x0070 |
| **Basic Clock System+** | Basic clock system control 3 | BCSCTL3 | 0x0053 |
| | Basic clock system control 2 | BCSCTL2 | 0x0058 |
| | Basic clock system control 1 | BCSCTL1 | 0x0057 |
| | DCO clock frequency control | DCOCTL | 0x0056 |
| **Brownout, SVS** | SVS control register (reset by brownout signal) | SVSCTL | 0x0055 |
| **Port P2** | Port P2 selection 2 | P2SEL2 | 0x0042 |
| | Port P2 resistor enable | P2REN | 0x002F |
| | Port P2 selection | P2SEL | 0x002E |
| | Port P2 interrupt enable | P2IE | 0x002D |
| | Port P2 interrupt edge select | P2IES | 0x002C |
| | Port P2 interrupt flag | P2IFG | 0x002B |
| | Port P2 direction | P2DIR | 0x002A |
| | Port P2 output | P2OUT | 0x0029 |
| | Port P2 input | P2IN | 0x0028 |
| **Port P1** | Port P1 selection 2 register | P1SEL2 | 0x0041 |
| | Port P1 resistor enable | P1REN | 0x0027 |
| | Port P1 selection | P1SEL | 0x0026 |
| | Port P1 interrupt enable | P1IE | 0x0025 |
| | Port P1 interrupt edge select | P1IES | 0x0024 |
| | Port P1 interrupt flag | P1IFG | 0x0023 |
| | Port P1 direction | P1DIR | 0x0022 |
| | Port P1 output | P1OUT | 0x0021 |
| | Port P1 input | P1IN | 0x0020 |
| **Special Function** | SFR module enable 2 | ME2 | 0x0005 |
| | SFR module enable 1 | ME1 | 0x0004 |
| | SFR interrupt flag 2 | IFG2 | 0x0003 |
| | SFR interrupt flag 1 | IFG1 | 0x0002 |
| | SFR interrupt enable 2 | IE2 | 0x0001 |
| | SFR interrupt enable 1 | IE1 | 0x0000 |

## Absolute Maximum Ratings(1)

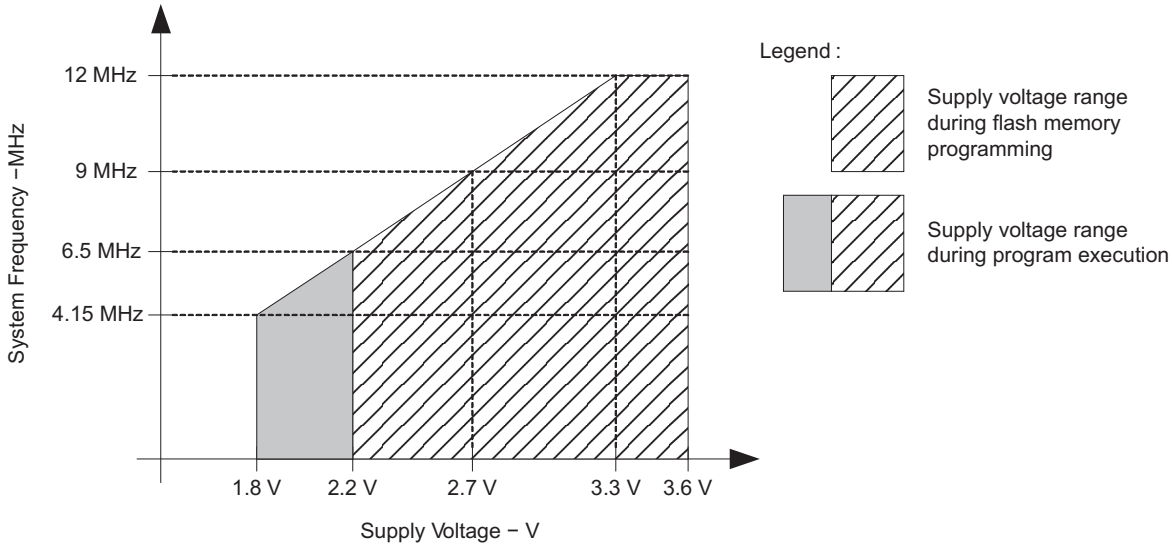
| | | |
|---|---|---|
| Voltage applied at $V_{CC}$ to $V_{SS}$ | | -0.3 V to 4.1 V |
| Voltage applied to any pin(2) | | -0.3 V to $V_{CC}$ + 0.3 V |
| Diode current at any device terminal | | ±2 mA |
| Storage temperature, $T_{stg}$(3) | Unprogrammed device | -55°C to 150°C |
| | Programmed device | -40°C to 85°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to VSS. The JTAG fuse-blow voltage, $V_{FB}$, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## Recommended Operating Conditions(1) (2)

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | AVCC = DVCC = $V_{CC}$(1) | During program execution(3) | 1.8 | | 3.6 | V |
| | | | During program/erase flash memory | 2.2 | | 3.6 | V |
| $V_{SS}$ | Supply voltage | AVSS = DVSS = $V_{SS}$ | | | 0 | | V |
| $T_A$ | Operating free-air temperature | | | -40 | | 85 | °C |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(1) (2) (see Figure 1) | $V_{CC}$ = 1.8 V, Duty cycle = 50% ±10% | | dc | | 4.15 | MHz |
| | | $V_{CC}$ = 2.7 V, Duty cycle = 50% ±10% | | dc | | 9 | |
| | | $V_{CC}$ ≥ 3.3 V, Duty cycle = 50% ±10% | | dc | | 12 | |

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(3) The operating voltage range for SD24_A is 2.5 V to 3.6 V




A. Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum $V_{CC}$ of 2.2 V.

B. If high frequency crystal used is above 12 MHz and selected to source CPU clock then MCLK divider should be programmed appropriately to run CPU below 8 MHz.

**Figure 1. Operating Area**

## Active Mode Supply Current (into $DV_{CC}$ + $AV_{CC}$) Excluding External Current(1)

| PARAMETER | | TEST CONDITIONS | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{AM, 1MHz}$ | Active mode (AM) current at 1 MHz | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = DCO default frequency (approximately 1 MHz), $f_{ACLK} = f_{VLO}$ = 12 kHz, Program executes in flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | | 2.2 V | | 220 | | µA |
| | | | | 3 V | | 350 | | |
| $I_{AM, 12MHz}$ | Active mode (AM) current at 12 MHz | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 12 MHz, $f_{ACLK} = f_{VLO}$ = 12 kHz, Program executes in flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | | 3.3 V | | 4.0 | 4.5 | mA |

(1) All inputs are tied to 0 V or $V_{CC}$. Outputs do not source or sink any current.

## Typical Characteristics – Active-Mode Supply Current (Into $DV_{CC}$ + $AV_{CC}$)

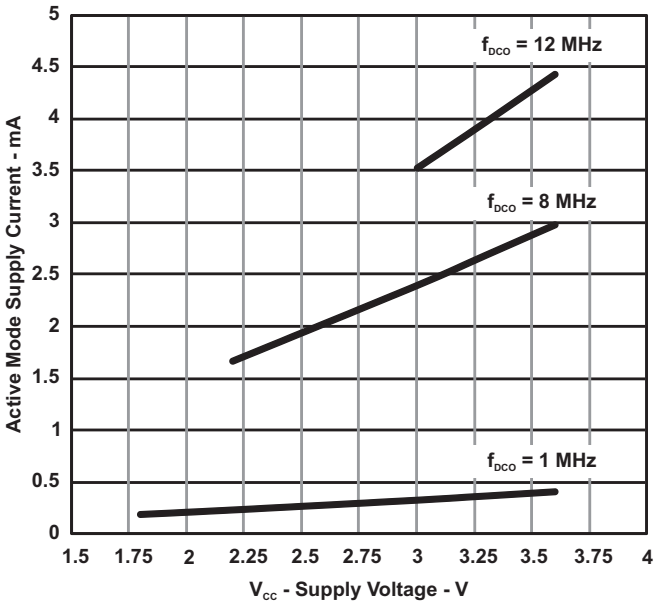



**Figure 2. Active-Mode Current vs $V_{CC}$, $T_A$ = 25°C**

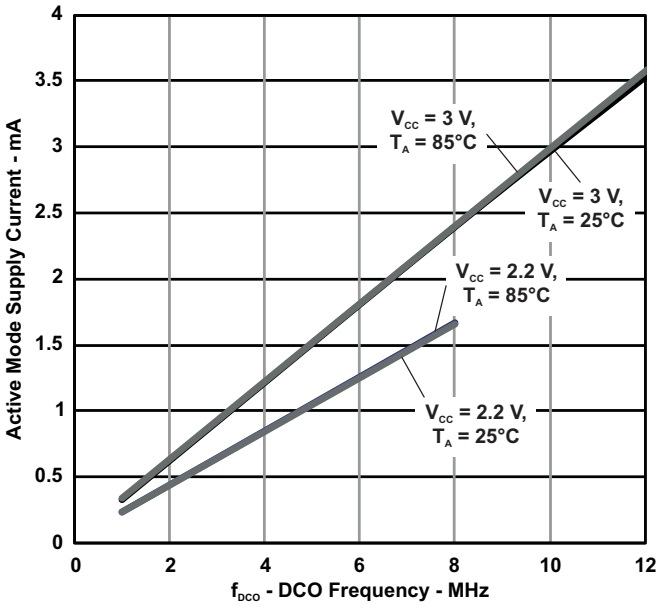



**Figure 3. Active-Mode Current vs DCO Frequency**

## Low-Power-Mode Supply Currents (Into $V_{CC}$) Excluding External Current (1)

| PARAMETER | | TEST CONDITIONS | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{LPM0}$ | Low-power mode 0 (LPM0) current(2) | $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = DCO default frequency (approximately 1 MHz), $f_{ACLK}$ = $f_{VLO}$ = 12 kHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 25°C | 2.2 V | | 65 | | µA |
| $I_{LPM2}$ | Low-power mode 2 (LPM2) current(3) | $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{DCO}$ = DCO default frequency (approximately 1 MHz), $f_{ACLK}$ = $f_{VLO}$ = 12 kHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 22 | | µA |
| $I_{LPM3,VLO}$ | Low-power mode 3 (LPM3) current(3) | $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = $f_{VLO}$ = 12 kHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.5 | 1.0 | µA |
| $I_{LPM4}$ | Low-power mode 4 (LPM4) current(4) | $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = $f_{VLO}$ = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | 25°C | 2.2 V | | 0.1 | 0.7 | µA |
| | | | 85°C | | | 1.1 | 2.5 | |

(1) All inputs are tied to 0 V or $V_{CC}$. Outputs do not source or sink any current.
(2) Current for brownout and WDT clocked by SMCLK included.
(3) Current for brownout and WDT clocked by ACLK included.
(4) Current for brownout included.

### Typical Characteristics – LPM4 Current

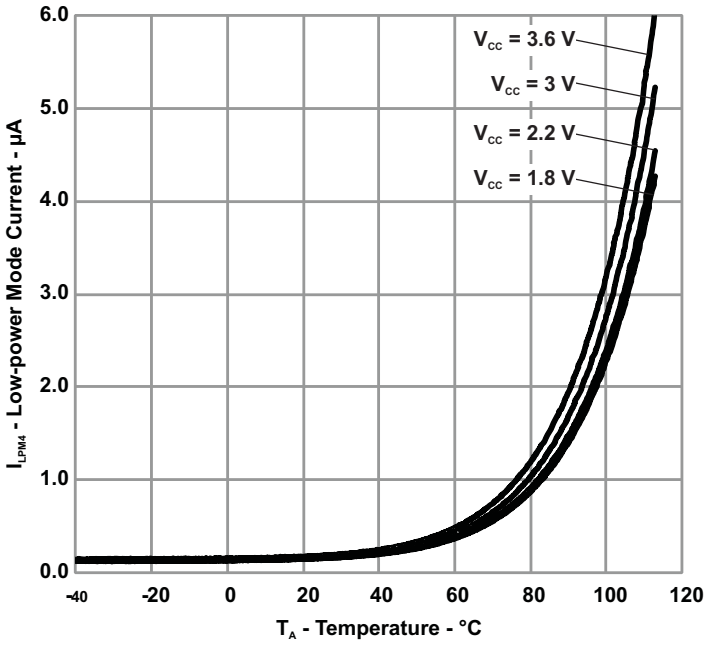



**Figure 4. $I_{LPM4}$ -- LPM4 Current vs Temperature**

## Schmitt-Trigger Inputs (Ports Px and $\overline{\text{RST}}$/NMI)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | | 0.45 $V_{CC}$ | | 0.75 $V_{CC}$ | V |
| | | | 3 V | 1.35 | | 2.25 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | | 0.25 $V_{CC}$ | | 0.55 $V_{CC}$ | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+}$ - $V_{IT-}$) | | 3 V | 0.3 | | 1.0 | V |
| $R_{Pull}$ | Pullup/pulldown resistor (not $\overline{\text{RST}}$/NMI pin) | For pullup: $V_{IN} = V_{SS}$; For pulldown: $V_{IN} = V_{CC}$ | 3 V | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

## Leakage Current (Ports Px)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{lkg(Px.y)}$ | High-impedance leakage current | (1) (2) | 3 V | | | ±50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## Outputs (Ports Px)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH(max)}$ = -6 mA (1) | 3 V | | $V_{CC}$ – 0.2 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL(max)}$ = 6 mA (1) | 3 V | | $V_{SS}$ + 0.2 | | V |

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

## Output Frequency (Ports Px)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | Px.y, $C_L$ = 20 pF, $R_L$ = 1 kΩ (1) (2) | 3 V | | 12 | | MHz |
| $f_{Port\_CLK}$ | Clock output frequency | Px.y, $C_L$ = 20 pF (2) | 3 V | | 16 | | MHz |

(1) A resistive divider with two 0.5-kΩ resistors between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

## Typical Characteristics – Outputs

One output loaded at a time.

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

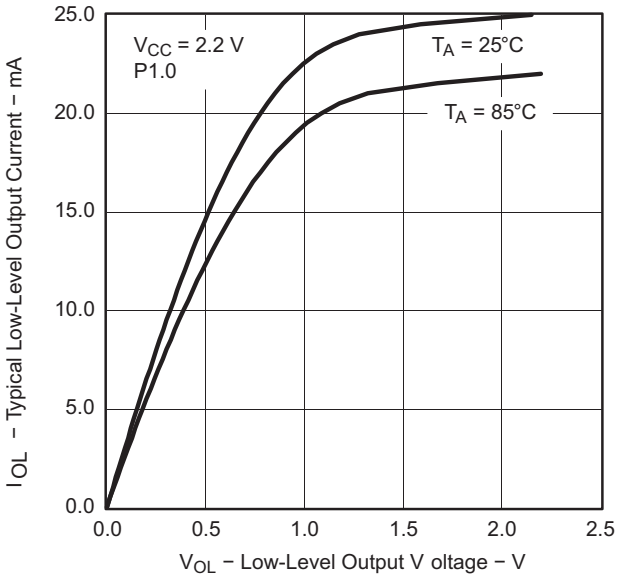



**Figure 5.**

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

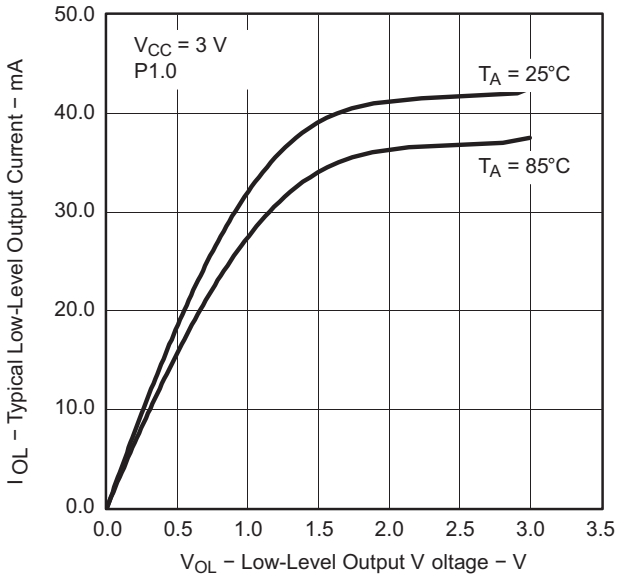



**Figure 6.**

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

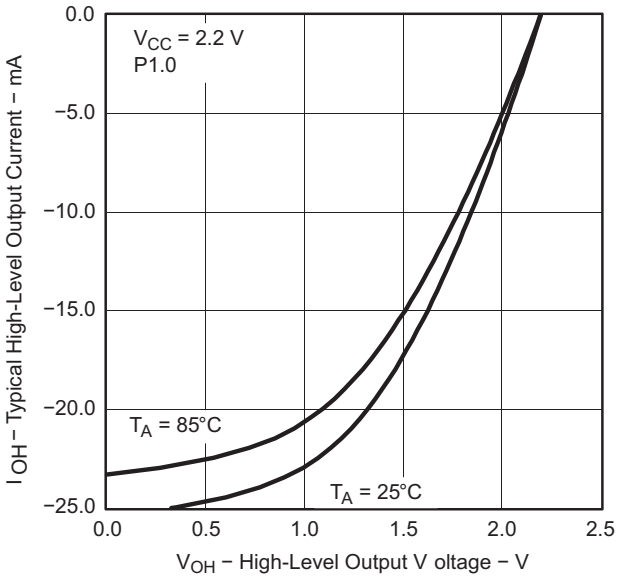



**Figure 7.**

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

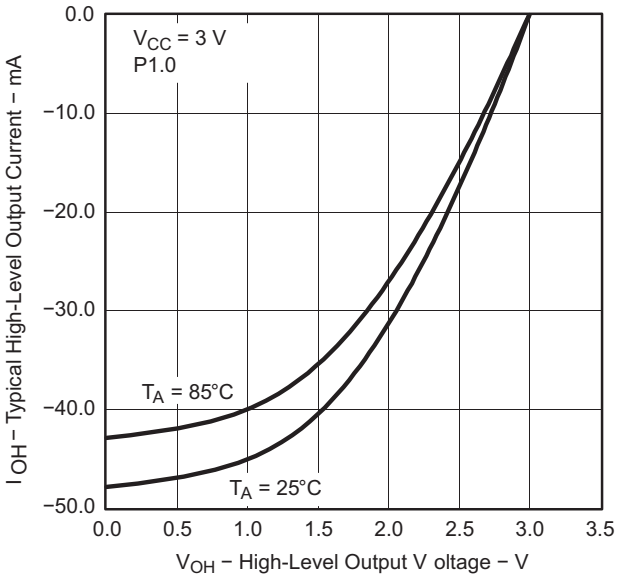



**Figure 8.**

## POR/Brownout Reset (BOR)(1) (2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(start)}$ | See Figure 9 | $dV_{CC}/dt \le 3$ V/s | | | 0.7 × $V_{(B\_IT-)}$ | | V |
| $V_{(B\_IT-)}$ | See Figure 9 through Figure 11 | $dV_{CC}/dt \le 3$ V/s | | | 1.42 | | V |
| $V_{hys(B\_IT-)}$ | See Figure 9 | $dV_{CC}/dt \le 3$ V/s | | | 120 | | mV |
| $t_{d(BOR)}$ | See Figure 9 | | | | 2000 | | µs |
| $t_{(reset)}$ | Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally | | 3 V | 2 | | | µs |

(1) The current consumption of the brownout module is already included in the $I_{CC}$ current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

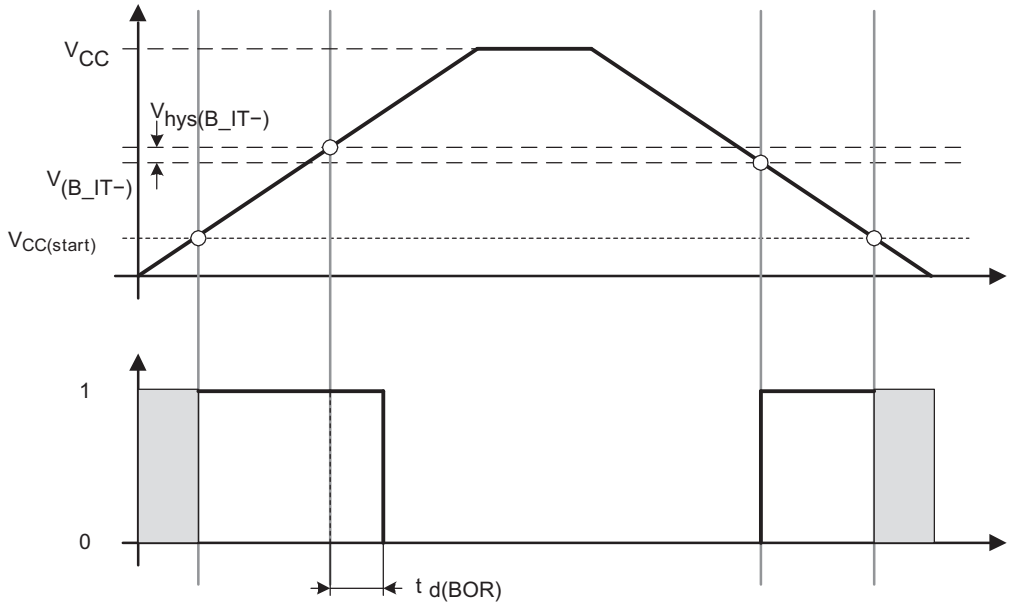



**Figure 9. POR/Brownout Reset (BOR) vs Supply Voltage**

## Typical Characteristics – POR/Brownout Reset (BOR)

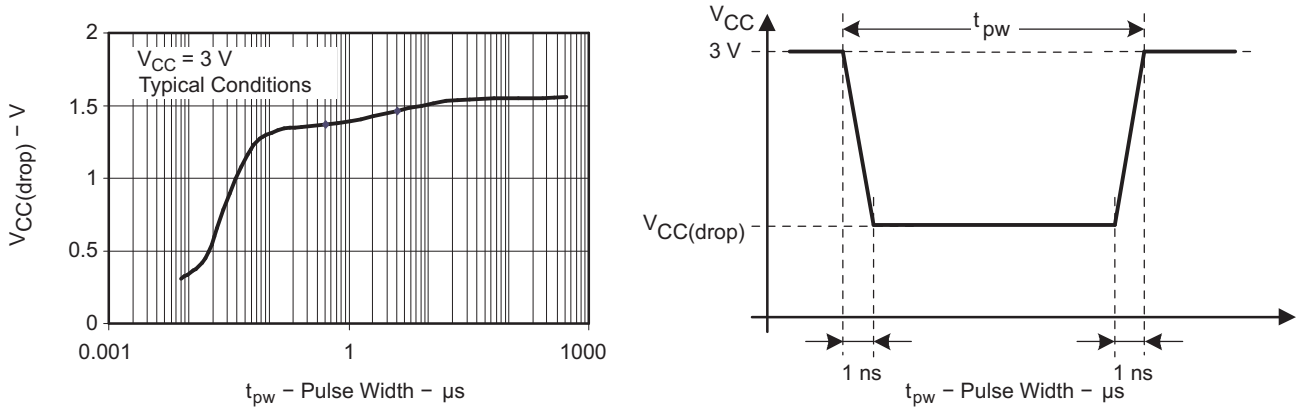



**Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal**

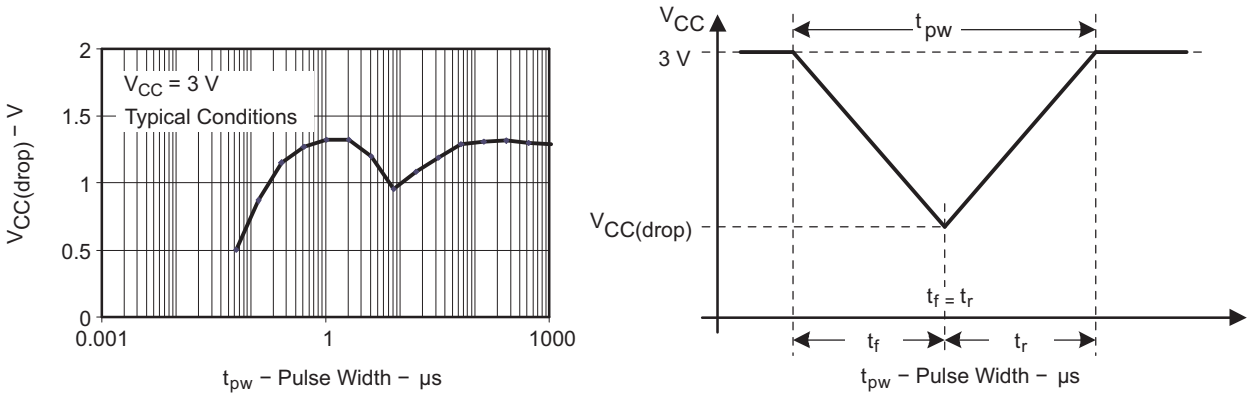



**Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**

## Supply Voltage Supervisor (SVS) / Supply Voltage Monitor (SVM)(1)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(SVSR)}$ | $dV_{CC}/dt$ > 30 V/ms (see Figure 12) | | | 100 | | µs |
| | $dV_{CC}/dt$ ≤ 30 V/ms | | | 2000 | | |
| $t_{d(SVSon)}$ | SVS on, switch from VLD = 0 to VLD ≠ 0, $V_{CC}$ =3 V | | | 100 | | µs |
| $t_{settle}$ | VLD ≠ 0(2) | | | 12 | | µs |
| $V_{(SVSstart)}$ | VLD ≠ 0, $V_{CC}/dt$ ≤ 3 V/s (see Figure 12) | | | 1.55 | 1.7 | V |
| $V_{hys(SVS\_IT-)}$ | $V_{CC}/dt$ ≤ 3 V/s (see Figure 12) | VLD = 1 | | 120 | | mV |
| | | VLD = 2 to 14 | | 15 | | mV |
| | $V_{CC}/dt$ ≤ 3 V/s (see Figure 12), external voltage applied on SVSIN | VLD = 15 | | 10 | | mV |
| $V_{(SVS\_IT-)}$ | $V_{CC}/dt$ ≤ 3V/s (see Figure 12) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | | 2.1 | | |
| | | VLD = 3 | | 2.2 | | |
| | | VLD = 4 | | 2.3 | | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | | 2.5 | | |
| | | VLD = 7 | | 2.65 | | |
| | | VLD = 8 | | 2.8 | | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | | 3.05 | | |
| | | VLD = 11 | | 3.2 | | |
| | | VLD = 12 | | 3.35 | | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76(3) | |
| | | VLD = 14 | | 3.7(3) | | |
| | $V_{CC}/dt$ ≤ 3 V/s (see Figure 12), external voltage applied on SVSIN | VLD = 15 | 1.1 | 1.2 | 1.3 | |
| $I_{CC(SVS)}$(1) | VLD ≠ 0, $V_{CC}$ = 3 V | | | 12 | 17 | µA |

(1) The current consumption of the SVS module is not included in the $I_{CC}$ current consumption data.
(2) $t_{settle}$ is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.
(3) The recommended operating voltage range is limited to 3.6 V.

## Typical Characteristics – SVS

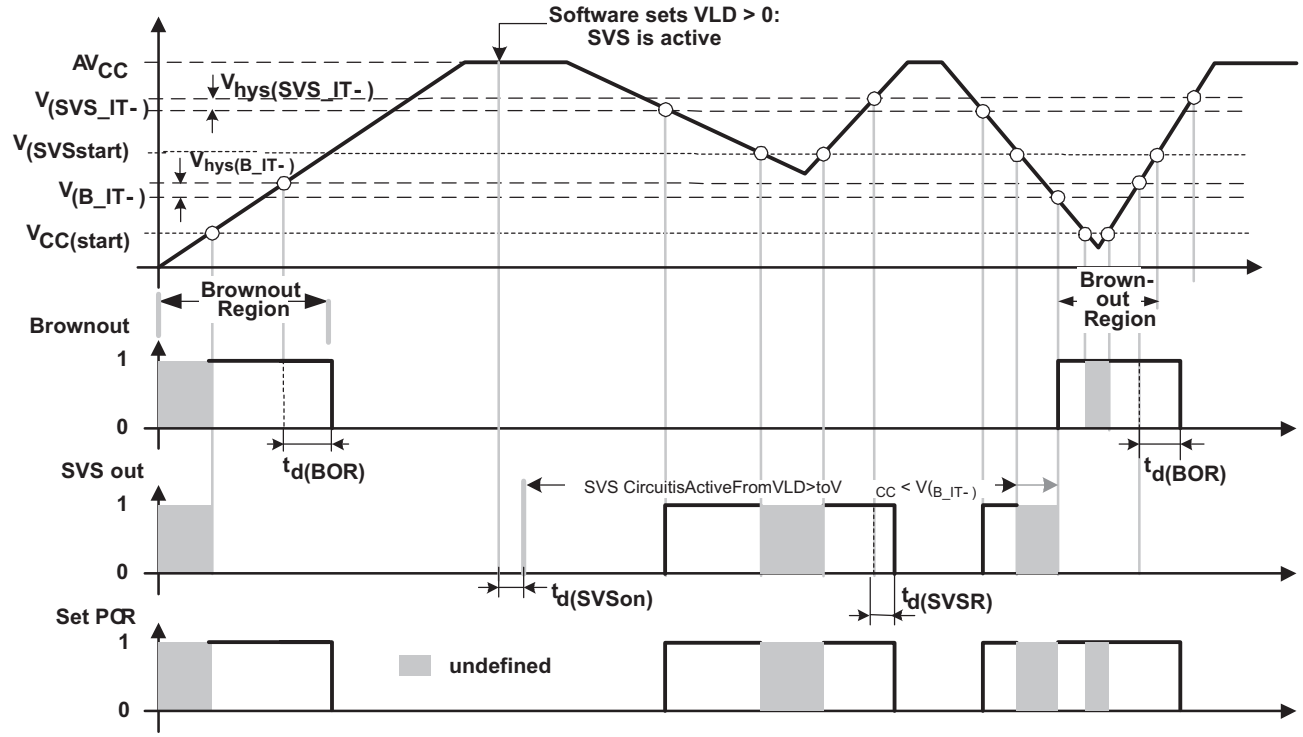



**Figure 12. SVS Reset (SVSR) vs Supply Voltage**

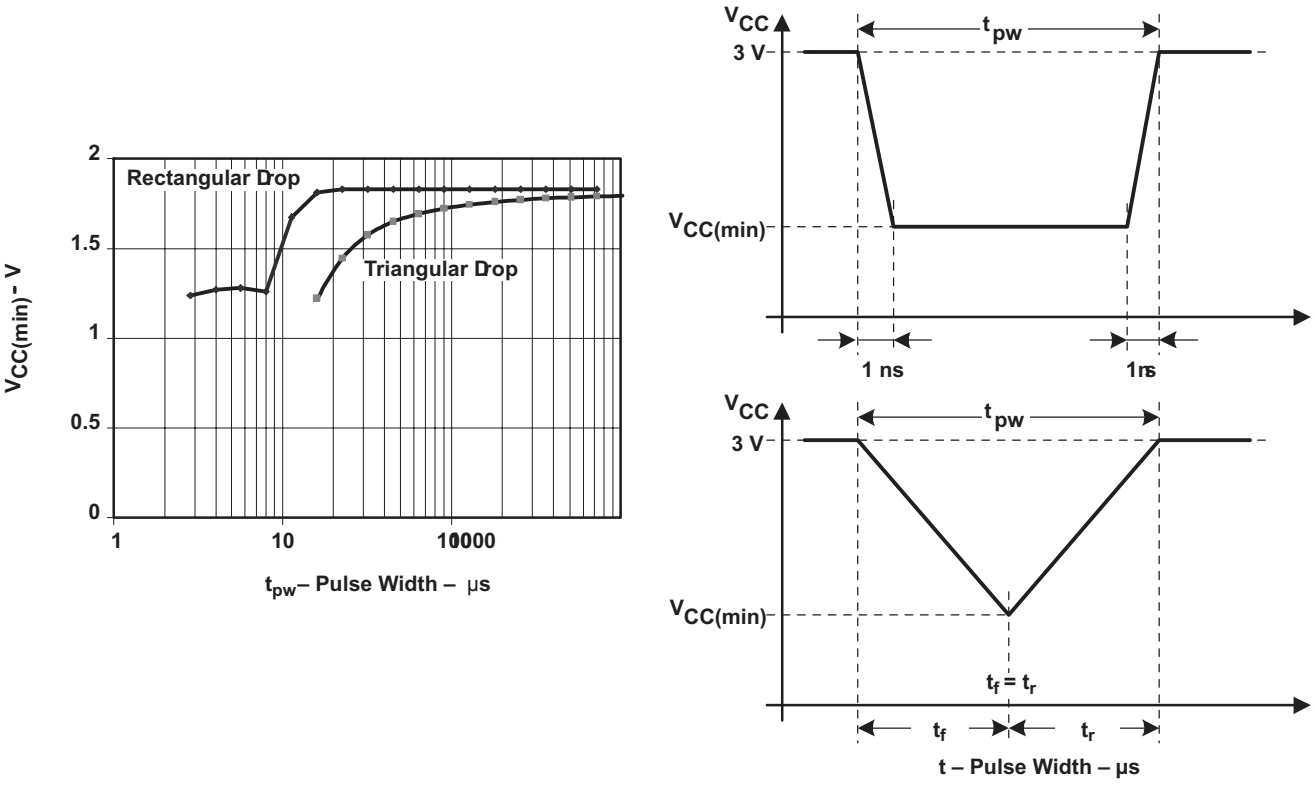



**Figure 13. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal**

## Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter $S_{DCO}$.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

## DCO Frequency

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | RSELx < 14 | | 1.8 | | 3.6 | V |
| | | RSELx = 14 | | 2.2 | | 3.6 | |
| | | RSELx = 15 | | 3.0 | | 3.6 | |
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) | RSELx = 0, DCOx = 0, MODx = 0 | 3.3 V | 0.06 | 0.10 | 0.14 | MHz |
| $f_{DCO(0,3)}$ | DCO frequency (0, 3) | RSELx = 0, DCOx = 3, MODx = 0 | 3.3 V | | 0.12 | | MHz |
| $f_{DCO(1,3)}$ | DCO frequency (1, 3) | RSELx = 1, DCOx = 3, MODx = 0 | 3.3 V | | 0.15 | | MHz |
| $f_{DCO(2,3)}$ | DCO frequency (2, 3) | RSELx = 2, DCOx = 3, MODx = 0 | 3.3 V | | 0.21 | | MHz |
| $f_{DCO(3,3)}$ | DCO frequency (3, 3) | RSELx = 3, DCOx = 3, MODx = 0 | 3.3 V | | 0.30 | | MHz |
| $f_{DCO(4,3)}$ | DCO frequency (4, 3) | RSELx = 4, DCOx = 3, MODx = 0 | 3.3 V | | 0.41 | | MHz |
| $f_{DCO(5,3)}$ | DCO frequency (5, 3) | RSELx = 5, DCOx = 3, MODx = 0 | 3.3 V | | 0.58 | | MHz |
| $f_{DCO(6,3)}$ | DCO frequency (6, 3) | RSELx = 6, DCOx = 3, MODx = 0 | 3.3 V | | 0.80 | | MHz |
| $f_{DCO(7,3)}$ | DCO frequency (7, 3) | RSELx = 7, DCOx = 3, MODx = 0 | 3.3 V | | 1.15 | | MHz |
| $f_{DCO(8,3)}$ | DCO frequency (8, 3) | RSELx = 8, DCOx = 3, MODx = 0 | 3.3 V | | 1.60 | | MHz |
| $f_{DCO(9,3)}$ | DCO frequency (9, 3) | RSELx = 9, DCOx = 3, MODx = 0 | 3.3 V | | 2.30 | | MHz |
| $f_{DCO(10,3)}$ | DCO frequency (10, 3) | RSELx = 10, DCOx = 3, MODx = 0 | 3.3 V | | 3.40 | | MHz |
| $f_{DCO(11,3)}$ | DCO frequency (11, 3) | RSELx = 11, DCOx = 3, MODx = 0 | 3.3 V | | 4.25 | | MHz |
| $f_{DCO(12,3)}$ | DCO frequency (12, 3) | RSELx = 12, DCOx = 3, MODx = 0 | 3.3 V | | 5.80 | | M Hz |
| $f_{DCO(13,3)}$ | DCO frequency (13, 3) | RSELx = 13, DCOx = 3, MODx = 0 | 3.3 V | | 7.80 | | MHz |
| $f_{DCO(14,3)}$ | DCO frequency (14, 3) | RSELx = 14, DCOx = 3, MODx = 0 | 3.3 V | 8.6 | 11.25 | 13.9 | MHz |
| $f_{DCO(15,3)}$ | DCO frequency (15, 3) | RSELx = 15, DCOx = 3, MODx = 0 | 3.3 V | | 15.30 | | MHz |
| $f_{DCO(15,7)}$ | DCO frequency (15, 7) | RSELx = 15, DCOx = 7, MODx = 0 | 3.3 V | | 21.00 | | MHz |
| $S_{RSEL}$ | Frequency step between range RSEL and RSEL+1 | $S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$ | 3.3 V | | 1.35 | | ratio |
| $S_{DCO}$ | Frequency step between tap DCO and DCO+1 | $S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$ | 3.3 V | | 1.08 | | ratio |
| | Duty cycle | Measured at SMCLK output | 3.3 V | | 50 | | % |

## Calibrated DCO Frequencies – Tolerance

| PARAMETER | TEST CONDITIONS | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| 8-MHz tolerance over temperature(1) | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3.3V | 0°C to 85°C | 3.3 V | 7.76 | 8 | 8.24 | MHz |
| 8-MHz tolerance over $V_{CC}$ | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3.3V | 30°C | 2.7 V to 3.6 V | 7.76 | 8 | 8.24 | MHz |
| 8-MHz tolerance overall | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3.3V | -40°C to 85°C | 2.7 V to 3.6 V | 7.52 | 8 | 8.48 | MHz |
| 12-MHz tolerance over temperature(1) | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3.3V | 0°C to 85°C | 3.3 V | 11.64 | 12 | 12.36 | MHz |
| 12-MHz tolerance over $V_{CC}$ | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3.3V | 30°C | 3.3 V to 3.6 V | 11.64 | 12 | 12.36 | MHz |
| 12-MHz tolerance overall | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3.3V | -40°C to 85°C | 3.3 V to 3.6 V | 11.28 | 12 | 12.72 | MHz |

(1) This is the frequency change from the measured frequency at 30°C over temperature.

## Wake-Up From Lower-Power Modes (LPM3/4)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{DCO,LPM3/4}$ | DCO clock wake-up time from LPM3/4(1) | $f_{DCO}$ = DCO default frequency (approximately 1 MHz) | 3 V | | 1.5 | | µs |
| $t_{CPU,LPM3/4}$ | CPU wake-up time from LPM3/4(2) | | | | $1 / f_{MCLK} + t_{DCO,LPM3/4}$ | | µs |

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

### Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

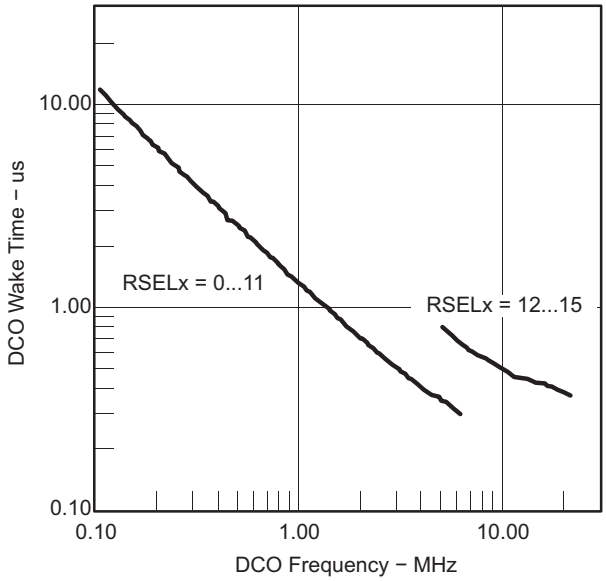



**Figure 14. Clock Wake-Up Time From LPM3 vs DCO Frequency**

## Internal Very-Low-Power Low-Frequency Oscillator (VLO)

| PARAMETER | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | -40°C to 85°C | 3 V | 4 | 12 | 22 | kHz |
| $df_{VLO}/dT$ | VLO frequency temperature drift(1) | -40°C to 85°C | 3 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift(2) | 25°C | 1.8 V to 3.6 V | | 4 | | %/V |

(1) Calculated using the box method: [MAX(-40...85°C) - MIN(-40...85°C)]/MIN(-40...85°C)/[85°C - (-40°C)]
(2) Calculated using the box method: [MAX(1.8...3.6 V) - MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V - 1.8 V)

## Crystal Oscillator (XT2)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{XT2,HF0}$ | XT2 oscillator crystal frequency, HF mode 0 | XT2OFF = 0, XT2Sx = 0 | 1.8 V to 3.6 V | 0.4 | | 1 | MHz |
| $f_{XT2,HF1}$ | XT2 oscillator crystal frequency, HF mode 1 | XT2OFF = 0, XT2Sx = 1 | 1.8 V to 3.6 V | 1 | | 4 | MHz |
| $f_{XT2,HF2}$ | XT2 oscillator crystal frequency, HF mode 2 | XT2OFF = 0, XT2Sx = 2 | 1.8 V to 2.2 V | 2 | | 10 | MHz |
| | | | 2.2 V to 3.0 V | 2 | | 12 | |
| | | | 3.0 V to 3.6 V | 2 | | 16 | |
| $f_{XT2,HF,logic}$ | XT2 oscillator logic-level square-wave input frequency, HF mode | XT2OFF = 0, XT2Sx = 3 | 1.8 V to 2.2 V | 0.4 | | 10 | MHz |
| | | | 2.2 V to 3.0 V | 0.4 | | 12 | |
| | | | 3.0 V to 3.6 V | 0.4 | | 16 | |
| $OA_{HF}$ | Oscillation allowance for HF crystals (see Figure 15 and Figure 16) | XT2OFF = 0, XT2Sx = 0<br>$f_{XT2,HF}$ = 1 MHz,<br>$C_{L,eff}$ = 15 pF | | | 2700 | | Ω |
| | | XT2OFF = 0, XT2Sx = 1<br>$f_{XT2,HF}$ = 4 MHz,<br>$C_{L,eff}$ = 15 pF | | | 800 | | |
| | | XT2OFF = 0, XT2Sx = 2<br>$f_{XT2,HF}$ = 16 MHz,<br>$C_{L,eff}$ = 15 pF | | | 300 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, HF mode(2) | XT2OFF = 0(3) | | | 1 | | pF |
| | Duty cycle | XT2OFF = 0, Measured at P1.0/SVSIN/TACLK/SMCLK/TA2, $f_{XT2,HF}$ = 10 MHz | 3 V | 40 | 50 | 60 | % |
| | | XT2OFF = 0, Measured at P1.0/SVSIN/TACLK/SMCLK/TA2, $f_{XT2,HF}$ = 16 MHz | | 40 | 50 | 60 | |
| $f_{Fault,HF}$ | Oscillator fault frequency (4) | XT2OFF = 0, XT2Sx = 3(5) | 3 V | 30 | | 300 | kHz |

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
(5) Measured with logic-level input frequency, but also applies to operation with crystals.

## Typical Characteristics – XT2 Oscillator

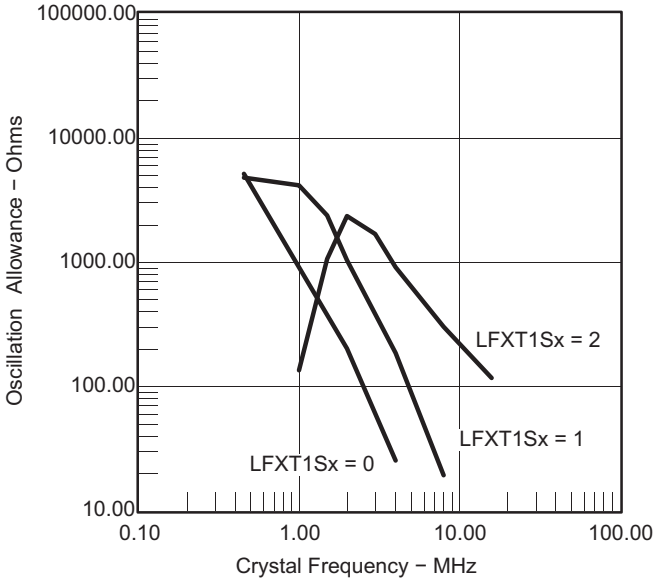



**Figure 15. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, $T_A$ = 25°C**

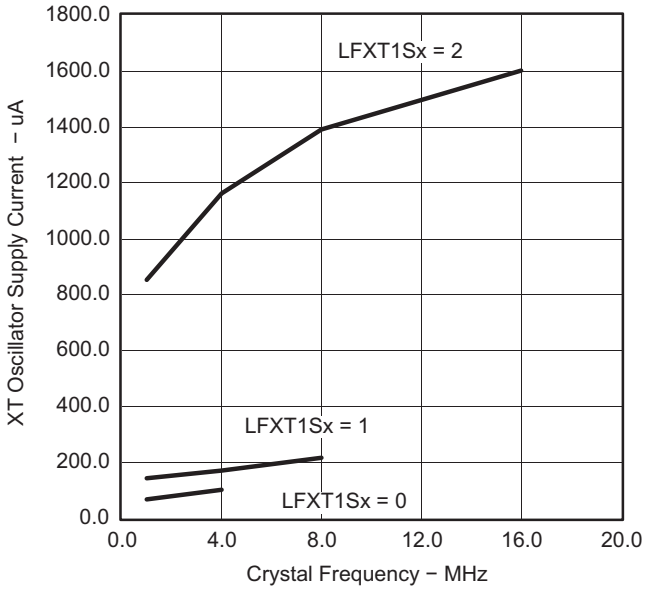



**Figure 16. XT2 Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, $T_A$ = 25°C**

## SD24_A, Power Supply and Recommended Operating Conditions

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC} = DV_{CC}$<br>$AV_{SS} = DV_{SS} = 0$ V | | | 2.5 | | 3.6 | V |
| $I_{SD24}$ | Analog supply current: 1 active SD24_A channel including internal reference | SD24LP = 0, $f_{SD24}$ = 1 MHz, SD24OSR = 256 | GAIN: 1, 2 | 3 V | | 800 | 1100 | µA |
| | | | GAIN: 4, 8, 16 | | | 900 | | |
| | | | GAIN: 32 | | | 1200 | | |
| | | SD24LP = 1, $f_{SD24}$ = 0.5 MHz, SD24OSR = 256 | GAIN: 1 | | | 800 | | |
| | | | GAIN: 32 | | | 900 | | |
| $f_{SD24}$ | Analog front-end input clock frequency | SD24LP = 0 (low-power mode disabled) | | 3 V | 0.03 | 1 | 1.1 | MHz |
| | | SD24LP = 1 (low-power mode enabled) | | | 0.03 | 0.5 | | |

## SD24_A, Input Range[1]

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{ID,FSR}$ | Differential full scale input voltage range | Bipolar mode, SD24UNI = 0 | | | $-V_{REF}$ / 2GAIN | | $+V_{REF}$ / 2GAIN | mV |
| | | Unipolar mode, SD24UNI = 1 | | | 0 | | $+V_{REF}$ / 2GAIN | |
| $V_{ID}$ | Differential input voltage range for specified performance[2] | SD24REFON = 1 | SD24GAINx = 1 | | | ±500 | | mV |
| | | | SD24GAINx = 2 | | | ±250 | | |
| | | | SD24GAINx = 4 | | | ±125 | | |
| | | | SD24GAINx = 8 | | | ±62 | | |
| | | | SD24GAINx = 16 | | | ±31 | | |
| | | | SD24GAINx = 32 | | | ±15 | | |
| $Z_I$ | Input impedance (one input pin to AVSS) | $f_{SD24}$ = 1 MHz | SD24GAINx = 1 | 3 V | | 200 | | kΩ |
| | | | SD24GAINx = 32 | | | 75 | | |
| $Z_{ID}$ | Differential input impedance (IN+ to IN-) | $f_{SD24}$ = 1 MHz | SD24GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | | SD24GAINx = 32 | | 100 | 150 | | |
| $V_I$ | Absolute input voltage range | | | | AVSS - 1 | | AVCC | V |
| $V_{IC}$ | Common-mode input voltage range | | | | AVSS - 1 | | AVCC | V |

(1) All parameters pertain to each SD24_A channel.
(2) The full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$. If VREF is sourced externally, the analog input range should not exceed 80% of $V_{FSR+}$ or $V_{FSR-}$; that is, $V_{ID} = 0.8\ V_{FSR-}$ to $0.8\ V_{FSR+}$. If VREF is sourced internally, the given $V_{ID}$ ranges apply.

## SD24_A, Performance ($f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFON = 1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| G | Nominal gain | SD24GAINx = 1 | 3 V | | 1 | | |
| | | SD24GAINx = 2 | | | 1.96 | | |
| | | SD24GAINx = 4 | | | 3.86 | | |
| | | SD24GAINx = 8 | | | 7.62 | | |
| | | SD24GAINx = 16 | | | 15.04 | | |
| | | SD24GAINx = 32 | | | 28.35 | | |
| $E_{OS}$ | Offset error | SD24GAINx = 1 | 3 V | | | ±0.2 | %FSR |
| | | SD24GAINx = 32 | | | | ±1.5 | |
| ΔEOS/ΔT | Offset error temperature coefficient | SD24GAINx = 1 | 3 V | | ±4 | ±20 | ppm FSR/°C |
| | | SD24GAINx = 32 | | | ±20 | ±100 | |
| CMRR | Common-mode rejection ratio | SD24GAINx = 1, Common-mode input signal: $V_{ID}$ = 500 mV, $f_{IN}$ = 50 Hz, 100 Hz | 3 V | | >90 | | dB |
| | | SD24GAINx = 32, Common-mode input signal: $V_{ID}$ = 16 mV, $f_{IN}$ = 50 Hz, 100 Hz | | | >75 | | |
| AC PSRR | AC power supply rejection ratio | SD24GAINx = 1, $V_{CC}$ = 3 V ± 100 mV, $f_{VCC}$ = 50 Hz | 3 V | | >80 | | dB |
| XT | Crosstalk | SD24GAINx = 1, $V_{ID}$ = 500 mV, $f_{IN}$ = 50 Hz, 100 Hz | 3 V | | <-100 | | dB |

## SD24_A, Temperature Sensor and Built-In $V_{CC}$ Sense

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $TC_{Sensor}$ | Sensor temperature coefficient | | | 1.18 | 1.32 | 1.46 | mV/°C |
| $V_{Offset,sensor}$ | Sensor offset voltage | | | -100 | | 100 | mV |
| $V_{Sensor}$ | Sensor output voltage (1) (2) | Temperature sensor voltage at $T_A$ = 85°C | 3 V | 420 | 475 | 515 | mV |
| | | Temperature sensor voltage at $T_A$ = 30°C | | 350 | 402 | 442 | |
| $V_{CC,Sense}$ | $V_{CC}$ divider at input 5 | $f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFON = 1 | | | $V_{CC}$/1 1 | | V |
| $R_{Source,VCC}$ | Source resistance of $V_{CC}$ divider at input 5 | | | | 20 | | kΩ |

(1) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV]
(2) Results based on characterization and/or production test, not $TC_{Sensor}$ or $V_{Offset,sensor}$. Measured with $f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFON = 1.

## SD24_A, Built-In Voltage Reference

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF}$ | Internal reference voltage | SD24REFON = 1, SD24VMIDON = 0 | 3 V | 1.14 | 1.2 | 1.26 | V |
| $I_{REF}$ | Reference supply current | SD24REFON = 1, SD24VMIDON = 0 | 3 V | | 200 | 320 | µA |
| TC | Temperature coefficient | SD24REFON = 1, SD24VMIDON = 0 (1) | 3 V | | 18 | 50 | ppm/°C |
| $C_{REF}$ | $V_{REF}$ load capacitance | SD24REFON = 1, SD24VMIDON = 0 (2) | | | 100 | | nF |
| $I_{LOAD}$ | $V_{REF(I)}$ maximum load current | SD24REFON = 1, SD24VMIDON = 0 | 3 V | | | ±200 | nA |
| $t_{ON}$ | Turn-on time | SD24REFON = 0→1, SD24VMIDON = 0, $C_{REF}$ = 100nF | 3 V | | 5 | | ms |
| DC PSR | DC power supply rejection $\Delta V_{REF}/\Delta V_{CC}$ | SD24REFON = 1, SD24VMIDON = 0, $V_{CC}$ = 2.5 V to 3.6 V | | | 100 | | µV/V |

(1) Calculated using the box method: (MAX(-40...85°C) - MIN(-40...85°C)) / MIN(-40...85°C) / (85°C - (-40°C))
(2) There is no capacitance required on $V_{REF}$. However, a capacitance of at least 100 nF is recommended to reduce any reference voltage noise.

## SD24_A, Reference Output Buffer

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF,BUF}$ | Reference buffer output voltage | SD24REFON = 1, SD24VMIDON = 1 | 3 V | | 1.2 | | V |
| $I_{REF,BUF}$ | Reference supply + reference output buffer quiescent current | SD24REFON = 1, SD24VMIDON = 1 | 3 V | | 430 | 650 | µA |
| $C_{REF(O)}$ | Required load capacitance on VREF | SD24REFON = 1, SD24VMIDON = 1 | | 470 | | | nF |
| $I_{LOAD,Max}$ | Maximum load current on VREF | SD24REFON = 1, SD24VMIDON = 1 | 3 V | | | ±1 | mA |
| | Maximum voltage variation vs load current | $\|I_{LOAD}\|$ = 0 to 1 mA | 3 V | -15 | | +15 | mV |
| $t_{ON}$ | Turn-on time | SD24REFON = 0→1, SD24VMIDON = 0→1, $C_{REF}$ = 470 nF | 3 V | | 100 | | µs |

## SD24_A, External Reference Input

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF(I)}$ | Input voltage range | SD24REFON = 0 | 3 V | 1.0 | 1.25 | 1.5 | V |
| $I_{REF(I)}$ | Input current | SD24REFON = 0 | 3 V | | | 50 | nA |

## USART0

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{USART}$ | USART clock frequency | | | | 8 | MHz |
| $t_{(τ)}$ | USART0: deglitch time(1) | $V_{CC}$ = 3 V, SYNC = 0, UART mode | 150 | 280 | 500 | ns |

(1) The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(τ)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(τ)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

## Timer_A3

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A3 clock frequency | SMCLK, Duty cycle = 50% ± 10% | | | $f_{SYSTEM}$ | | MHz |
| $t_{TA,cap}$ | Timer_A3, capture timing | TA0, TA1 | 3 V | 20 | | | ns |

## Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | | 2.2 | | 3.6 | V |
| $f_{FTG}$ | Flash timing generator frequency | | | 257 | | 476 | kHz |
| $I_{PGM}$ | Supply current from $V_{CC}$ during program | | 2.2 V/3.6 V | | 1 | 5 | mA |
| $I_{ERASE}$ | Supply current from $V_{CC}$ during erase | | 2.2 V/3.6 V | | 1 | 7 | mA |
| $t_{CPT}$ | Cumulative program time(1) | | 2.2 V/3.6 V | | | 10 | ms |
| $t_{CMErase}$ | Cumulative mass erase time | | 2.2 V/3.6 V | 20 | | | ms |
| | Program/erase endurance | | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | | 100 | | | years |
| $t_{Word}$ | Word or byte program time | (2) | | | 30 | | $t_{FTG}$ |
| $t_{Block,\ 0}$ | Block program time for first byte or word | (2) | | | 25 | | $t_{FTG}$ |
| $t_{Block,\ 1-63}$ | Block program time for each additional byte or word | (2) | | | 18 | | $t_{FTG}$ |
| $t_{Block,\ End}$ | Block program end-sequence wait time | (2) | | | 6 | | $t_{FTG}$ |
| $t_{Mass\ Erase}$ | Mass erase time | (2) | | | 10593 | | $t_{FTG}$ |
| $t_{Seg\ Erase}$ | Segment erase time | (2) | | | 4819 | | $t_{FTG}$ |

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine ($t_{FTG}$ = 1 / $f_{FTG}$).

## RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{(RAMh)}$ | RAM retention supply voltage (1) | CPU halted | 1.6 | | V |

(1) This parameter defines the minimum supply voltage $V_{CC}$ when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

## JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | | 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse length | | 3 V | 0.025 | | 15 | µs |
| $t_{SBW,En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1)) | | 3 V | | | 1 | µs |
| $t_{SBW,Ret}$ | Spy-Bi-Wire return to normal operation time | | 3 V | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency(2) | | 3 V | 0 | | 10 | MHz |
| $R_{Internal}$ | Internal pulldown resistance on TEST | | 3 V | 25 | 60 | 90 | kΩ |

(1) Tools accessing the Spy-Bi-Wire interface must wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

## JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC(FB)}$ | Supply voltage during fuse-blow condition | $T_A$ = 25°C | 2.5 | | V |
| $V_{FB}$ | Voltage level on TEST for fuse blow | | 6 | 7 | V |
| $I_{FB}$ | Supply current into TEST during fuse blow | | | 100 | mA |
| $t_{FB}$ | Time to blow fuse | | | 1 | ms |

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, or emulation feature is possible, and JTAG is switched to bypass mode.

## APPLICATION INFORMATION

### Port P1 Pin Schematic: P1.0 Input/Output With Schmitt Trigger

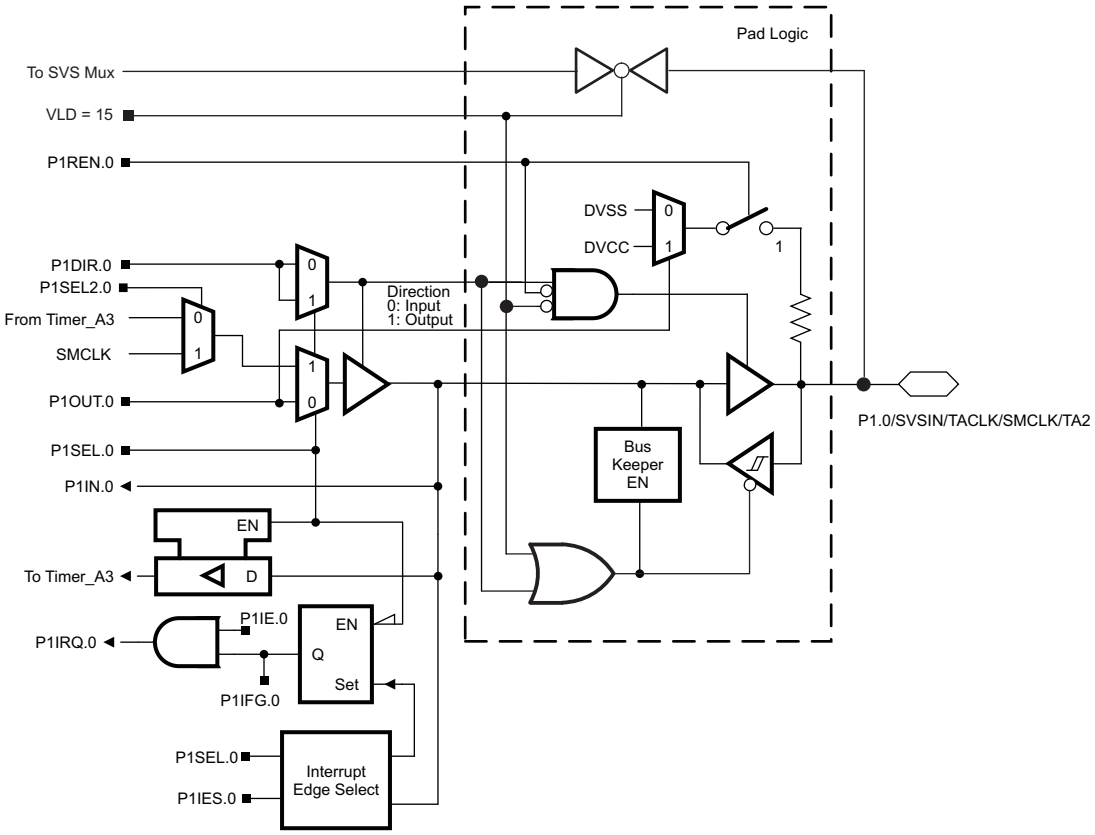
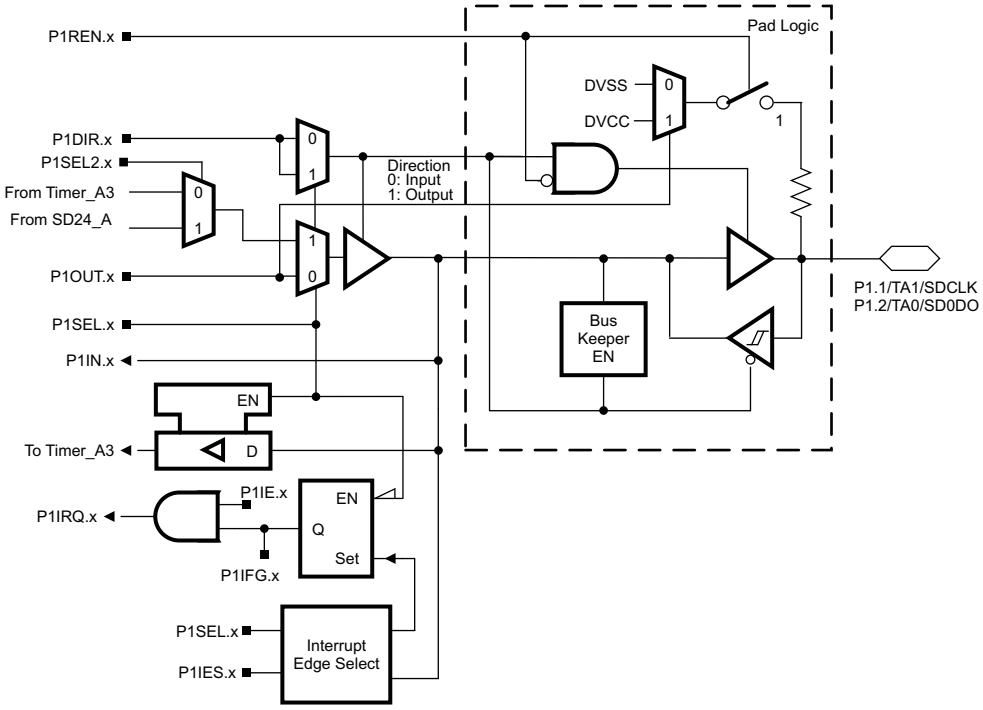



**Table 17. Port P1 (P1.0) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x |
| P1.0/SVSIN/TACLK/SMCLK/TA2 | 0 | P1.0 (I/O) | I: 0, O: 1 | 0 | X |
| | | SVSIN (VLD = 15) | X | X | X |
| | | Timer_A3.TACLK | 0 | 1 | 0 |
| | | SMCLK | 1 | 1 | 1 |
| | | Timer_A3.TA2 | 1 | 1 | 0 |

(1) X = don't care

## Port P1 Pin Schematic: P1.1 and P1.2 Input/Output With Schmitt Trigger

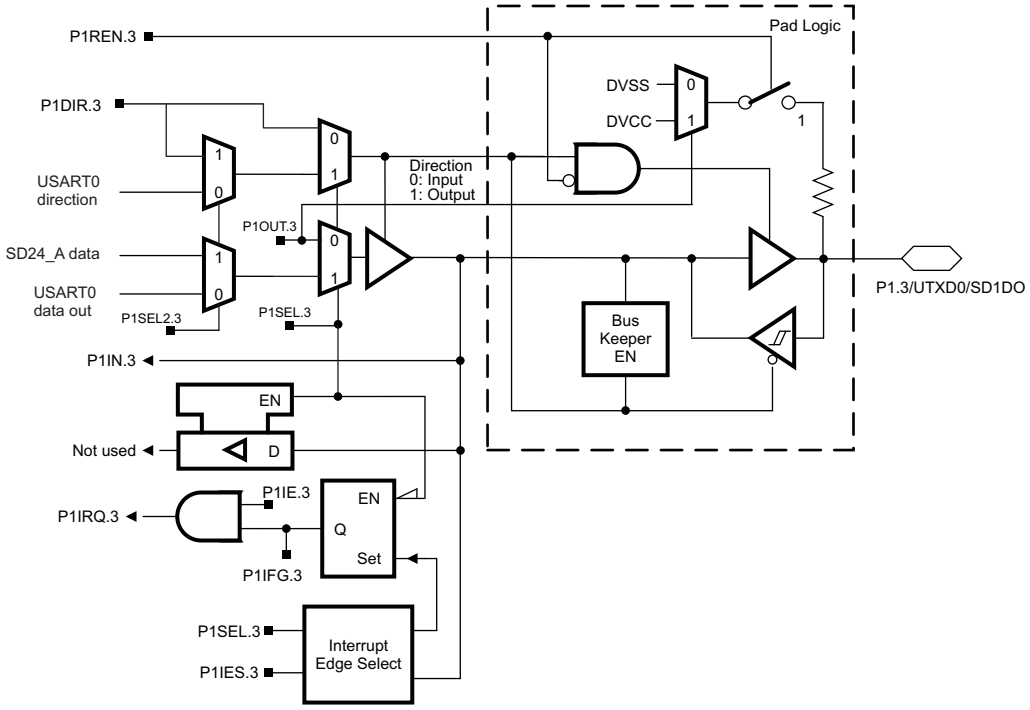



### Table 18. Port P1 (P1.1 and P1.2) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNAL (1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x |
| P1.1/TA1/SDCLK | 1 | P1.1 (I/O) | I: 0, O: 1 | 0 | X |
| | | Timer_A3.CCI1A and CCI1B | 0 | 1 | 0 |
| | | Timer_A3.TA1 | 1 | 1 | 0 |
| | | SDCLK | 1 | 1 | 1 |
| P1.2/TA0/SD0DO | 2 | P1.2 (I/O) | I: 0, O: 1 | 0 | X |
| | | Timer_A3.CCI0A and CCI0B | 0 | 1 | 0 |
| | | Timer_A3.TA0 | 1 | 1 | 0 |
| | | SD0DO | 1 | 1 | 1 |

(1) X = don't care

## Port P1 Pin Schematic: P1.3 Input/Output With Schmitt Trigger




### Table 19. Port P1 (P1.3) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x |
| P1.3/UTXD0/SD1DO | 3 | P1.3 (I/O) | I: 0, O: 1 | 0 | X |
| | | UTXD0 | X | 1 | 0 |
| | | SD1DO | 1 | 1 | 1 |

(1) X = don't care

## Port P1 Pin Schematic: P1.4 Input/Output With Schmitt Trigger

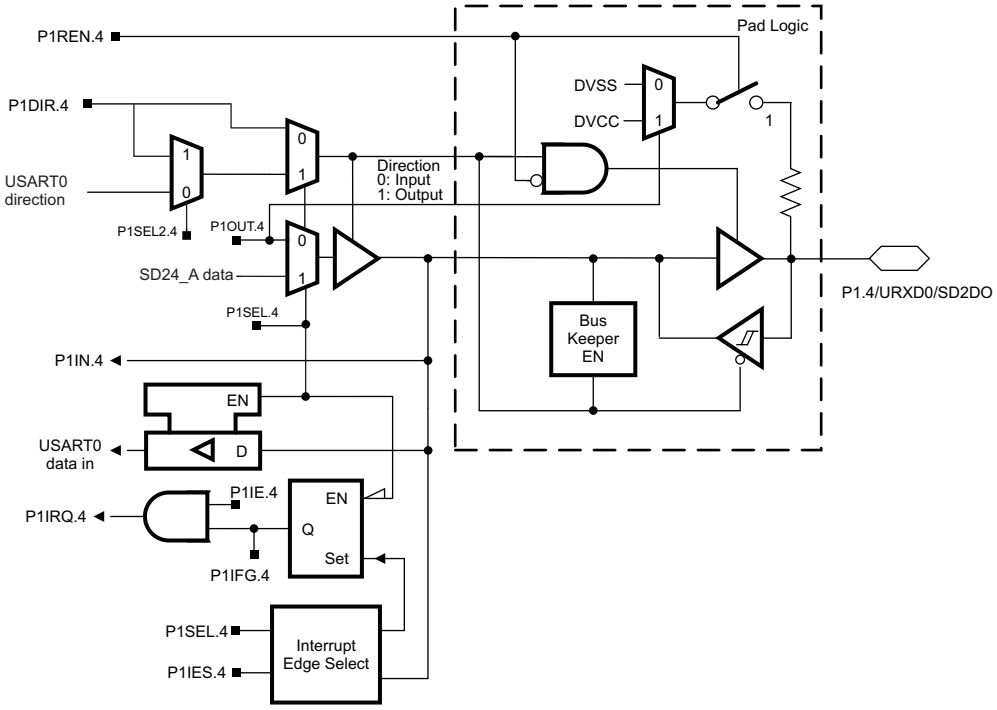
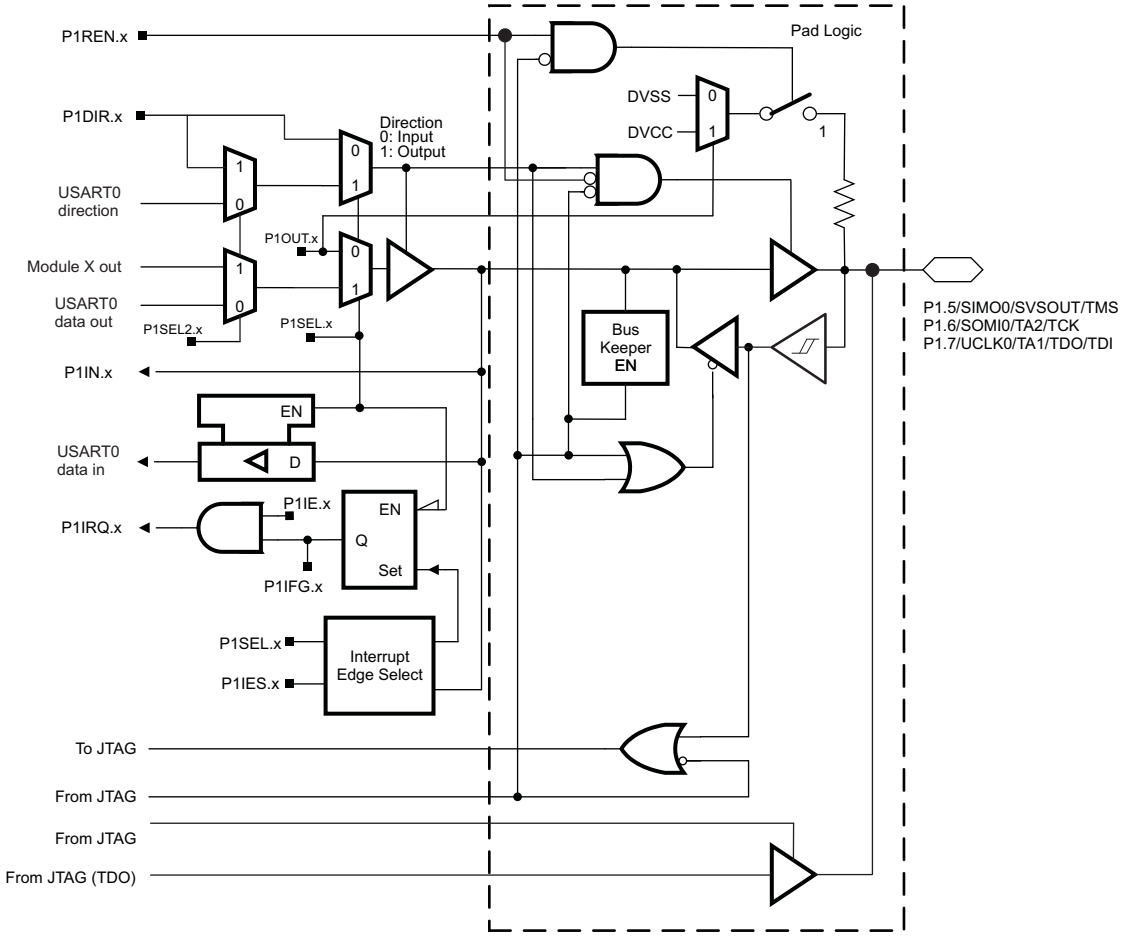



**Table 20. Port P1 (P1.4) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x |
| P1.4/URXD0/SD2DO | 4 | P1.4 (I/O) | I: 0, O: 1 | 0 | X |
| | | URXD0 | X | 1 | 0 |
| | | SD2DO | 1 | 1 | 1 |

(1) X = don't care

## Port P1 Pin Schematic: P1.5 to P1.7 Input/Output With Schmitt Trigger

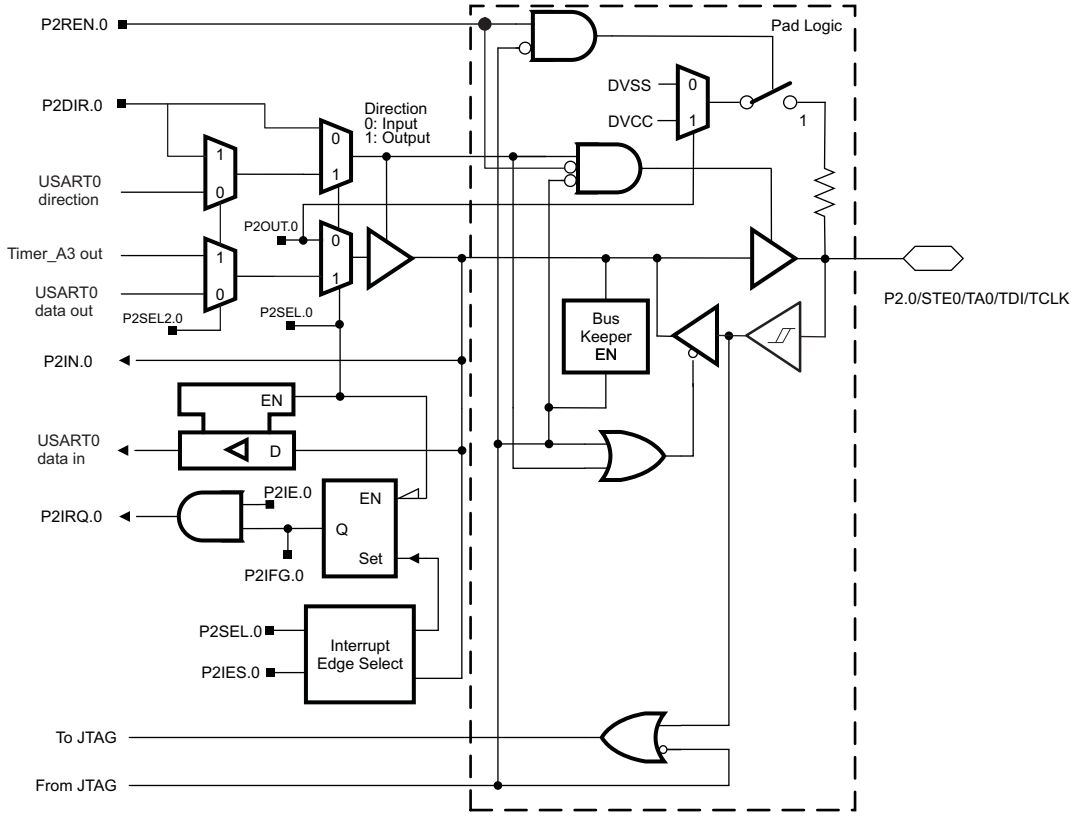



### Table 21. Port P1 (P1.5 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | | |
|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | JTAG Mode[2] |
| P1.5/SIMO0/SVSOUT/TMS | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SIMO0 | X | 1 | 0 | 0 |
| | | SVSOUT | 1 | 1 | 1 | 0 |
| | | TMS | X | X | X | 1 |
| P1.6/SOMI0/TA2/TCK | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SOMI0 | X | 1 | 0 | 0 |
| | | Timer_A3.TA2 | 1 | 1 | 1 | 0 |
| | | TCK | X | X | X | 1 |
| P1.7/UCLK0/TA1/TDO/TDI | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCLK0 | X | 1 | 0 | 0 |
| | | Timer_A3.TA1 | 1 | 1 | 1 | 0 |
| | | TDO/TDI | X | X | X | 1 |

(1) X = don't care
(2) JTAG Mode is not a register bit but signal generated internally when 4-wire JTAG option is selected in IDE

## Port P2 Pin Schematic: P2.0 Input/Output With Schmitt Trigger

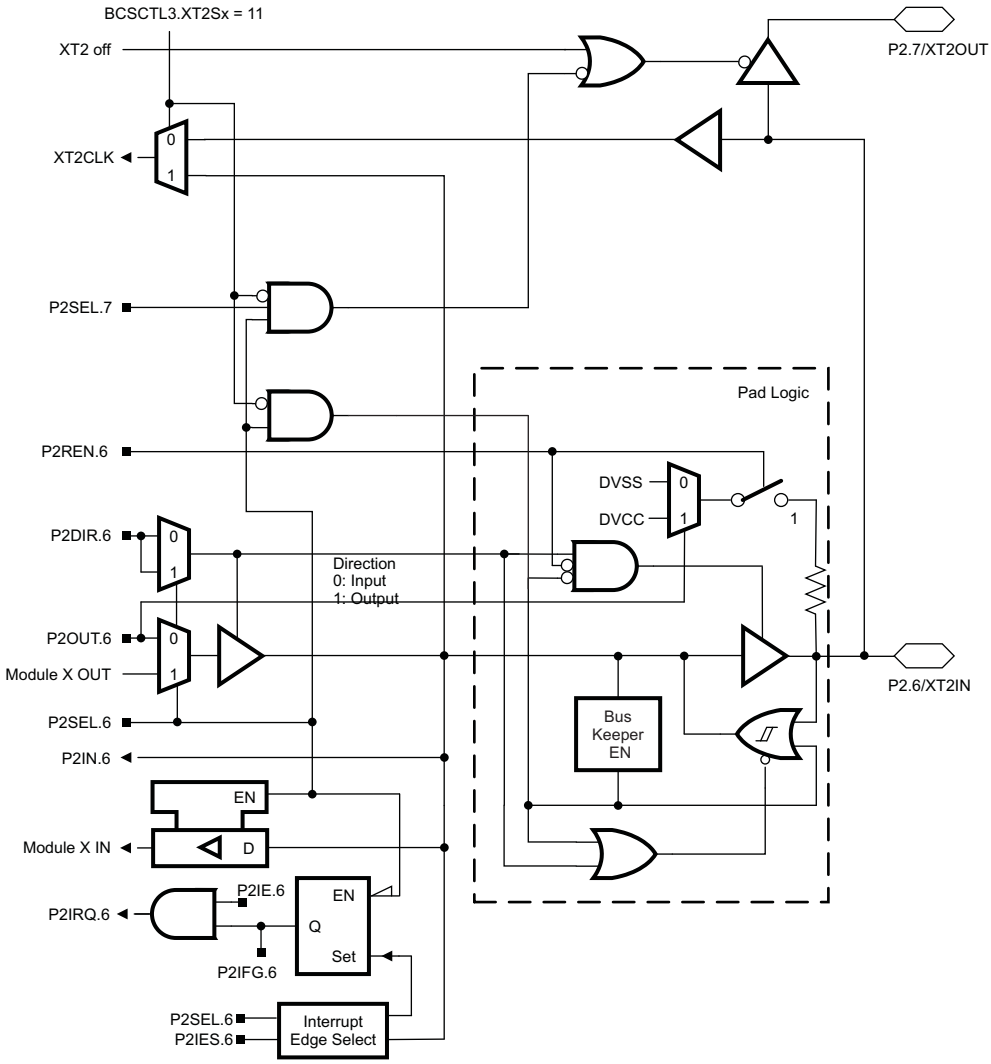



### Table 22. Port P2 (P2.0) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2SEL2.x | JTAG Mode[2] |
| P2.0/STE0/TA0/TDI/TCLK | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | STE0 | X | 1 | 0 | 0 |
| | | Timer_A3.TA0 | 1 | 1 | 1 | 0 |
| | | TDI/TCLK | X | X | X | 1 |

(1) X = don't care
(2) JTAG Mode is not a register bit but signal generated internally when 4-wire JTAG option is selected in IDE

## Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger




### Table 23. Port P2 (P2.6) Pin Functions

| Pin Name (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P2DIR.6 | P2SEL.6 |
| P2.6/XT2IN | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 |
| | | XT2IN (default) | 0 | 1 |

## Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

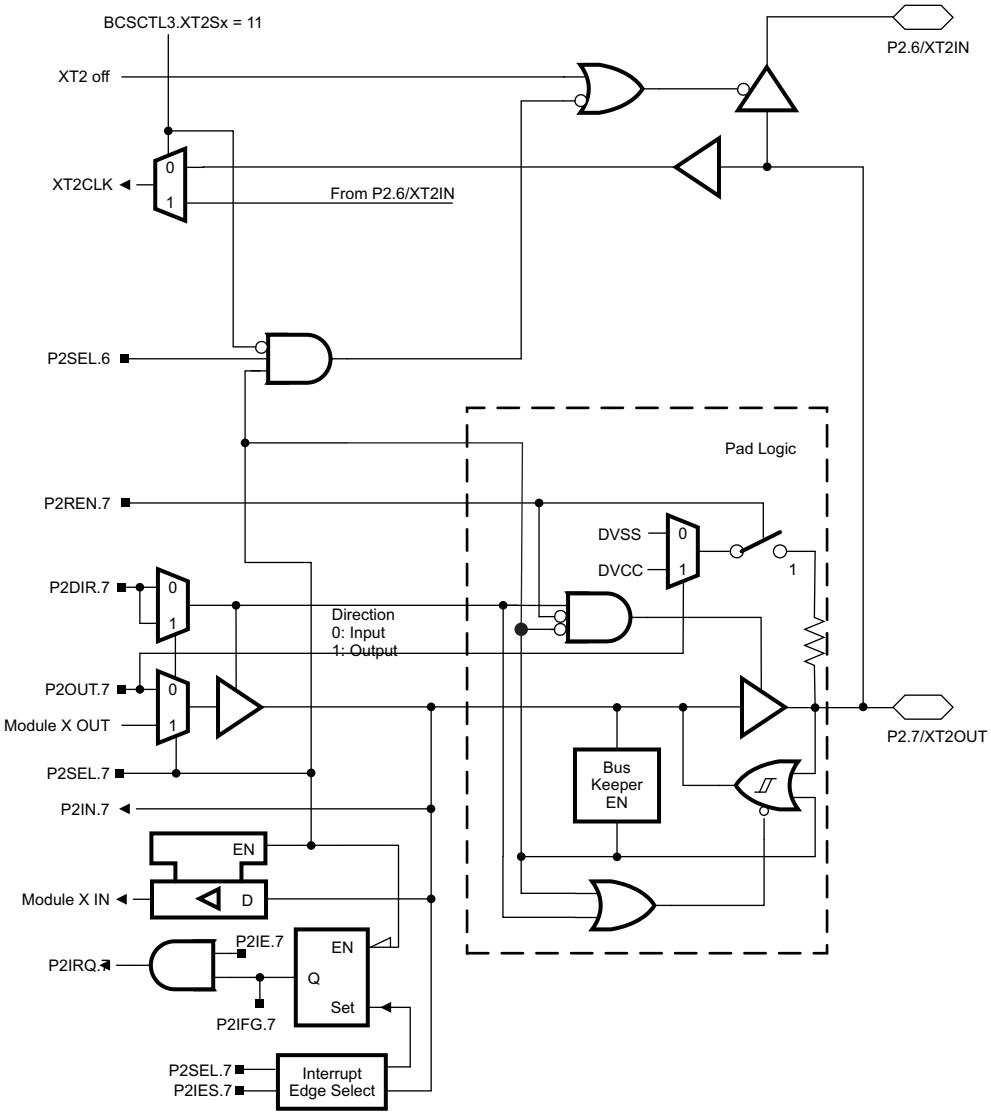



**Table 24. Port P2 (P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P2DIR.7 | P2SEL.7 |
| P2.7/XT2OUT | 7 | P2.7 (I/O) | I: 0, O: 1 | 0 |
| | | XT2OUT (default) | 0 | 1 |

## JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, $I_{TF}$ , of 1 mA at 3 V or 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR, the fuse check mode has the potential to be activated.

The fuse check current flow only when the fuse check mode is active and the TMS pin is in a low state (see Figure 17). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

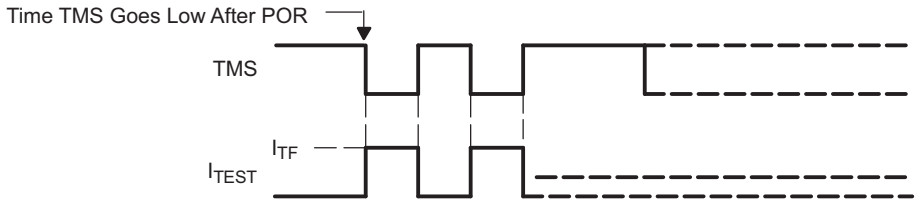



**Figure 17. Fuse Check Mode Current**

**NOTE**

The CODE and RAM data protection is ensured if the JTAG fuse is blown.

## REVISION HISTORY

| REVISION | COMMENTS |
|---|---|
| SLAS701 | Product Preview release |
| SLAS701A | Production Data release |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430AFE221IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE221IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE222IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE222IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE223IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE223IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE231IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE231IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE232IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE232IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE233IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE233IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE251IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE251IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE252IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE252IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430AFE253IPW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

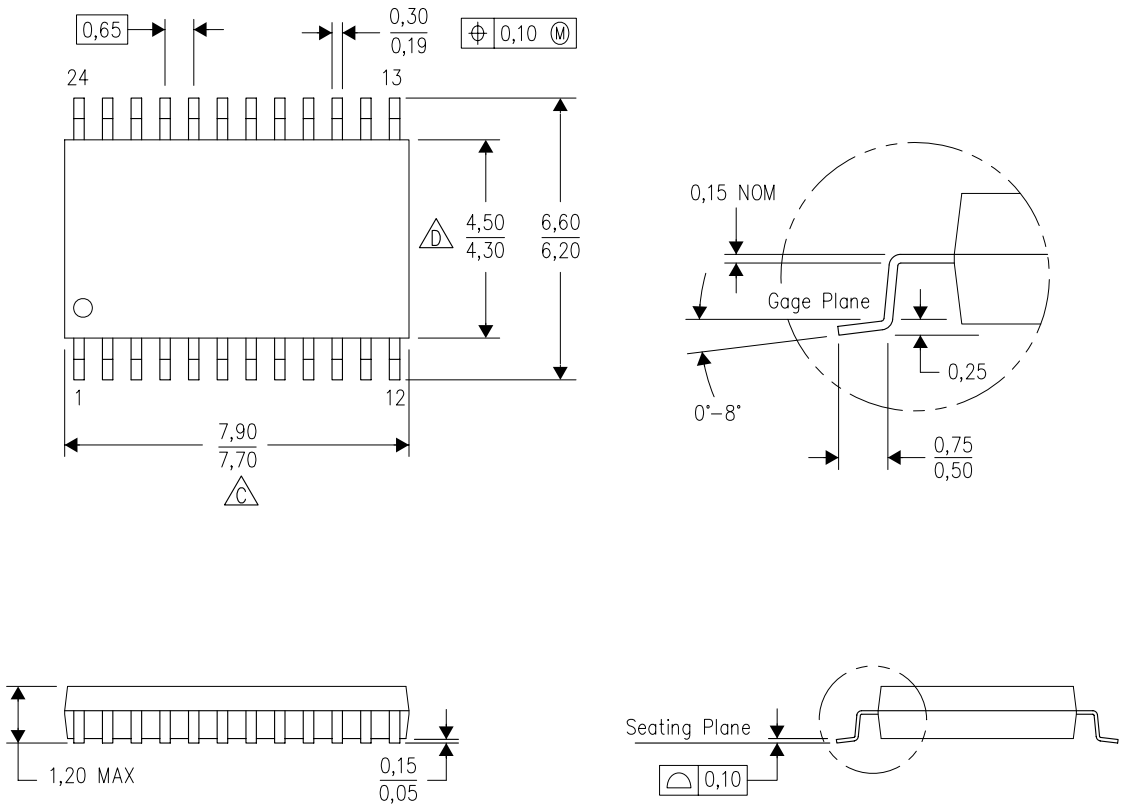
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430AFE253IPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

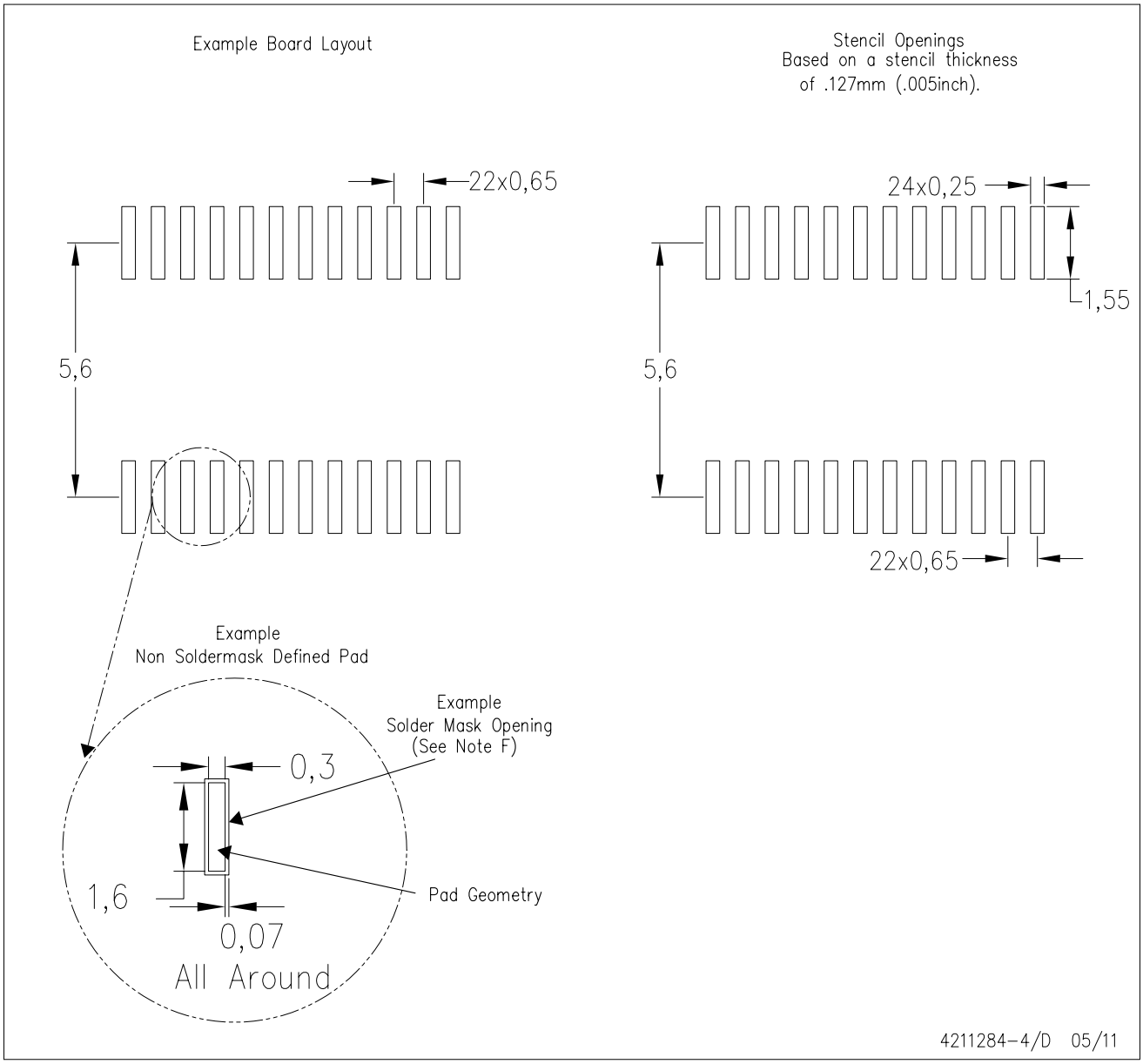
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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