MSP430F22x2 Device Erratasheet

1 Current Version

Devices	Rev:	BCL12	CPU19	FLASH24	FLASH27	PORT10	TA12	TA16	TAB22	TB2	TB16	USCI20	USCI21	USCI22	USCI23	USCI24	USCI25	USCI26	USCI27	XOSC5	XOSC8
MSP430F2232	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

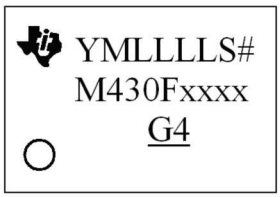
Note: See Appendix A for prior revisions.

✓ The checkmark means that the issue is present in that revision.

2 Package Markings

DA38

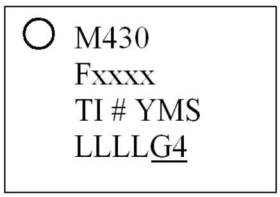
TSSOP (DA), 38 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RHA40

QFN (RHA), 40 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

3 Detailed Bug Description

BCL12 *Basic Clock Module*

Function Switching RSEL can cause DCO dead time

Description After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 µs. In some instances, the DCO may completely stop, requiring a power cycle.

Workaround

- When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

- When switching RSEL from <12 to >13, ensure that the maximum system frequency is not exceeded during the transition. This can be achieved by clearing the DCO bits first (DCOCTL control register, bits 7–5), then increasing the RSEL value, and finally applying the target frequency DCO bit values. For more details, see the examples in the "TLV Structure" chapter in the *MSP430F2xx Family User's Guide* (SLAU144).

CPU19 *CPU Module*

Function CPUOFF can change register values

Description If a CPUOFF command is followed by an instruction with an indirect addressed operand (for example, `mov @R8, R9, and RET`), an unintentional register-read operation can occur during the wakeup of the CPU. If the unintentional read occurs to a read-sensitive register (for example, UCB0RXBUF or TAIV), which changes its value or the value of other registers (IFGs), the bug leads to lost interrupts or wrong register read values.

Workaround Insert a NOP instruction after each CPUOFF instruction.

FLASH24 *Flash Module*

Function Write or erase emergency exit can cause failures

Description When a flash write or erase is abruptly terminated, any further reliable reads by the flash controller are not ensured. The abrupt termination can be the result of one the following events:

- The flash controller clock is configured to be SMCLK sourced by an external crystal. An oscillator fault occurs, thus stopping this clock abruptly.
- The Emergency Exit bit (EMEX in FCTL3), when set, forces a write or an erase operation to be terminated before normal completion.
- The Enable Emergency Interrupt Exit bit (EEIEX in FCTL1), when set with GIE = 1, can lead to an interrupt, causing an emergency exit during a flash operation.

Workaround

- Do not use SMCLK as the source for the flash controller clock if it is sourced from an external crystal.
- After setting EMEX = 1, wait for a sufficient amount of time before flash is accessed again.
- No workaround. Do not use EEIEX bit.

FLASH27 *Flash Module*

Function EEI feature can disrupt segment erase

Description When a flash segment erase operation is active with EEI feature selected (EEI = 1 in FLCTL1) and GIE = 0, the following can occur:

An interrupt event causes the flash erase to be stopped, and the flash controller expects an RETI to resume the erase. Because GIE = 0, interrupts are not serviced and RETI never happens.

Workaround

- Do not set bit EEI = 1 when GIE = 0.

  or
- Force an RETI instruction during the erase operation during the check for BUSY=1 (FCLTL3).

Example

```
            MOV   R5, 0(R5)       ; Dummy write, erase segment
LOOP:       BIT   #BUSY, &FCTL3   ; test busy bit
            JMP   SUB_RETI        ; Force RETI instruction
            JNZ   LOOP            ; loop while BUSY=1

SUB_RETI:   PUSH  SR
            RETI
```

PORT10 *Digital I/O Module*

Function Pullup/pulldown resistor selection when module pin function is selected

Description When the pullup/pulldown resistor for a certain port pin is enabled (PxREN.y = 1) and the module port pin function is selected (PxSEL.y = 1), the pullup/pulldown resistor configuration of this pin is controlled by the respective module output signal (Module X OUT) instead of the port output register (PxOUT.y).

Workaround None. Do not set PxSEL.y and PxREN.y at the same time.

TA12 *Timer_A Module*

Function Interrupt is lost (slow ACLK)

Description Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TA16 *Timer_A Module*

Function First increment of TAR erroneous when IDx > 00

Description The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround None

TAB22 *Timer_A/Timer_B Module*

Function Timer_A/B register modification after Watchdog Timer PUC

Description Unwanted modification of the Timer_A/B registers TACTL and TAIV can occur when a PUC is generated by the Watchdog Timer (WDT) in watchdog mode and any Timer_A/B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/B does not need to be running).

Workaround Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

```
MOV.W #VAL, &TBCTL
```

Where, VAL = 0, if Timer is not used in application; otherwise, user defined per desired function.

TB2 *Timer_B Module*

Function Interrupt is lost (slow ACLK)

Description Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if TBR = CCRx + 1). This interrupt is lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TB16 *Timer_B Module*

Function First increment of TBR erroneous when IDx > 00

Description The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

Workaround None

USCI20 *USCI Module*

Function I^2C mode multi-master transmitter issue

Description When configured for I^2C master-transmitter mode and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following conditions are true:

1. Two masters are generating SCL.
   and
2. The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA.
   and
3. The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line is released.
   and
4. The transmit buffer has not been loaded before the other master continues communication by driving SCL low.

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI interferes with the current bus activity and may cause unpredictable bus behavior.

Workaround

- Ensure that slave does not stretch the SCL low phase of an ACK period.
  or
- Ensure that the transmit buffer is loaded in time.
  or
- Do not use the multi-master transmitter mode.

USCI21 *USCI Module*

Function UART IrDA receiver mode

Description IrDA reception does not function correctly at certain baud rates. This occurs only when the IrDA receive filter via the UCAxIRRCTL register is enabled and the USCI source clock (BRCLK) is higher than 6 MHz.

Workaround

1. Set the filter length (UCIRRXFLx in UCAxIRRCTL) to the maximum value 0x3F to achieve proper functionality.
2. Reduce the frequency of the USCI source clock (BRCLK) to the IrDA module to be less than 6 MHz.

USCI22 *USCI Module*

Function I^2C master receiver with 10-bit slave addressing

Description Unexpected behavior of the USCI_B can occur when configured in I^2C master receive mode with 10-bit slave addressing under the following conditions:

1. The USCI sends first byte of slave address, the slave sends an ACK and when second address byte is sent, the slave sends a NACK.
2. Master sends a repeat start condition (if UCTXSTT = 1).
3. The first address byte following the repeated start is acknowledged.

However, the second address byte is not sent, instead the master incorrectly starts to receive data and sets UCBxRXIFG = 1.

Workaround Do not use a repeated start condition; instead, set the stop condition UCTXSTP = 1 in the NACK ISR prior to the following start condition (USTXSTT = 1).

USCI23 *USCI Module*

Function UART transmit mode with automatic baud rate detection

Description Erroneous behavior of the USCI_A can occur when configured in UART transmit mode with automatic baud rate detection. During transmission if a "Transmit break" is initiated (UCTXBRK = 1), the USCI_A does not deliver a stop bit of logic high; instead, it sends a logic low during the subsequent synch period.

Workaround

- Follow user's guide instructions for transmitting a break/synch field following UCSWRST = 1.

  or
- Set UCTXBRK = 1 before an active transmission; that is, check for bit UCBUSY = 0 and then set UCTXBRK = 1.

USCI24 *USCI Module*

Function Incorrect baud rate information during UART automatic baud rate detection mode

Description Erroneous behavior of the USCI_A can occur when configured in UART mode with automatic baud rate detection. After automatic baud rate measurement is complete, the UART updates UCAxBR0 and UCAxBR1. Under oversampling mode (UCOS16 = 1), for baud rates that should result in UCAxBRx = 0x0002, the UART incorrectly reports it as UCAxBRx = 0x5555.

Workaround When break/synch is detected following the automatic baud rate detection, the flag UCBRK flag is set to 1. Check if UCAxBRx = 0x5555 and correct it to 0x0002.

USCI25 *USCI Module*

Function TXIFG is not reset when NACK is received in I^2C mode

Description When the USCI_B module is configured as an I^2C master transmitter, the TXIFG is not reset after a NACK is received if the master is configured to send a restart (UCTXSTT = 1 and UCTXSTP = 0).

Workaround Reset TXIFG in software within the NACKIFG interrupt service routine.

USCI26 *USCI Module*

Function t_{buf} parameter violation in I^2C multi-master mode

Description In multi-master I^2C systems, the timing parameter t_{buf} (bus free time between a stop condition and the following start) is not ensured to match the I^2C specification of 4.7 µs in standard mode and 1.3 µs in fast mode. If the UCTXSTT bit is set during a running I^2C transaction, the USCI module waits and issues the start condition on bus release, causing the violation to occur.

NOTE: It is recommended to check if UCBBUSY bit is cleared before setting UCTXSTT = 1.

Workaround None

USCI27 — *USCI Module*

Function

Timing of USCI I²C interrupts may cause device reset due to automatic clear of an IFG.

Description

When certain USCI I²C interrupt flags (IFG) are set and an automatic flag-clearing event on the I²C bus occurs, the program counter may become corrupted. This happens only when the IFG is cleared within a critical time window (~6 CPU clock cycles) after a USCI interrupt request occurs and before the interrupt servicing is initiated. The affected interrupts are UCBxTXIFG, UCSTPIFG, UCSTTIFG and UCNACKIFG.

The automatic flag-clearing scenarios are described in the following situations:

- A pending UCBxTXIFG interrupt request is cleared on the falling SCL clock edge following a NACK.
- A pending UCSTPIFG, UCSTTIFG, or UCNACKIFG interrupt request is cleared by a following Start condition.

Workaround

- Polling the affected flags instead of enabling the interrupts
  or
- Ensuring the above mentioned flag-clearing events occur after a time delay of 6 CPU clock cycles has elapsed since the interrupt request occurred and was accepted.

XOSC5 — *LFXT1 Module*

Function

LF crystal failures may not be properly detected by the oscillator fault circuitry

Description

The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU; that is, OFIFG is not set.

Workaround

None

XOSC8 — *LFXT1 Module*

Function

ACLK failure when crystal ESR is below 40 kΩ

Description

When ACLK is sourced by a low-frequency crystal with an ESR below 40 kΩ, the duty cycle of ACLK may fall below the specification; the OFIFG may become set or, in some instances, ACLK may stop completely.

Workaround

See the application report *XOSC8 Guidance* (SLAA423) for information regarding working with this erratum.

Appendix A Prior Versions

Devices	Rev:	BCL12	BCL13	CPU14	CPU19	FLASH21	FLASH22	FLASH24	FLASH27	JTAG13	JTAG14	PORT10	TA12	TA16	TAB22	TB2	TB16	USCI16	USCI20	USCI21
MSP430F2232	G	✓			✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓		✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	G	✓			✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓		✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	G	✓			✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓		✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	G	✓			✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓		✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	G	✓			✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓		✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	G	✓			✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓		✓			✓	✓			✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Devices	Rev:	USCI22	USCI23	USCI24	USCI25	USCI26	USCI27	XOSC5	XOSC8
MSP430F2232	G	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	G	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	G	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	G	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	G	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	G	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓

✓ The checkmark means that the issue is present in that revision.

A.1 Detailed Bug Description

BCL13 — *Basic Clock Module*

Function Exiting reset state with slow V_{CC} rise time

Description When subject to very slow V_{CC} rise times, the device may enter a state in which the DCO does not oscillate. No JTAG access or program execution is possible, and the device remains in the reset state until the supply voltage is disconnected.

Workaround Apply a V_{CC} power-on ramp ≥10 V/s under all power-on/power-cycle scenarios.

FLASH21 — *Flash Module*

Function Information memory read data corrupted

Description Flash addresses between 0x1080 and 0x10FF (information memory) might not be read correctly. Supply voltages and addressing mode affect the read value.

Workaround None

FLASH22 — *Flash Module*

Function Flash controller may prevent correct LPM entry

Description When ACLK (or SMCLK) is used as the flash controller clock source and this clock source is deactivated due to a low-power mode entry while a flash erase or write operating is pending, the flash controller keeps ACLK (or SMCLK) active even after the flash operation has been completed. This results in an incorrect LPM entry and increased current consumption. Note that this issue can only occur when the flash operation and the low-power mode entry are initiated from code located in RAM.

Workaround Do not enter low-power modes while flash erase or write operations are active. Wait for the operation to complete before entering a low-power mode.

JTAG13 — *JTAG Module*

Function PSA checksum generation fails

Description PSA checksum generation gives a wrong result when data_psa is executed during test clock low phase and the last address of flash information memory addresses 0x107E or 0x10FE are part of the calculation.

Workaround Calculate PSA sum when test clock is at high level.

JTAG14 *JTAG Module*

Function Releasing JTAG control can corrupt CPU registers during debug

Description During a debug session, on rare occasions, the CPU register contents can be corrupted when JTAG control is released by the debugger. This behavior is exhibited during, but not limited to, the use of the "Use Virtual Breakpoints" and "Force Single Stepping" features in the IAR Embedded Workbench software. This bug does not affect normal device and application operation, such as starting a device out of POR and executing application code.

For the bug to occur, both of the following conditions must be true:

1. The CPU (MCLK) is sourced by the DCO.
2. The "External Resistor (Rosc)" feature of the DCO is not used.

Workaround Use an external crystal or a digital high-speed clock source connected to the LFXT1 oscillator to source the CPU (MCLK) during a debug session. Alternatively, use the on-chip DCO in the "External Resistor (Rosc)" configuration. Note that, in this case, an external resistor connected to the device Rosc pin is mandatory and that the factory-programmed DCO calibration constants cannot be applied directly.

USCI16 *USCI Module*

Function UART/IrDA mode lost characters

Description When configured for UART/IrDA mode, the USCI baud rate generator may halt operation under the following conditions:

- IrDA mode: Repeated invalid start bits on the receive line

  or
- UART/IrDA modes: Positive pulse on the receive line during break character reception inside the stop-bit time slot (the second stop-bit time slot if UCSPB = 1) with a pulse width that passes the deglitch filter but is shorter than one-half of a bit time.

After halting, additional characters are ignored. Transmit functionality is not affected.

Workaround Check the UCBUSY flag status periodically in software. If the flag is set and no character has been received in the expected time, reset the USCI module in software. To reset the USCI module, toggle UCSWRST and reenable the USCI interrupts.

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