NCP2892 Series

1.3 Watt Audio Power Amplifier with Fast Turn On Time

The NCP2892 is an audio power amplifier designed for portable communication device applications such as mobile phone applications. The NCP2892 is capable of delivering 1.3 W of continuous average power to an 8.0 Ω BTL load from a 5.0 V power supply, and 1.0 W to a 4.0 Ω BTL load from a 3.6 V power supply.

The NCP2892 provides high quality audio while requiring few external components and minimal power consumption. It features a low−power consumption shutdown mode, which is achieved by driving the $\overline{\text{SHUTDOWN}}$ pin with logic low.

The NCP2892 contains circuitry to prevent from “pop and click” noise that would otherwise occur during turn−on and turn−off transitions.

For maximum flexibility, the NCP2892 provides an externally controlled gain (with resistors), as well as an externally controlled turn−on time (with the bypass capacitor). When using a 1 μF bypass capacitor, it offers 100 ms wake up time.

Due to its excellent PSRR, it can be directly connected to the battery, saving the use of an LDO.

This device is available in a 9−Pin Flip−Chip CSP (Lead−Free).

Features

- 1.3 W to an 8.0 Ω BTL Load from a 5.0 V Power Supply
- Excellent PSRR: Direct Connection to the Battery
- “Pop and Click” Noise Protection Circuit
- Ultra Low Current Shutdown Mode: 10 nA
- 2.2 V−5.5 V Operation
- External Gain Configuration Capability
- External Turn−on Time Configuration Capability: 100 ms (1 μF Bypass Capacitor)
- Up to 1.0 nF Capacitive Load Driving Capability
- Thermal Overload Protection Circuitry
- This is a Pb−Free Device*

Typical Applications

- Portable Electronic Devices
- PDAs
- Wireless Phones

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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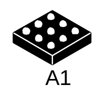
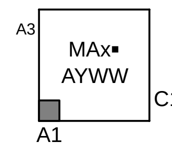
MARKING DIAGRAMS



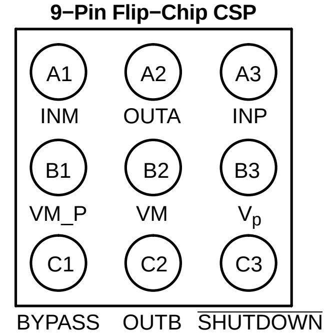
9−Pin Flip−Chip CSP
FC SUFFIX
CASE 499E



MAx	= Specific Device Code
	X = NCP2892A
	Z = NCP2892B
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS

9−Pin Flip−Chip CSP



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

September, 2006 − Rev. 3

Publication Order Number:
NCP2892/D

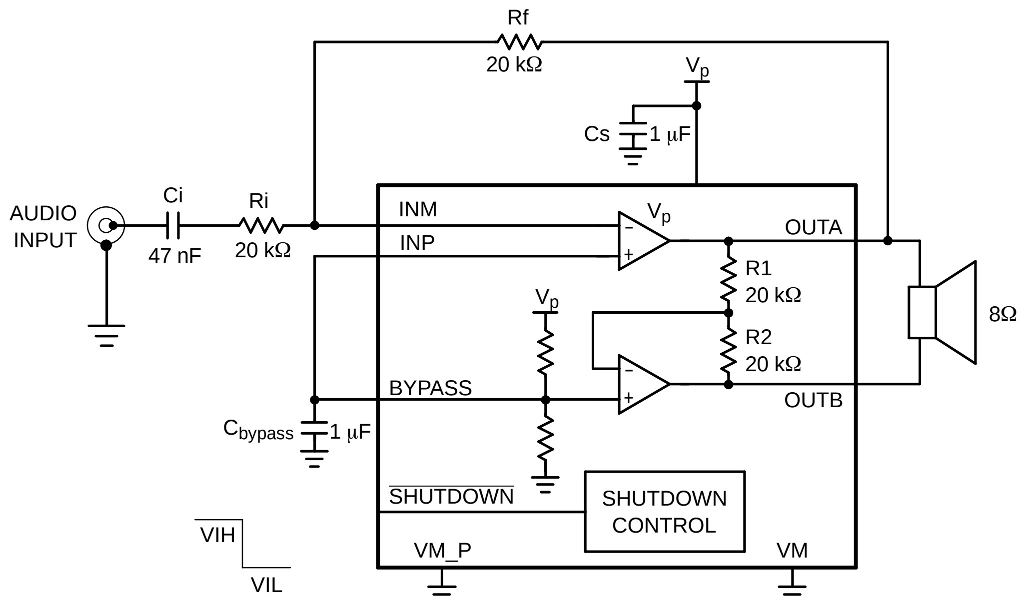


Figure 1. Typical Audio Amplifier Application Circuit with Single Ended Input

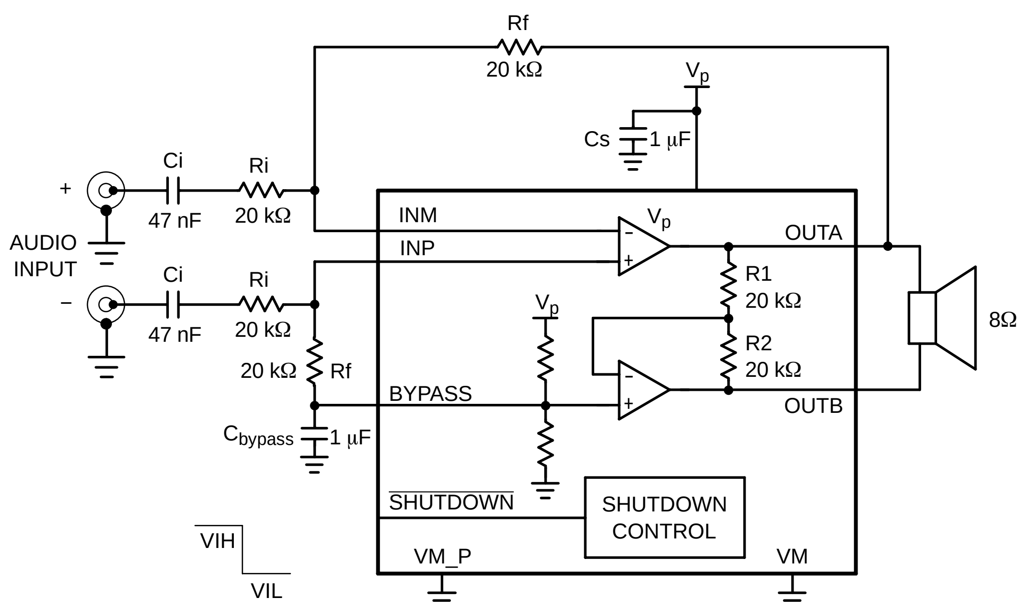


Figure 2. Typical Audio Amplifier Application Circuit with a Differential Input

This device contains 671 active transistors and 1899 MOS gates.

PIN DESCRIPTION

Pin	Type	Symbol	Description
A1	I	INM	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R_f and to the input resistor R_{in}.
A2	O	OUTA	Negative output of the NCP2892. Connected to the load and to the feedback resistor Rf.
A3	I	INP	Positive input of the first amplifier, receives the common mode voltage.
B1	I	VM_P	Power Analog Ground.
B2	I	VM	Core Analog Ground.
B3	I	V_p	Positive analog supply of the cell. Range: 2.2 V−5.5 V.
C1	I	BYPASS	Bypass capacitor pin which provides the common mode voltage (Vp/2).
C2	O	OUTB	Positive output of the NCP2892. Connected to the load.
C3	I	$\overline{\text{SHUTDOWN}}$	The device enters in shutdown mode when a low level is applied on this pin.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_p	6.0	V
Operating Supply Voltage	Op Vp	2.2 to 5.5 V 2.0 V = Functional Only	−
Input Voltage	V_{in}	−0.3 to Vcc +0.3	V
Max Output Current	Iout	500	mA
Power Dissipation (Note 2)	Pd	Internally Limited	−
Operating Ambient Temperature	T_A	−40 to +85	°C
Max Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance Junction−to−Air	$R_{\theta JA}$	(Note 3)	°C/W
ESD Protection Human Body Model (HBM) (Note 4) NCP2892A NCP2892B Machine Model (MM) (Note 5)	−	 8000 6000 >250	V
Latchup Current at T_A = 85°C (Note 6)	−	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
2. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation. For further information see page 10.
3. The $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. For further information see page 10. The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.
4. Human Body Model, 100 pF discharge through a 1.5 kΩ resistor following specification JESD22/A114.
5. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
6. Maximum ratings per JEDEC standard JESD78.

ELECTRICAL CHARACTERISTICS Limits apply for T_A between −40°C to +85°C (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Supply Quiescent Current	I_{dd}	V_p = 2.6 V, No Load V_p = 5.0 V, No Load	− −	1.5 1.7	4	mA
		V_p = 2.6 V, 8 Ω V_p = 5.0 V, 8 Ω	− −	1.7 1.9	5.5	
Common Mode Voltage	V_{cm}	−	−	$V_p/2$	−	V
Shutdown Current	I_{SD}	T_A = +25°C T_A = −40°C to +85°C	−	0.01	0.5 1.0	μA
Shutdown Voltage High	V_{SDIH}	−	1.2	−	−	V
Shutdown Voltage Low	V_{SDIL}	−	−	−	0.4	V
Turning On Time (Note 9)	T_{WU}	C_{by} = 1 μF	−	90	−	ms
Turning Off Time	T_{OFF}	−	−	1.0	−	μs
Output Impedance in Shutdown Mode NCP2892A NCP2892B	Z_{SD}	−	 − −	 100 10	 − −	 Ω kΩ
Output Swing NCP2892A	$V_{loadpeak}$	V_p = 2.6 V, R_L = 8.0 Ω V_p = 5.0 V, R_L = 8.0 Ω (Note 8) T_A = +25°C T_A = −40°C to +85°C	1.6 4.0 3.85	2.12 4.15	− −	V
Output Swing NCP2892B	$V_{loadpeak}$	V_p = 2.6 V, R_L = 8.0 Ω V_p = 5.0 V, R_L = 8.0 Ω (Note 8) T_A = +25°C T_A = −40°C to +85°C	1.6 4.0 3.85	2.20 4.50	− −	V
Rms Output Power NCP2892A	P_O	V_p = 2.6 V, R_L = 4.0 Ω THD + N < 0.1% V_p = 2.6 V, R_L = 8.0 Ω THD + N < 0.1% V_p = 5.0 V, R_L = 8.0 Ω THD + N < 0.1%	− −	0.36 0.28 1.08	− −	W
Rms Output Power NCP2892B	P_O	V_p = 2.6 V, R_L = 4.0 Ω THD + N < 0.1% V_p = 2.6 V, R_L = 8.0 Ω THD + N < 0.1% V_p = 5.0 V, R_L = 8.0 Ω THD + N < 0.1%	− −	0.40 0.30 1.20	− −	W
Maximum Power Dissipation (Note 9)	P_{Dmax}	V_p = 5.0 V, R_L = 8.0 Ω	−	−	0.65	W
Output Offset Voltage	V_{OS}	V_p = 2.6 V V_p = 5.0 V	−30		30	mV
Signal−to−Noise Ratio	SNR	V_p = 2.6 V, G = 2.0 10 Hz < F < 20 kHz V_p = 5.0 V, G = 10 10 Hz < F < 20 kHz	− −	84 77	− −	dB
Positive Supply Rejection Ratio	PSRR V+	G = 2.0, R_L = 8.0 Ω Vp_{ripple_pp} = 200 mV C_{by} = 1.0 μF Input Terminated with 10 Ω F = 217 Hz V_p = 5.0 V V_p = 3.0 V V_p = 2.6 V F = 1.0 kHz V_p = 5.0 V V_p = 3.0 V V_p = 2.6 V	 − − − − − −	 −64 −72 −73 −64 −74 −75	 − − − − − −	dB
Efficiency	η	V_p = 2.6 V, P_{orms} = 320 mW V_p = 5.0 V, P_{orms} = 1.0 W	− −	48 63	− −	%

ELECTRICAL CHARACTERISTICS Limits apply for T_A between −40°C to +85°C (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Thermal Shutdown Temperature (Note 10)	T_{sd}		140	160	180	°C
Total Harmonic Distortion	THD	V_p = 2.6, F = 1.0 kHz R_L = 4.0 Ω, A_V = 2.0 P_O = 0.32 W	− − −	− 0.04 −	− − −	%
		V_p = 5.0 V, F = 1.0 kHz R_L = 8.0 Ω, A_V = 2.0 P_O = 1.0 W	− − −	− 0.02 −	− − −	

7. Min/Max limits are guaranteed by design, test or statistical analysis.
8. This parameter is guaranteed but not tested in production in case of a 5.0 V power supply.
9. See page 12 for a theoretical approach of this parameter.
10. For this parameter, the Min/Max values are given for information.

TYPICAL PERFORMANCE CHARACTERISTICS

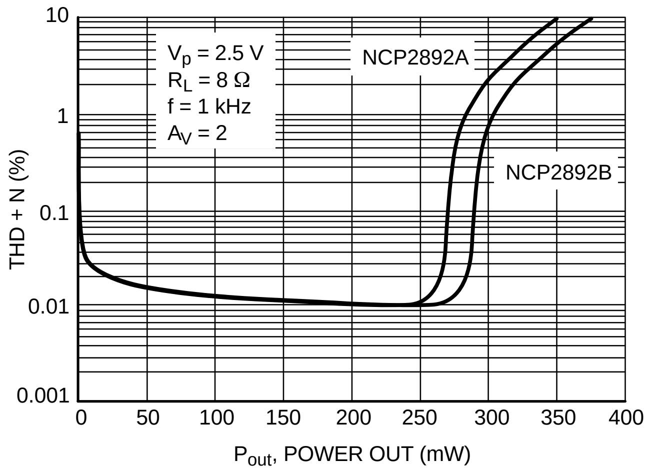


Figure 3. THD + N versus Power Out

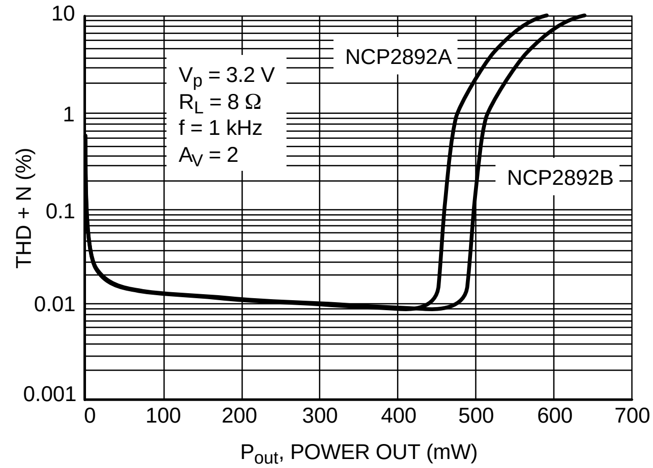


Figure 4. THD + N versus Power Out

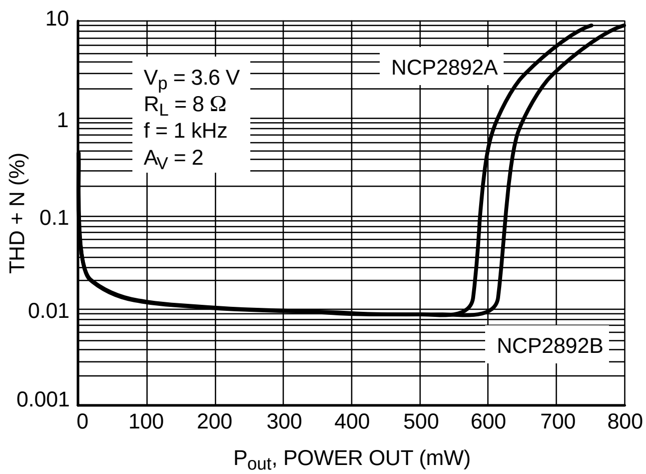


Figure 5. THD + N versus Power Out

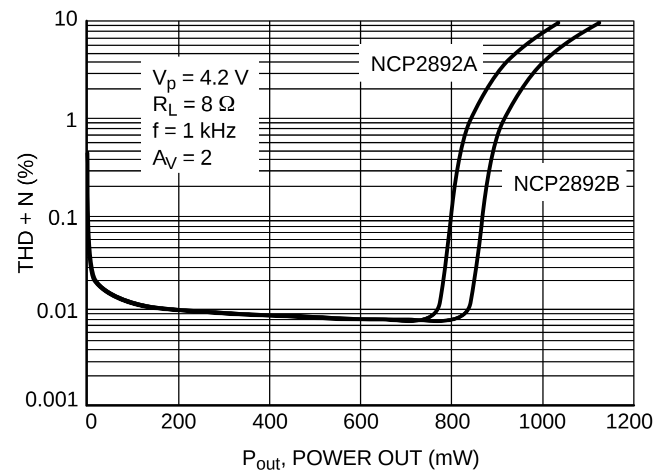


Figure 6. THD + N versus Power Out

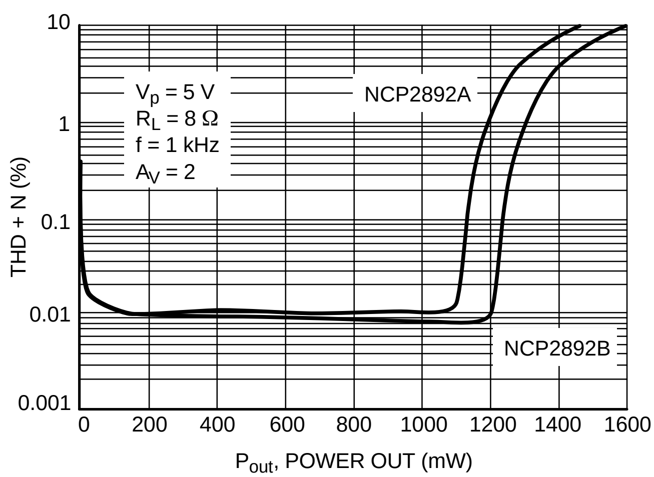


Figure 7. THD + N versus Power Out

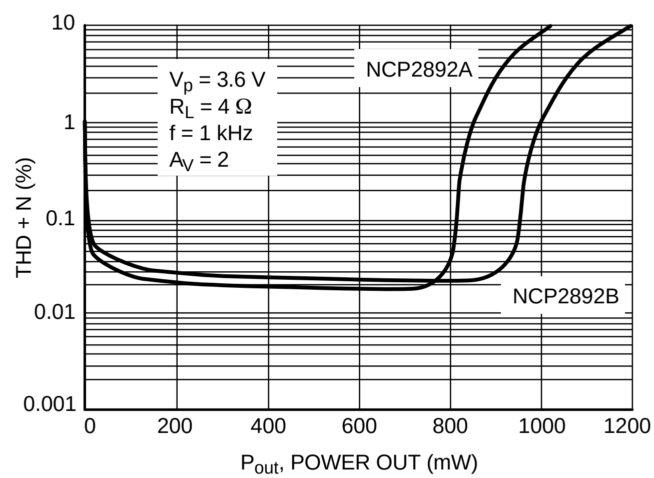


Figure 8. THD + N versus Power Out

TYPICAL PERFORMANCE CHARACTERISTICS

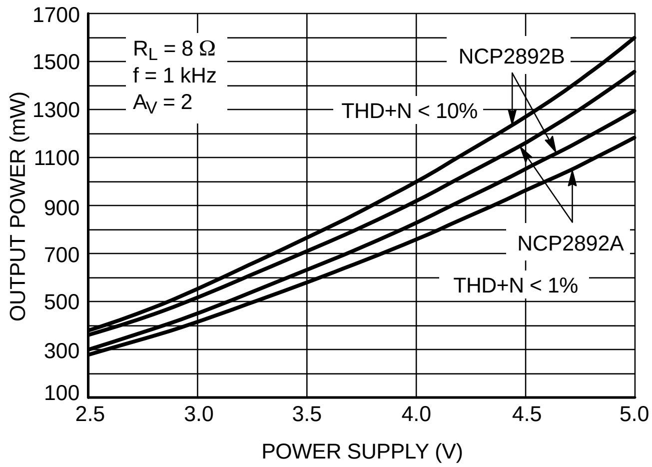


Figure 9. Output Power versus Power Supply

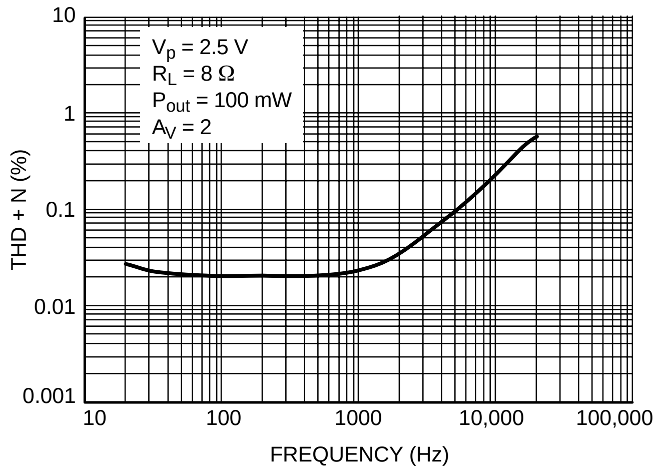


Figure 10. THD + N versus Frequency

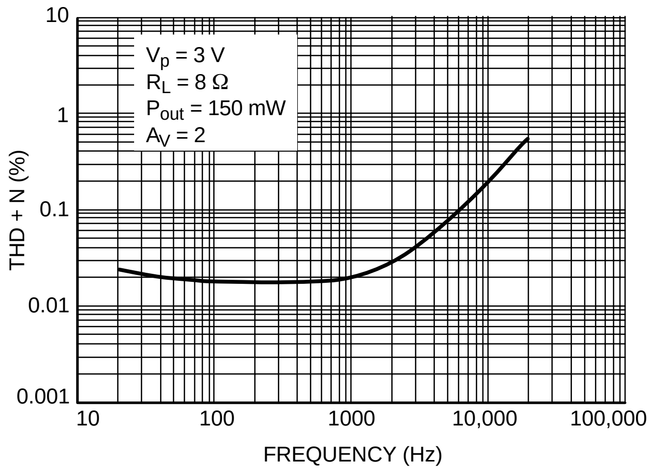


Figure 11. THD + N versus Frequency

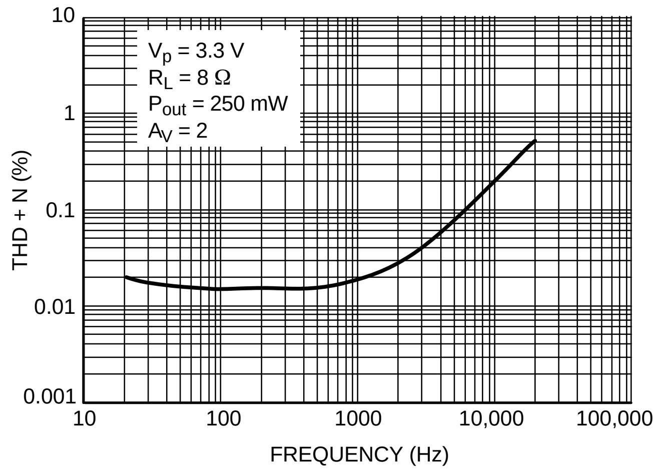


Figure 12. THD + N versus Frequency

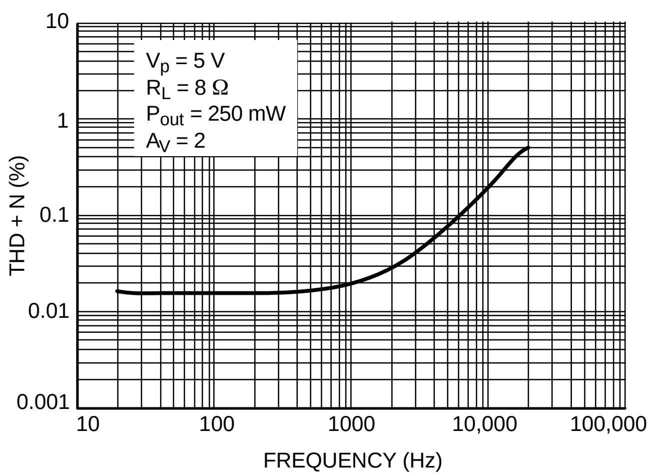


Figure 13. THD + N versus Frequency

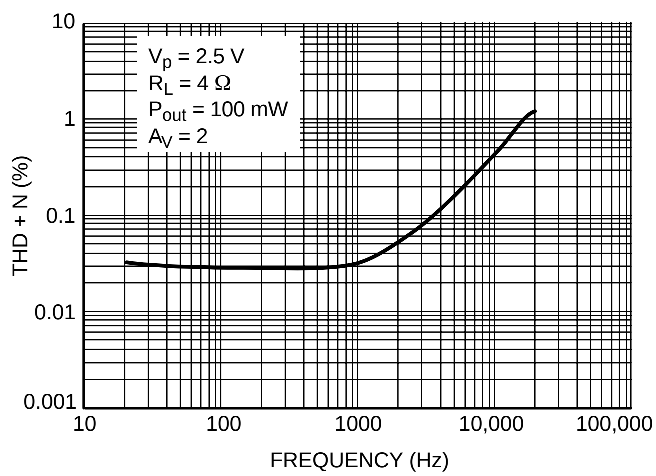


Figure 14. THD + N versus Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

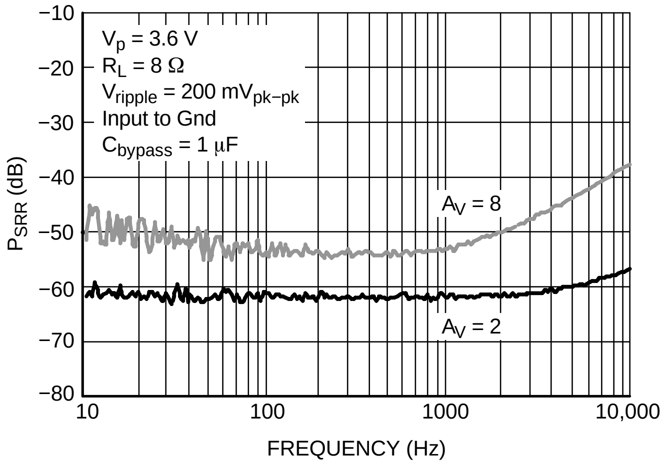


Figure 15. P_{SRR} @ V_p = 3.6 V Single Ended Audio Input to Ground

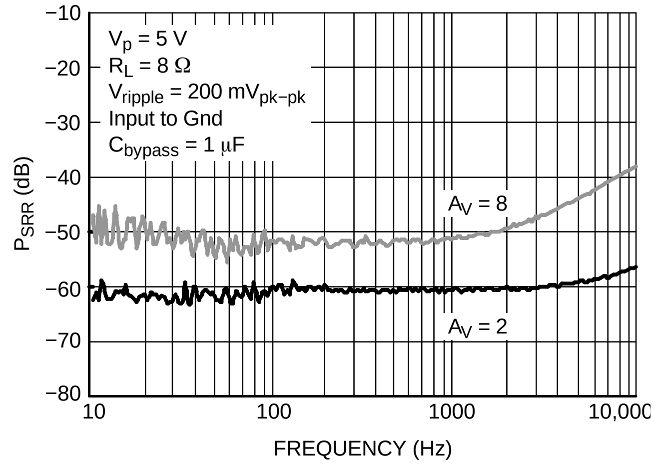


Figure 16. P_{SRR} @ V_p = 5 V Single Ended Audio Input to Ground

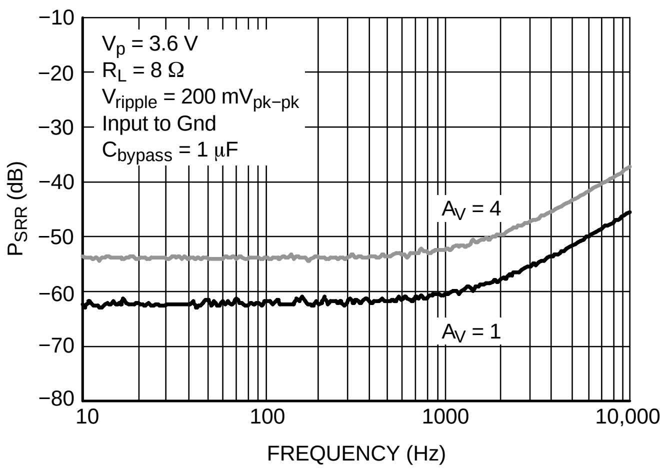


Figure 17. P_{SRR} @ V_p = 3.6 V Differential Audio Input to Ground

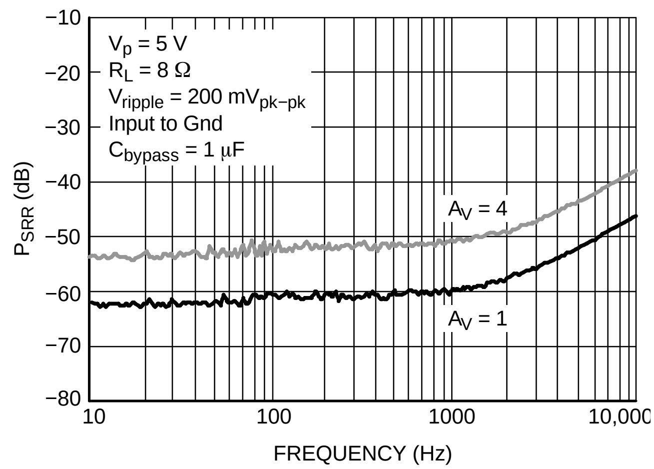


Figure 18. P_{SRR} @ V_p = 5 V Differential Audio Input to Ground

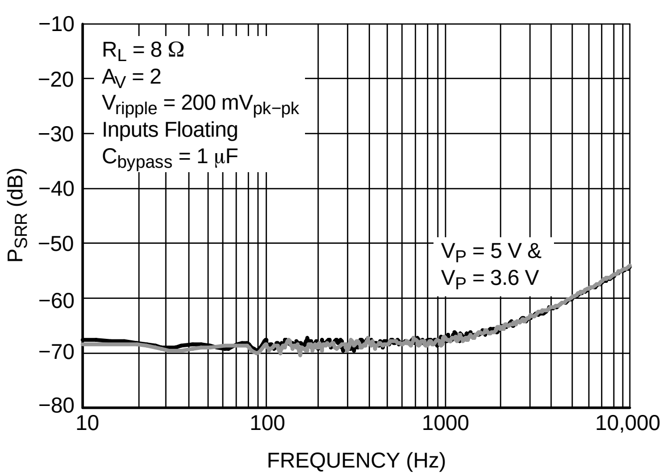


Figure 19. P_{SRR} @ V_p = 3.6 V Single Ended Audio Input Floating

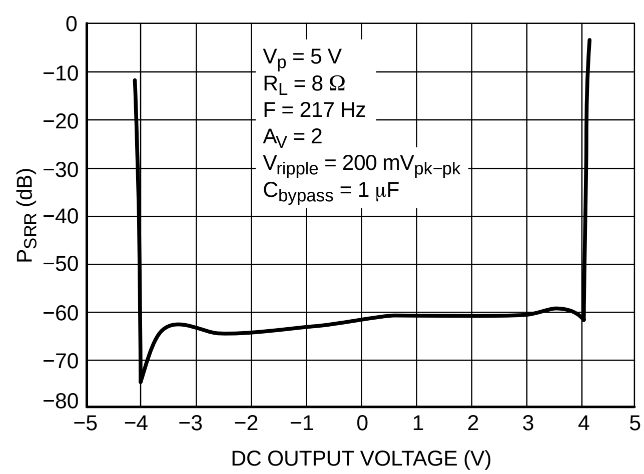


Figure 20. P_{SRR} @ DC Output Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

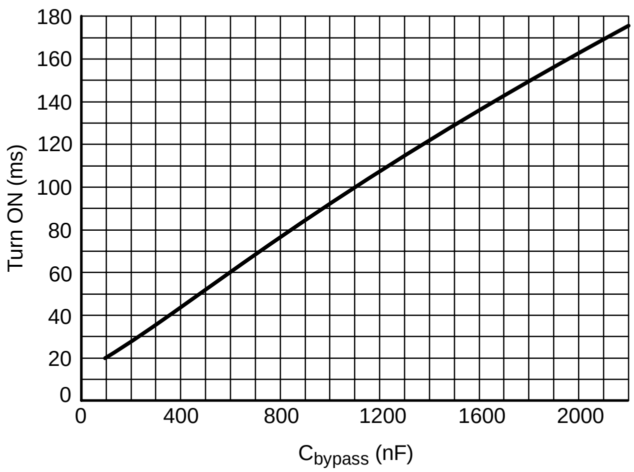


Figure 21. T_{ON} versus C_{bypass} @ V_{bat} = 3.6 V, T_A = +25°C

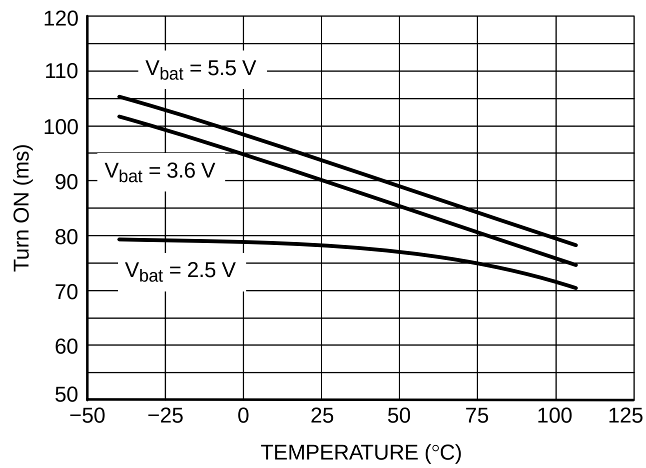


Figure 22. T_{ON} versus Temperature @ V_{bat} = 3.6 V, C_{bypass} = 1 μF

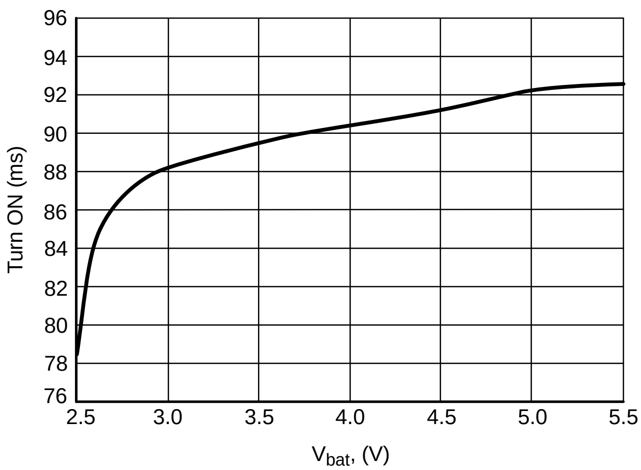


Figure 23. T_{ON} vs. V_{bat} @ C_{bypass} = 1 μF, T_A = +25°C

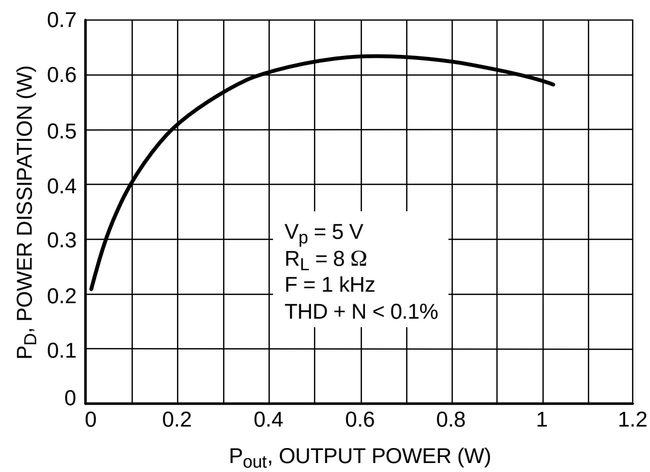


Figure 24. Power Dissipation versus Output Power

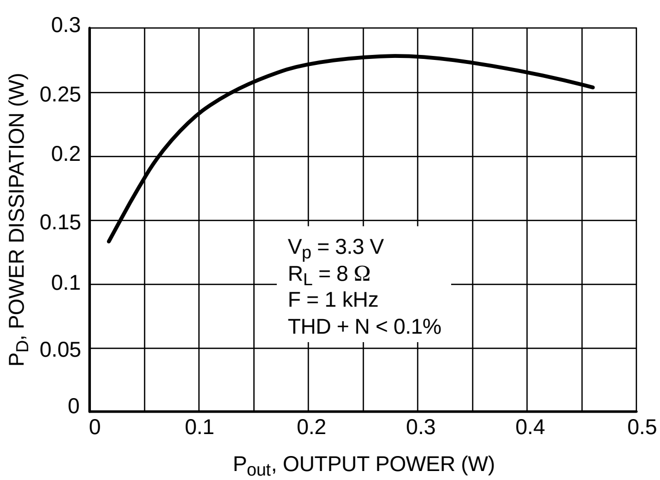


Figure 25. Power Dissipation versus Output Power

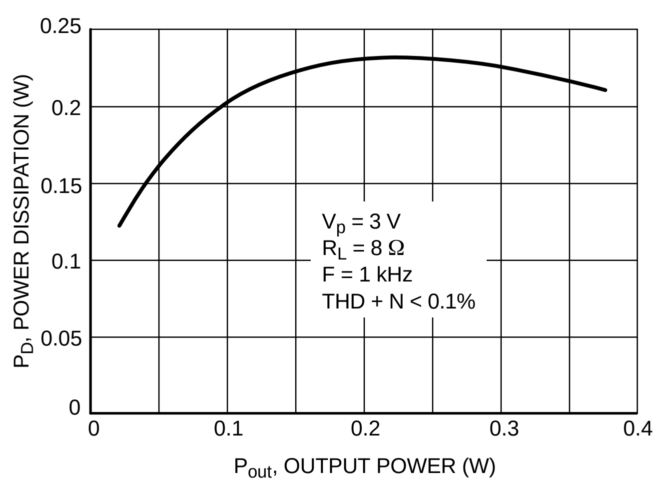


Figure 26. Power Dissipation versus Output Power

TYPICAL PERFORMANCE CHARACTERISTICS

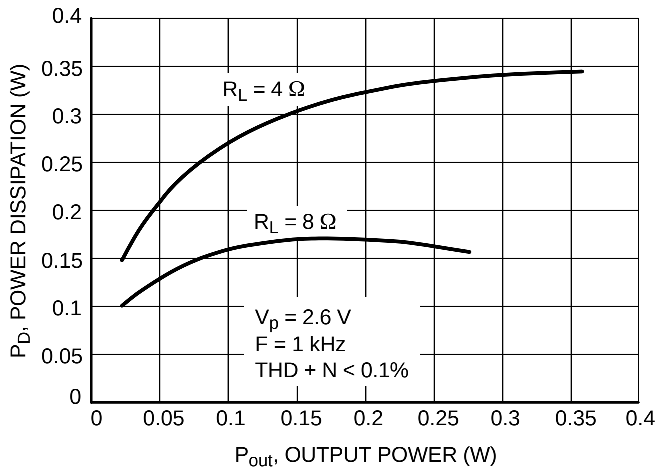


Figure 27. Power Dissipation versus Output Power

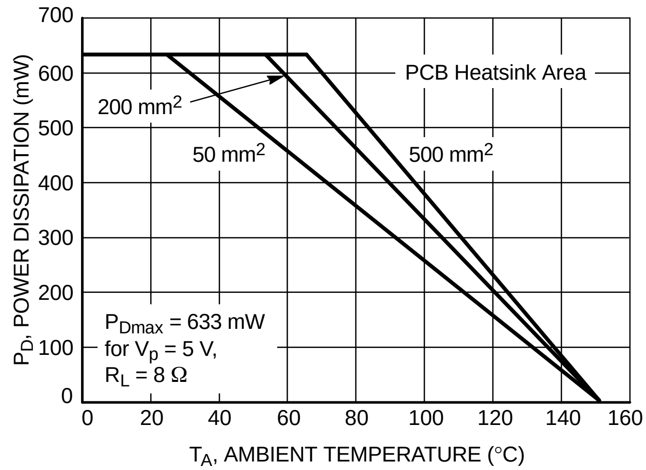


Figure 28. Power Derating − 9−Pin Flip−Chip CSP

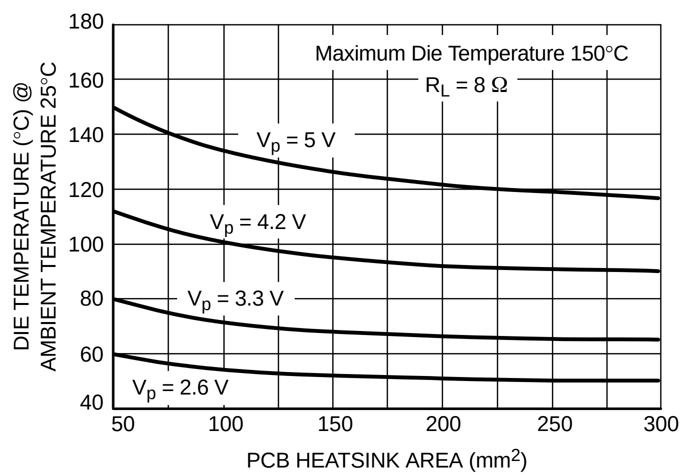


Figure 29. Maximum Die Temperature versus PCB Heatsink Area

TYPICAL PERFORMANCE CHARACTERISTICS

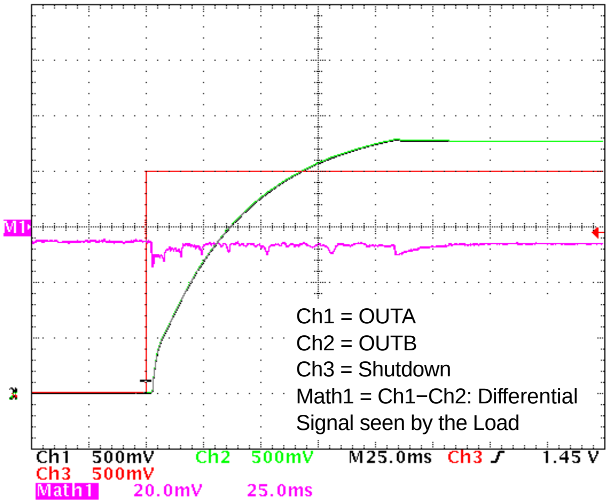


Figure 30. Zero Pop Noise Turn On Sequence with Differential Input to Ground; C_{in} = 100 nF, R_{in} = 24 Ω, R_f = 100 kΩ, C_{byp} = 1 µF, R_L = 8 Ω

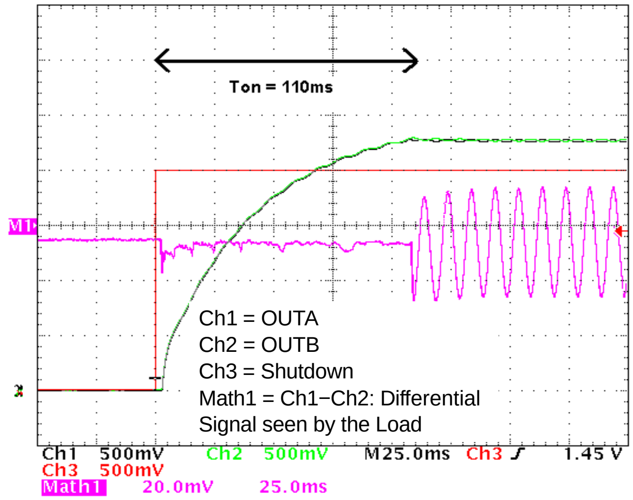


Figure 31. Zero Pop Noise Turn On Sequence with Differential Audio Source; C_{in} = 100 nF, R_{in} = 24 Ω, R_f = 100 kΩ, C_{byp} = 1 µF, R_L = 8 Ω

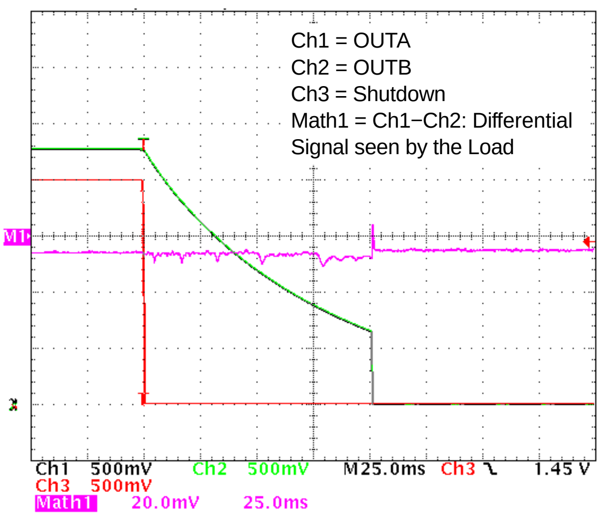


Figure 32. Zero Pop Noise Turn Off Sequence with Differential Input to Ground; C_{in} = 100 nF, R_{in} = 24 Ω, R_f = 100 kΩ, C_{byp} = 1 µF, R_L = 8 Ω

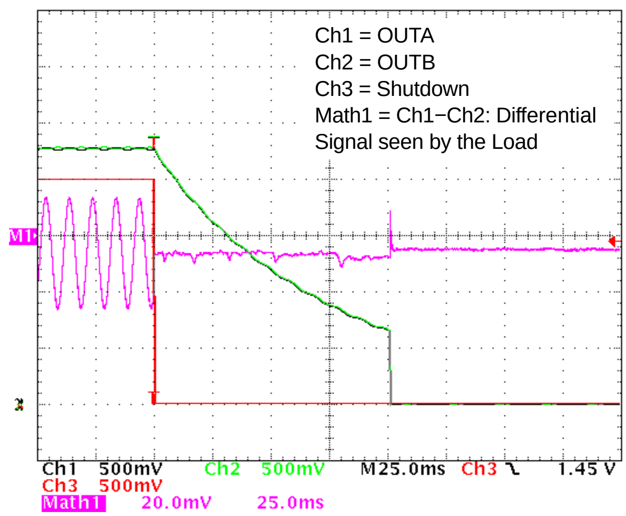


Figure 33. Zero Pop Noise Turn Off Sequence with Differential Audio Source; C_{in} = 100 nF, R_{in} = 24 Ω, R_f = 100 kΩ, C_{byp} = 1 µF, R_L = 8 Ω

APPLICATION INFORMATION

Detailed Description

The NCP2892 audio amplifier can operate under 2.6 V until 5.5 V power supply. With less than 1% THD+N, B version can deliver up to 1.2 W rms output power to an 8.0 Ω load (V_p = 5.0 V). If application allows to reach 10% THD+N, then 1.6 W can be provided using a 5.0 V power supply.

The structure of the NCP2892 is basically composed of two identical internal power amplifiers; the first one is externally configurable with gain−setting resistors R_{in} and R_f (the closed−loop gain is fixed by the ratios of these resistors) and the second is internally fixed in an inverting unity−gain configuration by two resistors of 20 kΩ. So the load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor. The NCP2892A has around 100 Ω and the NCP2892B has around 10 kΩ output impedance in the shutdown mode.

Internal Power Amplifier

The output PMOS and NMOS transistors of the amplifier were designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors does not exceed 0.6 Ω when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

Turn−On and Turn−Off Transitions

A cycle with a turn−on and turn−off transition is illustrated with plots that show both single ended signals on the previous page.

In order to eliminate “pop and click” noises during transitions, output power in the load must be slowly established or cut. When logic high is applied to the shutdown pin, the bypass voltage begins to rise exponentially and once the output DC level is around the common mode voltage, the gain is established instantaneously. This way to turn−on the device is optimized in terms of rejection of “pop and click” noises.

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. During the shutdown mode, amplifier outputs are connected to the ground.

When a shutdown low level is applied, with 1 μF bypass capacitor, it takes 65 ms before the DC output level is tied to Ground on each output. However, no audio signal will be provided to the BTL load only 1 μs after the falling edge on the shutdown pin.

With 1 μF bypass capacitor, turn on time is set to 90 ms. This fast turn on time added to a very low shutdown current saves battery life and brings flexibility when designing the audio section of the final application.

NCP2892 is a zero pop noise device when using a differential audio input. In case of a single ended one, there is no audible pop click noise, especially when the input cut off frequency is higher than 100 Hz.

Shutdown Function

The device enters shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 100 nA. In this configuration, the output impedance is 10 kΩ on each output.

Current Limit Circuit

The maximum output power of the circuit (Porms = 1.0 W, V_p = 5.0 V, R_L = 8.0 Ω) requires a peak current in the load of 500 mA.

In order to limit the excessive power dissipation in the load when a short−circuit occurs, the current limit in the load is fixed to 800 mA. The current in the four output MOS transistors are real−time controlled, and when one current exceeds 800 mA, the gate voltage of the MOS transistor is clipped and no more current can be delivered.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceeds 160°C, and will be switched on again only when the temperature decreases fewer than 140°C.

The NCP2892 is unity−gain stable and requires no external components besides gain−setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application.

The first amplifier is externally configurable (R_f and R_{in}), while the second is fixed in an inverting unity gain configuration.

The differential−ended amplifier presents two major advantages:

− The possible output power is four times larger (the output swing is doubled) as compared to a single−ended amplifier under the same conditions.
− Output pins (OUTA and OUTB) are biased at the same potential $V_p/2$, this eliminates the need for an output coupling capacitor required with a single−ended amplifier configuration.

The differential closed loop−gain of the amplifier is given by $A_{vd} = 2 * \frac{R_f}{R_{in}} = \frac{V_{orms}}{V_{inrms}}$.

Output power delivered to the load is given by $P_{orms} = \frac{(Vopeak)^2}{2 * R_L}$ (Vopeak is the peak differential output voltage).

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500 mA $I_{opeak} = \frac{V_{opeak}}{R_L}$.

Gain−Setting Resistor Selection (R_{in} and R_f)

R_{in} and R_f set the closed−loop gain of the amplifier.

In order to optimize device and system performance, the NCP2892 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance.

An input resistor (R_{in}) value of 22 kΩ is realistic in most of applications, and doesn't require the use of a too large capacitor C_{in}.

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{in}, the cut−off frequency is given by

$$fc = \frac{1}{2 * \Pi * R_{in} * C_{in}}.$$

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage ($V_p/2$) and can increase the turn−on pops when a single ended audio input is used.

An input capacitor value between 33 nF and 220 nF performs well in many applications (With R_{in} = 22 KΩ).

Bypass Capacitor Selection (Cby)

The bypass capacitor Cby provides half−supply filtering and determines how fast the NCP2892 turns on (see Figure 21). With a differential audio input, the amplifier will be a zero pop noise device no matter the bypass capacitor.

With a single ended audio input, this capacitor is a critical component to minimize the turn−on pop. A 1.0 μF bypass capacitor value (C_{in} = < 0.39 μF) should produce clickless and popless shutdown transitions. The amplifier is still functional with a 0.1 μF capacitor value but is more susceptible to "pop and click" noises.

Thus, a 1.0 μF bypassing capacitor is recommended.

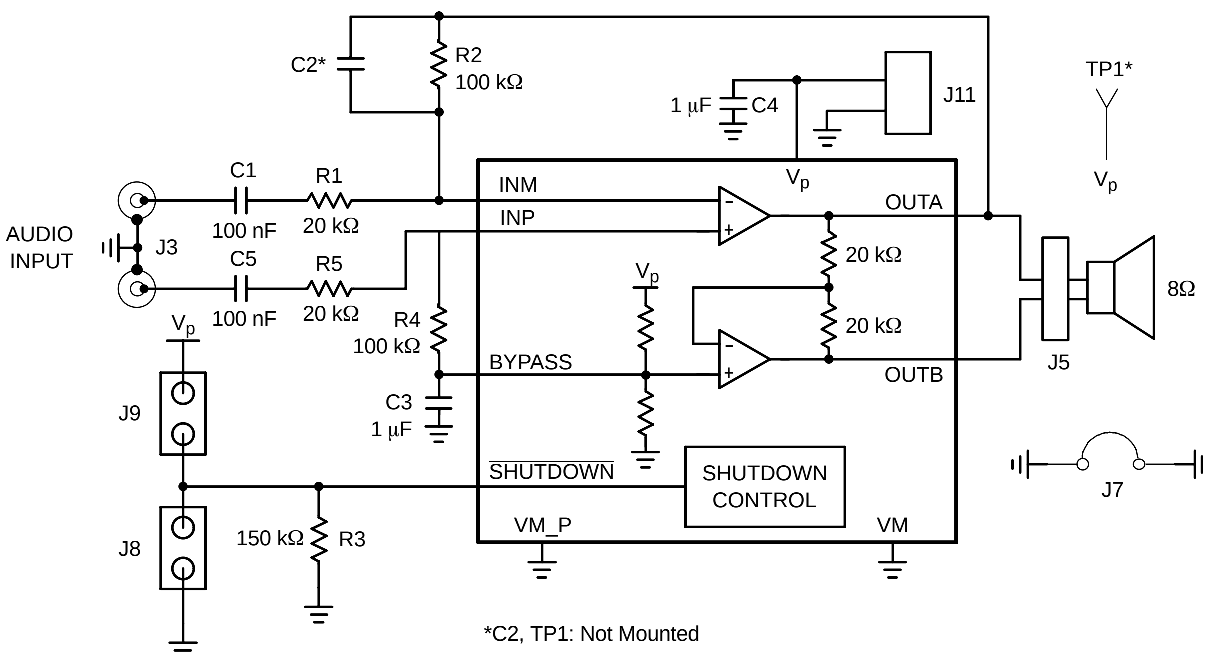
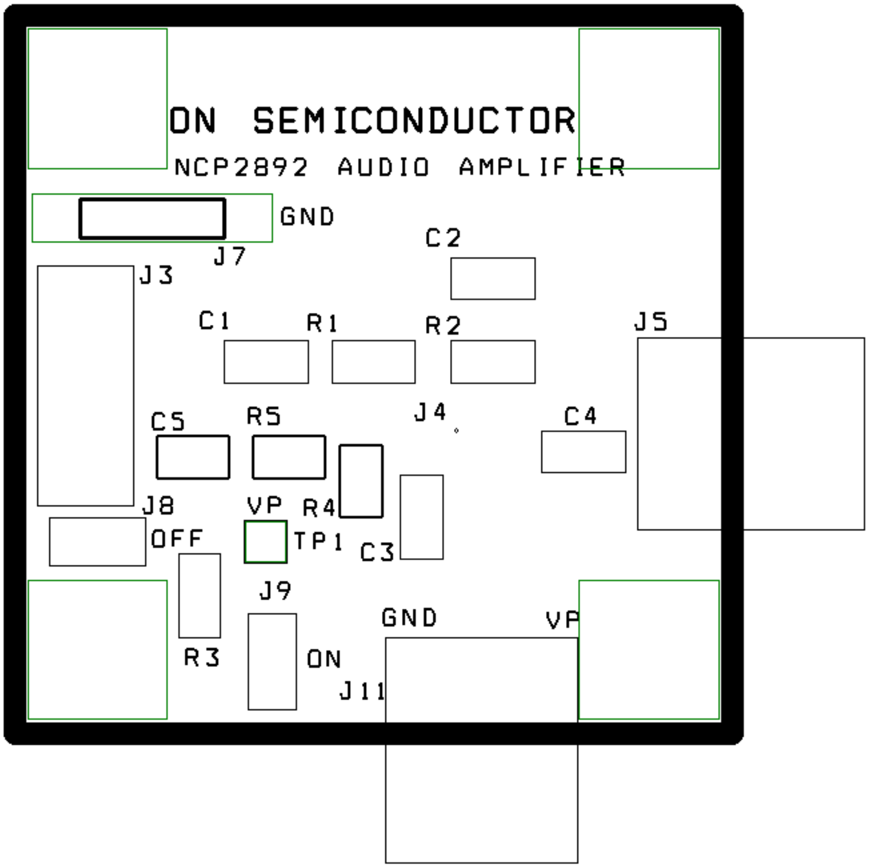


Figure 34. Schematic of the Demonstration Board of the 9−Pin Flip−Chip CSP Device



Silkscreen Layer

Figure 35. Demonstration Board for 9−Pin Flip−Chip CSP Device − PCB Layers

BILL OF MATERIAL

Item	Part Description	Ref.	PCB Footprint	Manufacturer	Manufacturer Reference
1	NCP2892 Audio Amplifier	−	−	ON Semiconductor	NCP2892
2	SMD Resistor 20 KΩ	R1, R5	0805	Panasonic	ERJ−6GEYJ203V
3	SMD Resistor 100 KΩ	R2, R4	0805	Panasonic	ERJ−6GEYJ104V
4	SMD Resistor 150 KΩ	R3	0805	Panasonic	ERJ−6GEYJ154V
5	Ceramic Capacitor 100 nF, 100 V X7R	C1, C5	0805	TDK	C2012X7R2A473K
6	Ceramic Capacitor 1.0 μF, 10 V X7R	C3, C4	0805	TDK	C2012X7R1A105K
7	Jumper Header Vertical Mount, 2 positions, 100 mils	J8, J9, J12	100 mils	Tyco Electronics / AMP	5−826629−0
8	I/O Connector, 2 positions	J5, J11	200 mils	Phoenix Contact	1757242
9	Jumper Connector	J7	400 mils	Harwin	D3082−B01
10	Not Mounted	C2, TP1	−	−	−

ORDERING INFORMATION

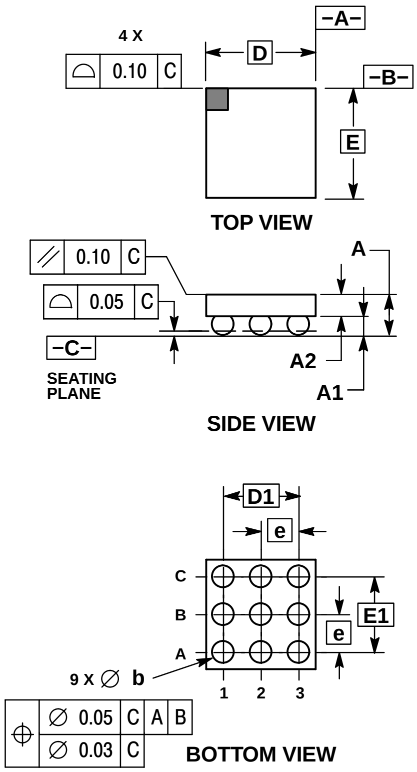
Device	Marking	Package	Shipping†
NCP2892AFCT2G	MAX	9−Pin Flip−Chip CSP (Pb−Free)	3000/Tape and Reel
NCP2892BFCT2G	MAZ	9−Pin Flip−Chip CSP (Pb−Free)	3000/Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The NCP2892AFCT2G version requires a lead−free solder paste and should not be used with a SnPb solder paste.

PACKAGE DIMENSIONS

9 PIN FLIP−CHIP
CASE 499E−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

PUBLICATION ORDERING INFORMATION

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