NCV898031

2 MHz Non-Synchronous SEPIC/Boost Controller

The NCV898031 is an adjustable output non−synchronous 2 MHz SEPIC/boost controller which drives an external N−channel MOSFET. The device uses peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the gate driver.

Protection features include internally−set soft−start, undervoltage lockout, cycle−by−cycle current limiting and thermal shutdown.

Additional features include low quiescent current sleep mode and microprocessor compatible enable pin.

Features

- Peak Current Mode Control with Internal Slope Compensation
- 1.2 V ±2% Reference Voltage
- 2 MHz Fixed Frequency Operation
- Wide Input Voltage Range of 3.2 V to 40 V, 45 V Load Dump
- Input Undervoltage Lockout (UVLO)
- Internal Soft−Start
- Low Quiescent Current in Sleep Mode (< 10 μA Typical)
- Cycle−by−Cycle Current Limit Protection
- Hiccup−Mode Overcurrent Protection (OCP)
- Hiccup−Mode Short−Circuit Protection (SCP)
- Thermal Shutdown (TSD)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Small Form Factor Point−of−Load Power Regulation
- Headlamps
- Backlighting

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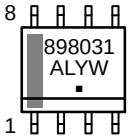
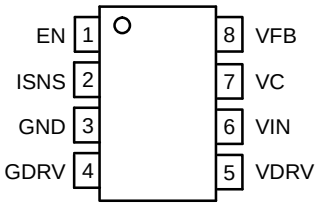
MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751



898031	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV898031D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

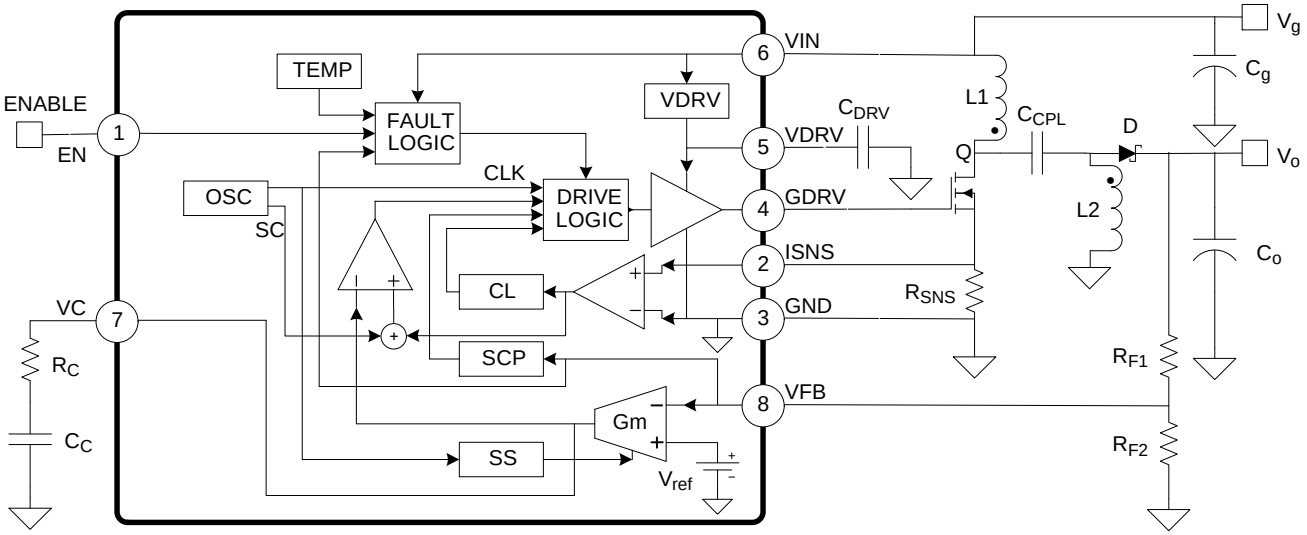


Figure 1. Simplified Block Diagram and Application Schematic

PACKAGE PIN DESCRIPTIONS

Pin No.	Pin Symbol	Function
1	EN	Enable input. The part is disabled into sleep mode when this pin is brought low for longer than the enable time−out period.
2	ISNS	Current sense input. Connect this pin to the source of the external N−MOSFET, through a current−sense resistor to ground to sense the switching current for regulation and current limiting.
3	GND	Ground reference.
4	GDRV	Gate driver output. Connect to gate of the external N−MOSFET. A series resistance can be added from GDRV to the gate to tailor EMC performance.
5	VDRV	Driving voltage. Internally−regulated supply for driving the external N−MOSFET, sourced from VIN. Bypass with a 1.0 μF ceramic capacitor to ground.
6	VIN	Input voltage. If bootstrapping operation is desired, connect a diode from the input supply to VIN, in addition to a diode from the output voltage to VDRV and/or VIN.
7	VC	Output of the voltage error amplifier. An external compensator network from VC to GND is used to stabilize the converter.
8	VFB	Output voltage feedback. A resistor from the output voltage to VFB with another resistor from VFB to GND creates a voltage divider for regulation and programming of the output voltage.

ABSOLUTE MAXIMUM RATINGS (Voltages are with respect to GND, unless otherwise indicated)

Rating	Value	Unit
Dc Supply Voltage (VIN)	−0.3 to 40	V
Peak Transient Voltage (Load Dump on VIN)	45	V
Dc Supply Voltage (VDRV, GDRV)	12	V
Peak Transient Voltage (VFB)	−0.3 to 6	V
Dc Voltage (VC, VFB, ISNS)	−0.3 to 3.6	V
Dc Voltage (EN)	−0.3 to 6	V
Dc Voltage Stress (VIN − VDRV)*	−0.7 to 40	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*An external diode from the input to the VIN pin is required if bootstrapping VDRV and VIN off of the output voltage.

PACKAGE CAPABILITIES

Characteristic		Value	Unit
ESD Capability (All Pins)	Human Body Model Machine Model	≥ 2.0 ≥ 200	KV V
Moisture Sensitivity Level		1	
Package Thermal Resistance	Junction−to−Ambient, $R_{\theta JA}$ (Note 1)	100	°C/W

1. Value based on copper are of 650 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 150°C$, $3.2\ V < V_{IN} < 40\ V$, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0, T_J = 25°C	−	2.0	−	μA
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0, −40°C < T_J < 125°C	−	2.0	6.0	μA
Quiescent Current, No switching	$I_{q,off}$	Into VIN pin, EN = 1, No switching	−	1.5	2.5	mA
Quiescent Current, Switching, normal operation	$I_{q,on}$	Into VIN pin, EN = 1, Switching	−	4.0	6.0	mA
OSCILLATOR						
Minimum pulse width	$t_{on,min}$		30	65	90	ns
Maximum duty cycle	D_{max}		85	88	90	%
Switching frequency	f_s		1.8	2.0	2.2	MHz
Soft−start time	t_{ss}	From start of switching with V_{FB} = 0 until reference voltage = V_{REF}	520	650	780	μs
Soft−start delay	$t_{ss,dly}$	From EN → 1 until start of switching with V_{FB} = 0 with V_C pin compensation network disconnected	80	100	280	μs
Slope compensating ramp	S_a		28	34	40	mV/μs
ENABLE						
EN pull−down current	I_{EN}	V_{EN} = 5 V	−	5.0	10	μA
EN input high voltage	$V_{s,ih}$		2.0	−	5.0	V
EN input low voltage	$V_{s,il}$		0	−	800	mV
EN time−out ratio	$\%t_{en}$	From EN falling edge, to oscillator control (EN high) or shutdown (EN low), Percent of typical switching frequency	−	250	350	%
CURRENT SENSE AMPLIFIER						
Low−frequency gain	A_{csa}	Input−to−output gain at dc, ISNS ≤ 1 V	0.9	1.0	1.1	V/V
Bandwidth	BW_{csa}	Gain of A_{csa} − 3 dB	2.5	−	−	MHz
ISNS input bias current	$I_{sns,bias}$	Out of ISNS pin	−	30	50	μA
Current limit threshold voltage	V_{cl}	Voltage on ISNS pin	360	400	440	mV
Current limit, Response time	t_{cl}	CL tripped until GDRV falling edge, V_{ISNS} = V_{cl}(typ) + 60 mV	−	80	125	ns
Overcurrent protection, Threshold voltage	$\%V_{ocp}$	Percent of V_{cl}	125	150	175	%
Overcurrent protection, Response Time	t_{ocp}	From overcurrent event, Until switching stops, V_{ISNS} = V_{OCP} + 40 mV	−	80	125	ns
VOLTAGE ERROR OPERATIONAL TRANSCONDUCTANCE AMPLIFIER						
Transconductance	$g_{m,vea}$	$V_{FB} - V_{ref} = \pm 20$ mV	0.92	1.28	1.63	mS
VEA output resistance	$R_{o,vea}$		2.0	−	−	MΩ
VFB input bias current	$I_{vfb,bias}$	Current out of VFB pin	−	0.5	2.0	μA
Reference voltage	V_{ref}		1.176	1.200	1.224	V
VEA maximum output voltage	$V_{c,max}$		2.5	−	−	V
VEA minimum output voltage	$V_{c,min}$		−	−	0.3	V
VEA sourcing current	$I_{src,vea}$	VEA output current, Vc = 2.0 V	80	100	−	μA
VEA sinking current	$I_{snk,vea}$	VEA output current, Vc = 0.7 V	80	100	−	μA

ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 150°C$, $3.2\ V < V_{IN} < 40\ V$, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVER						
Sourcing current	I_{src}	$V_{DRV} \geq 6\ V$, $V_{DRV} - V_{GDRV} = 2\ V$	600	800	−	mA
Sinking current	I_{sink}	$V_{GDRV} \geq 2\ V$	500	600	−	mA
Driving voltage dropout	$V_{drv,do}$	$V_{IN} - V_{DRV}$, $Iv_{DRV} = 25\ mA$	−	0.3	0.6	V
Driving voltage source current	I_{drv}	$V_{IN} - V_{DRV} = 1\ V$	35	45	−	mA
Backdrive diode voltage drop	$V_{d,bd}$	$V_{DRV} - V_{IN}$, $I_{d,bd} = 5\ mA$	−	−	0.7	V
Driving voltage	V_{DRV}	$I_{VDRV} = 0.1 - 25\ mA$	6.0	6.3	6.6	V
UVLO						
Undervoltage lock−out, Threshold voltage	V_{uvlo}	V_{IN} falling	2.95	3.05	3.15	V
Undervoltage lock−out, Hysteresis	$V_{uvlo,hys}$	V_{IN} rising	50	150	250	mV
SHORT CIRCUIT PROTECTION						
Startup blanking period	$\%t_{scp,dly}$	From start of soft−start, Percent of t_{ss}	100	120	150	%
Hiccup−mode period	$\%t_{hcp,dly}$	From shutdown to start of soft−start, Percent of t_{ss}	70	85	100	%
Short circuit threshold voltage	$\%V_{scp}$	V_{FB} as percent of V_{ref}	60	67	75	%
Short circuit delay	t_{scp}	From $V_{FB} < V_{scp}$ to stop switching	−	35	100	ns
THERMAL SHUTDOWN						
Thermal shutdown threshold	T_{sd}	T_J rising	160	170	180	°C
Thermal shutdown hysteresis	$T_{sd,hys}$	T_J falling	10	15	20	°C
Thermal shutdown delay	$t_{sd,dly}$	From $T_J > T_{sd}$ to stop switching	−	−	100	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

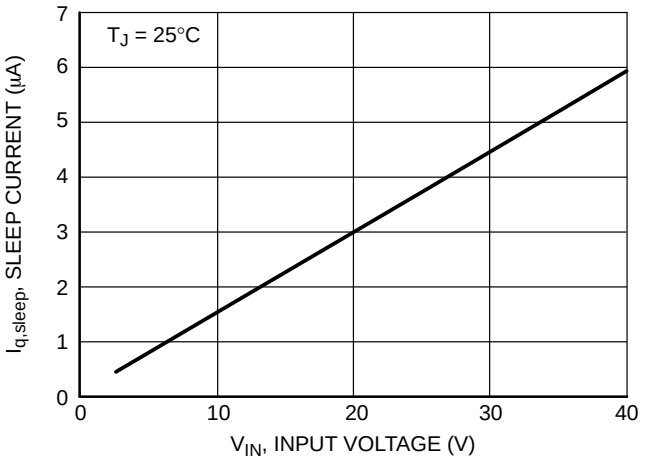


Figure 2. Sleep Current vs. Input Voltage

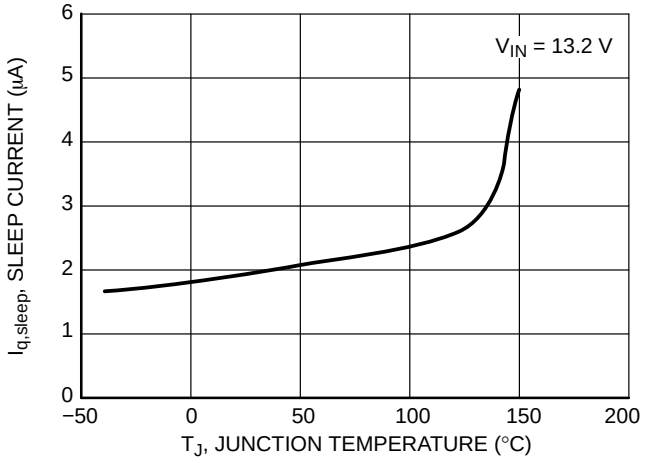


Figure 3. Sleep Current vs. Temperature

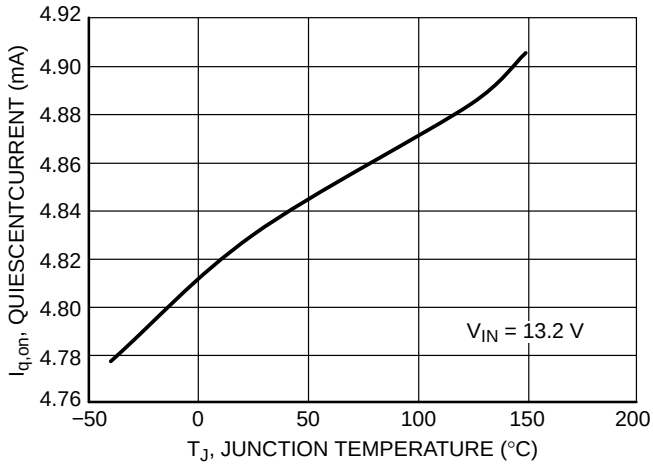


Figure 4. Quiescent Current vs. Temperature

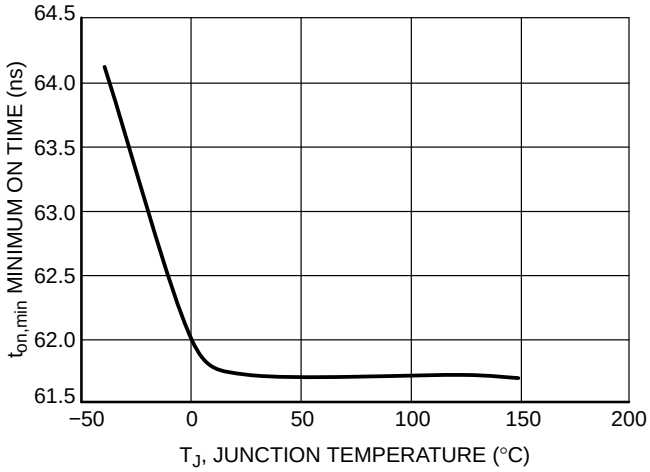


Figure 5. Minimum On Time vs. Temperature

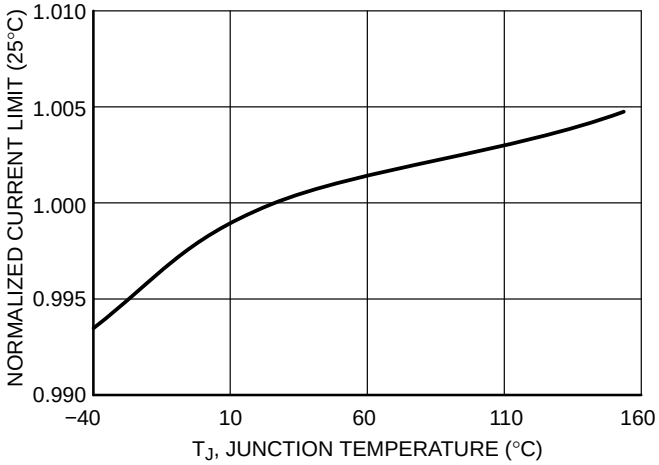


Figure 6. Normalized Current Limit vs. Temperature

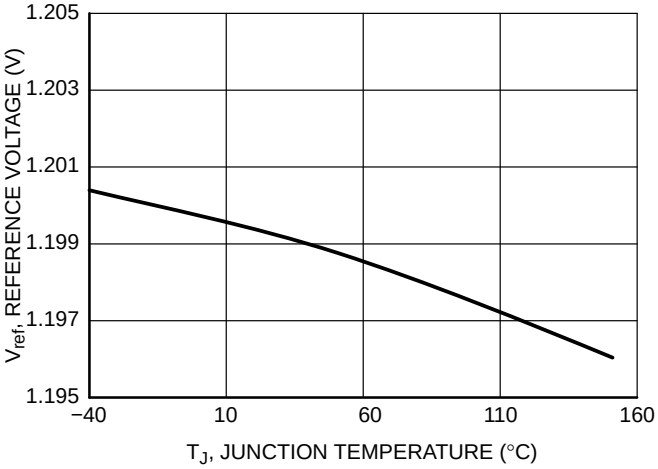


Figure 7. Reference Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

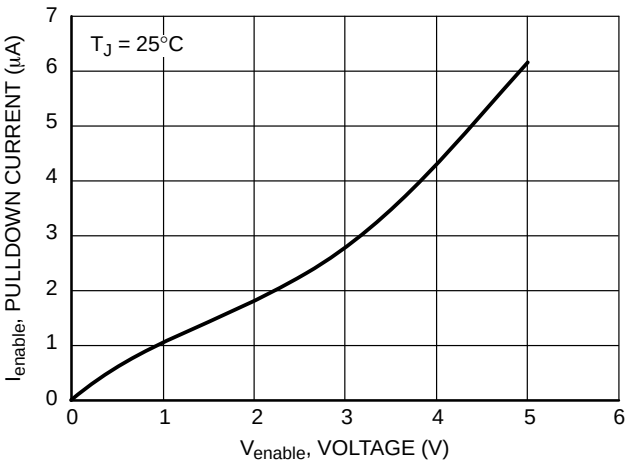


Figure 8. Enable Pulldown Current vs. Voltage

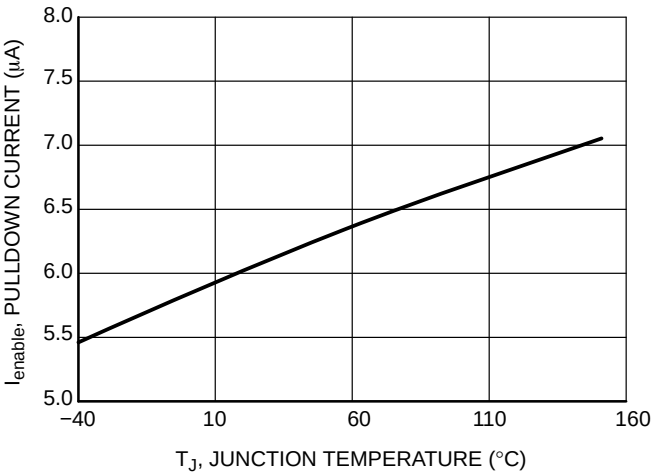


Figure 9. Enable Pulldown Current vs. Temperature

APPLICATION INFORMATION

Current Mode Control

The NCV898031 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

The NCV898031 also includes a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Current Limit

The NCV898031 features two current limit protections, peak current mode and over current latch off. When the current sense amplifier detects a voltage above the peak current limit between ISNS and GND after the current limit leading edge blanking time, the peak current limit causes the power switch to turn off for the remainder of the cycle. Set the current limit with a resistor from ISNS to GND, with $R = V_{CL} / I_{limit}$.

If the voltage across the current sense resistor exceeds the over current threshold voltage, the device enters over current hiccup mode. The device will remain off for the hiccup time and then go through the soft−start procedure.

Short Circuit Protection

If the short circuit enable bit is set (SCE = Y), the device will attempt to protect the power MOSFET from damage. When the output voltage falls below the short circuit trip voltage, after the initial short circuit blanking time, the device enters short circuit latch−off. The device will remain off for the hiccup time and then go through the soft−start.

Enable

The Enable pin has two modes. When a DC logic high (CMOS/TTL compatible) voltage is applied to this pin, the NCV898031 operates at the programmed frequency. When a DC logic low voltage is applied, the NCV898031 enters a low quiescent current sleep mode. The NCV898031 requires 2 clock cycles after the falling edge of the Enable signal to stop switching.

UVLO

Input Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VIN is too low to support the internal rails and power the controller. The IC will start up when enabled and VIN surpasses the UVLO threshold plus the UVLO hysteresis and will shut down when VIN drops below the UVLO threshold or the part is disabled.

Internal Soft-Start

To insure moderate inrush current and reduce output overshoot, the NCV898031 features a soft start which charges a capacitor with a fixed current to ramp up the reference voltage.

VDRV

An internal regulator provides the drive voltage for the gate driver. Bypass with a ceramic capacitor to ground to ensure fast turn on times. The capacitor should be between 0.1 μF and 1 μF, depending on switching speed and charge requirements of the external MOSFET.

SEPIC TOPOLOGY APPLICATION INFORMATION

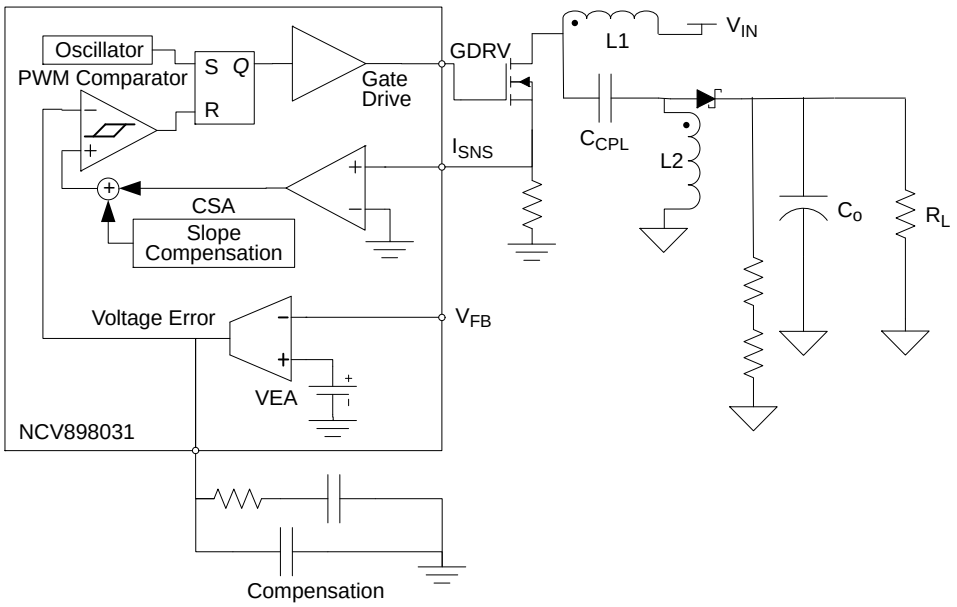


Figure 10. SEPIC Current Mode Schematic

SEPIC Design Methodology

This section details an overview of the component selection process for the NCV898031 in continuous conduction mode SEPIC. It is intended to assist with the design process but does not remove all engineering design work. Many of the equations make heavy use of the small ripple approximation. This process entails the following steps:

1. Define Operational Parameters
2. Select Current Sense Resistor
3. Select SEPIC Inductors
4. Select Coupling Capacitor
5. Select Output Capacitors
6. Select Input Capacitors
7. Select Feedback Resistors
8. Select Compensator Components
9. Select MOSFET(s)
10. Select Diode

Define Operational Parameters

Before beginning the design, define the operating parameters of the application. These include:

$V_{IN(min)}$: minimum input voltage [V]
$V_{IN(max)}$: maximum input voltage [V]
V_{OUT}: output voltage [V]
$I_{OUT(max)}$: maximum output current [A]
I_{CL}: desired typical cycle−by−cycle current limit [A]

From this the ideal minimum and maximum duty cycles can be calculated as follows:

$$D_{min} = \frac{V_{OUT}}{V_{IN(max)} + V_{OUT}}$$

$$D_{max} = \frac{V_{OUT}}{V_{IN(min)} + V_{OUT}}$$

Both duty cycles will actually be higher due to power loss in the conversion. The exact duty cycles will depend on conduction and switching losses.

If the calculated D_{WC} (worst case) is higher than the D_{max} limit of the NCV898031, the conversion will not be possible. It is important for a SEPIC converter to have a restricted D_{max}, because while the ideal conversion ratio of a SEPIC converter goes up to infinity as D approaches 1, a real converter's conversion ratio starts to decrease as losses overtake the increased power transfer. If the converter is in this range it will not be able to regulate properly.

If the following equation is not satisfied, the device will skip pulses at high V_{IN}:

$$\frac{D_{min}}{f_s} \geq t_{on(min)}$$

Where: f_s: switching frequency [Hz]
$t_{on(min)}$: minimum on time [s]

Select Current Sense Resistor

Current sensing for peak current mode control and current limit relies on the MOSFET current signal, which is measured with a ground referenced amplifier. Note that the I_{CL} equals the sum of the currents from both inductors. The easiest method of generating this signal is to use a current sense resistor from the source of the MOSFET to device ground. The sense resistor should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}}$$

Where: R_S: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desire current limit [A]

Select SEPIC Inductors

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in case of load steps. A good starting point for peak to peak ripple is around 20−40% of the inductor current at the maximum load at the worst case V_{IN}, but operation should be verified empirically. The worst case V_{IN} is the minimum input voltage. After choosing a peak current ripple value, calculate the inductor value as follows:

$$L = \frac{V_{IN(WC)}\, D_{WC}}{\Delta I_{L,max}\, f_s}$$

Where: $V_{IN(WC)}$: V_{IN} value as close as possible to half of V_{OUT} [V]
D_{WC}: duty cycle at $V_{IN(WC)}$
$\Delta I_{L,max}$: maximum peak to peak ripple [A]

The maximum average inductor current can be calculated as follows:

$$I_{L,AVG} = \frac{V_{OUT}\, I_{OUT(max)}}{V_{IN(min)}\eta}$$

The Peak Inductor current can be calculated as follows:

$$I_{L1,peak} = I_{L1,avg} + \frac{\Delta I_{L1}}{2}$$

$$I_{L2,peak} = I_{OUT(max)} + \frac{\Delta I_{L2}}{2}$$

Where (if L1 = L2): $\Delta I_{L1} = \Delta I_{L2}$

Select Coupling Capacitor

Coupling capacitor RMS current is significant. A low ESR ceramic capacitor is required as a coupling capacitor. Selecting a capacitor value too low will result in high capacitor ripple voltage which will distort ripple current and diminish input line regulation capability. Budgeting 2−5% coupling capacitor ripple voltage is a reasonable guideline.

$$\Delta V_{coupling} = \frac{I_{out}\, D_{WC}}{C_{coupling}\, f_s}$$

Current mode control helps resolve some of the resonant frequencies that create issues in voltage mode SEPIC converter designs, but some resonance issues may occur. A resonant frequency exists at

$$f_{resonance} = \frac{1}{2\pi\sqrt{(L1 + L2)C_{coupling}}}$$

It may become necessary to place an RC damping network in parallel with the coupling capacitor if the resonance is within ~1 decade of the closed−loop crossover frequency. The capacitance of the damping capacitor should be ~5 times that of the coupling capacitor. The optimal damping resistance (including the ESR of the damping capacitor) is calculated as

$$R_{damping} = \sqrt{\frac{L1 + L2}{C_{coupling}}}$$

Select Output Capacitors

The output capacitors smooth the output voltage and reduce the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{I_{OUT(max)} D_{WC}}{C_{OUT}\, f_s} + \left(\frac{I_{OUT(max)}}{1 - D_{WC}} + \frac{D_{WC} V_{IN(min)}}{2\, f_s L_2}\right) R_{esr}$$

The capacitors need to survive an RMS ripple current as follows:

$$I_{Cout(RMS)} = \sqrt{I_{OUT(max)}{}^2\, D_{WC} + \left(I_a^2 + \frac{I_r^2}{3} - I_a I_r\right) D'_{WC}}$$

where

$$I_a = I_{L1\_peak} + I_{L2\_peak} - I_{L1\_peak}$$

$$I_r = \Delta I_{L1} + \Delta I_{L2}$$

The use of parallel ceramic bypass capacitors is strongly encouraged to help with the transient response.

Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \frac{\Delta I_{L1}}{\sqrt{12}}$$

Select Feedback Resistors

The feedback resistors form a resistor divider from the output of the converter to ground, with a tap to the feedback pin. During regulation, the divided voltage will equal V_{ref}. The lower feedback resistor can be chosen, and the upper feedback resistor value is calculated as follows:

$$R_{upper} = R_{lower}\frac{(V_{out} - V_{ref})}{V_{ref}}$$

The total feedback resistance ($R_{upper} + R_{lower}$) should be in the range of 1 kΩ – 100 kΩ.

Select Compensator Components

Current Mode control method employed by the NCV898031 allows the use of a simple, Type II compensation to optimize the dynamic response according to system requirements.

The maximum RMS Current can be calculated as follows:

$$I_{D(max)} = \sqrt{D_{WC}\left(I_{Q(peak)}{}^2 + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3} - I_{Q(peak)}\left(\Delta I_{L1} + \Delta I_{L2}\right) \right)}$$

where

$$I_{Q(peak)} = I_{L1\_peak} + I_{L2\_peak}$$

The maximum voltage across the MOSFET will be the maximum output voltage, which is the higher of the maximum input voltage and the regulated output voltaged:

$$V_{Q(max)} = V_{OUT(max)} + V_{IN(max)}$$

Select MOSFET(s)

In order to ensure the gate drive voltage does not drop out the MOSFET(s) chosen must not violate the following inequality:

$$Q_{g(total)} \leq \frac{I_{drv}}{f_s}$$

Where: $Q_{g(total)}$: Total Gate Charge of MOSFET(s) [C]
I_{drv}: Drive voltage current [A]
f_s: Switching Frequency [Hz]

Select Diode

The output diode rectifies the output current. The average current through diode will be equal to the output current:

$$I_{D(avg)} = I_{OUT(max)}$$

Additionally, the diode must block voltage equal to the higher of the output voltage and the maximum input voltage:

$$V_{D(max)} = V_{OUT(max)} + V_{IN(max)}$$

The maximum power dissipation in the diode can be calculated as follows:

$$P_D = V_{f(max)}\, I_{OUT(max)}$$

Where: P_d: Power dissipation in the diode [W]
$V_{f(max)}$: Maximum forward voltage of the diode [V]

BOOST TOPOLOGY APPLICATION INFORMATION

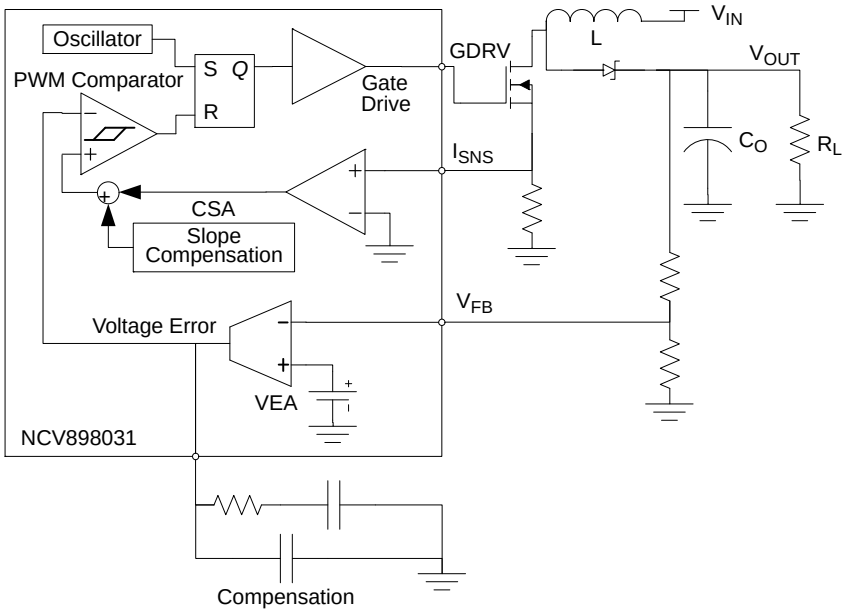


Figure 11. Boost Current Mode Schematic

Design Methodology

This section details an overview of the component selection process for the NCV898031 in continuous conduction mode boost. It is intended to assist with the design process but does not remove all engineering design work. Many of the equations make heavy use of the small ripple approximation. This process entails the following steps:

1. Define Operational Parameters
2. Select Current Sense Resistor
3. Select Output Inductor
4. Select Output Capacitors
5. Select Input Capacitors
6. Select Feedback Resistors
7. Select Compensator Components
8. Select MOSFET(s)
9. Select Diode

Define Operational Parameters

Before beginning the design, define the operating parameters of the application. These include:

$V_{IN(min)}$: minimum input voltage [V]
$V_{IN(max)}$: maximum input voltage [V]
V_{OUT}: output voltage [V]
$I_{OUT(max)}$: maximum output current [A]
I_{CL}: desired typical cycle−by−cycle current limit [A]

From this the ideal minimum and maximum duty cycles can be calculated as follows:

$$D_{min} = 1 - \frac{V_{IN(max)}}{V_{OUT}}$$

$$D_{WC} = 1 - \frac{V_{IN(WC)}}{V_{OUT}}$$

Both duty cycles will actually be higher due to power loss in the conversion. The exact duty cycles will depend on conduction and switching losses. If the maximum input voltage is higher than the output voltage, the minimum duty cycle will be negative. This is because a boost converter cannot have an output lower than the input. In situations where the input is higher than the output, the output will follow the input, minus the diode drop of the output diode and the converter will not attempt to switch.

If the calculated D_{WC} is higher than the D_{max} limit of the NCV898031, the conversion will not be possible. It is important for a boost converter to have a restricted D_{max}, because while the ideal conversion ratio of a boost converter goes up to infinity as D approaches 1, a real converter's conversion ratio starts to decrease as losses overtake the increased power transfer. If the converter is in this range it will not be able to regulate properly.

If the following equation is not satisfied, the device will skip pulses at high V_{IN}:

$$\frac{D_{min}}{f_s} \geq t_{on(min)}$$

Where: f_s: switching frequency [Hz]
$t_{on(min)}$: minimum on time [s]

Select Current Sense Resistor

Current sensing for peak current mode control and current limit relies on the MOSFET current signal, which is measured with a ground referenced amplifier. The easiest method of generating this signal is to use a current sense resistor from the source of the MOSFET to device ground. The sense resistor should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}}$$

Where: R_S: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desire current limit [A]

Select Output Inductor

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in case of load steps. A good starting point for peak to peak ripple is around 20−40% of the inductor current at the maximum load at the worst case V_{IN}, but operation should be verified empirically. The worst case V_{IN} is half of V_{OUT}, or whatever V_{IN} is closest to half of V_{IN}. After choosing a peak current ripple value, calculate the inductor value as follows:

$$L = \frac{V_{IN(WC)}{}^2 D_{WC}}{\Delta I_{L,max} f_s V_{OUT}}$$

Where: $V_{IN(WC)}$: V_{IN} value as close as possible to half of V_{OUT} [V]
D_{WC}: duty cycle at $V_{IN(WC)}$
$\Delta I_{L,max}$: maximum peak to peak ripple [A]

The maximum average inductor current can be calculated as follows:

$$I_{L,avg} = \frac{V_{OUT} I_{OUT(max)}}{V_{IN(min)}}$$

The Peak Inductor current can be calculated as follows:

$$I_{L,peak} = I_{L,avg} + \frac{V_{IN(min)}{}^2 D_{WC}}{L f_s V_{OUT}}$$

Where: $I_{L,peak}$: Peak inductor current value [A]

Select Output Capacitors

The output capacitors smooth the output voltage and reduce the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{I_{OUT(max)}(V_{OUT} - V_{IN(WC)})}{C_{OUT} f} + \frac{I_{OUT(max)} V_{OUT} R_{ESR}}{V_{IN(WC)}}$$

The capacitors need to survive an RMS ripple current as follows:

$$I_{Cout(RMS)} = I_{OUT} \sqrt{\frac{D_{WC}}{D'_{WC}} + \frac{D_{WC}}{12} \left(\frac{D'_{WC}}{\frac{L}{R_{OUT} \times T_{SW}}} \right)^2}$$

The use of parallel ceramic bypass capacitors is strongly encouraged to help with the transient response.

Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \frac{V_{IN(WC)}{}^2 D_{WC}}{L f_s V_{OUT} 2\sqrt{3}}$$

Select Feedback Resistors

The feedback resistors form a resistor divider from the output of the converter to ground, with a tap to the feedback pin. During regulation, the divided voltage will equal V_{ref}. The lower feedback resistor can be chosen, and the upper feedback resistor value is calculated as follows:

$$R_{upper} = R_{lower} \frac{(V_{out} - V_{ref})}{V_{ref}}$$

The total feedback resistance ($R_{upper} + R_{lower}$) should be in the range of 1 kΩ – 100 kΩ.

Select Compensator Components

Current Mode control method employed by the NCV898031 allows the use of a simple, Type II compensation to optimize the dynamic response according to system requirements.

Select MOSFET(s)

In order to ensure the gate drive voltage does not drop out the MOSFET(s) chosen must not violate the following inequality:

$$Q_{g(total)} \leq \frac{I_{drv}}{f_s}$$

Where: $Q_{g(total)}$: Total Gate Charge of MOSFET(s) [C]
I_{drv}: Drive voltage current [A]
f_s: Switching Frequency [Hz]

The maximum RMS Current can be calculated as follows:

$$I_{D(max)} = I_{out} \frac{\sqrt{D_{WC}}}{D'_{WC}}$$

The maximum voltage across the MOSFET will be the maximum output voltage, which is the higher of the maximum input voltage and the regulated output voltaged:

$$V_{Q(max)} = V_{OUT(WC)}$$

Select Diode

The output diode rectifies the output current. The average current through diode will be equal to the output current:

$$I_{D(avg)} = I_{OUT(max)}$$

Additionally, the diode must block voltage equal to the higher of the output voltage and the maximum input voltage:

$$V_{D(max)} = V_{OUT(max)}$$

The maximum power dissipation in the diode can be calculated as follows:

$$P_D = V_{f(max)} I_{OUT(max)}$$

Where: P_d: Power dissipation in the diode [W]

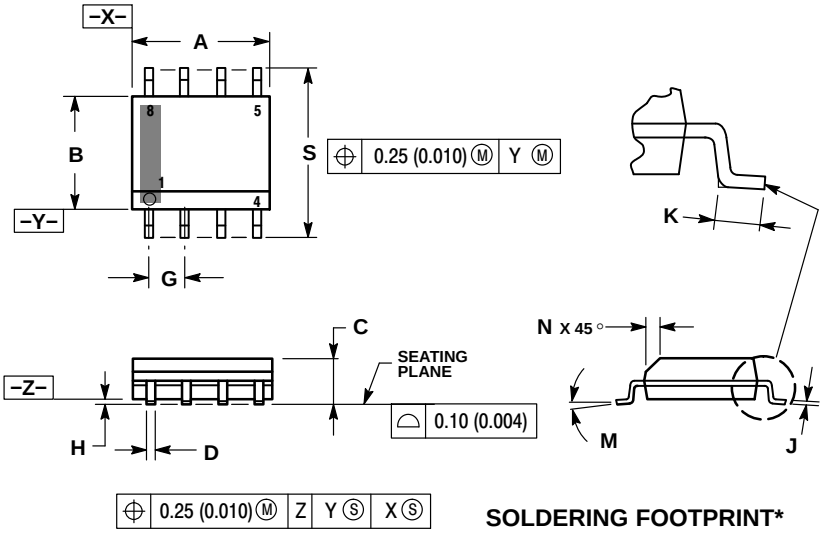
$V_{f(max)}$: Maximum forward voltage of the diode [V]

Low Voltage Operation

If the input voltage drops below the UVLO or MOSFET threshold voltage, another voltage may be used to power the device. Simply connect the voltage you would like to boost to the inductor and connect the stable voltage to the VIN pin of the device. In boost configuration, the output of the converter can be used to power the device. In some cases it may be desirable to connect 2 sources to VIN pin, which can be accomplished simply by connecting each of the sources through a diode to the VIN pin.

PACKAGE DIMENSIONS

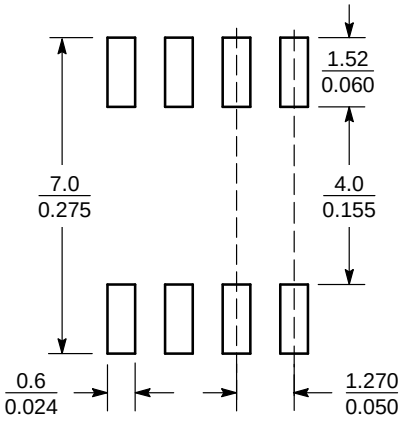
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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