

# Very Low Noise, High-Speed, 12V CMOS Operational Amplifier

## FEATURES

- **BANDWIDTH: 20MHz**
- **SLEW RATE: 30V/μs**
- **FAST 16-BIT SETTling TIME**
- **LOW NOISE: 6nV/√Hz (typ) at 100kHz**
- **EXCELLENT CMRR, PSRR, and A<sub>OL</sub>**
- **RAIL-TO-RAIL OUTPUT**
- **CM RANGE INCLUDES GND**
- **THD+N: 0.0003% (typ) at 1kHz**
- **QUIESCENT CURRENT: 5.5mA/ch (max)**
- **SUPPLY VOLTAGE: 4V to 12V**
- **SHUTDOWN MODE (OPAx726): 6μA/ch**

## APPLICATIONS

- **OPTICAL NETWORKING**
- **TRANSIMPEDANCE AMPLIFIERS**
- **INTEGRATORS**
- **ACTIVE FILTERS**
- **A/D CONVERTER BUFFERS**
- **I/V CONVERTER FOR DACs**
- **PORTABLE AUDIO**
- **PROCESS CONTROL**
- **TEST EQUIPMENT**

## OPA725 RELATED PRODUCTS

FEATURES	PRODUCT
10MHz, 16V, 16V/μs, 8.5nV/√Hz at 1kHz	TLC080
8MHz, 36V, FET Input, 20V/μs, 8.5nV/√Hz at 1kHz	OPA132
100MHz, 5.5V, Precision Transimpedance Amplifier	OPA380
500MHz, ±5V, FET Input, 290V/μs, 7nV/√Hz at 100kHz	OPA656
7MHz, 12V, RRIO, 10V/μs, 30nV/√Hz at 10kHz	OPA743
16-Bit, 250kSPS, 4-Channel, Parallel Output ADC	ADS8342

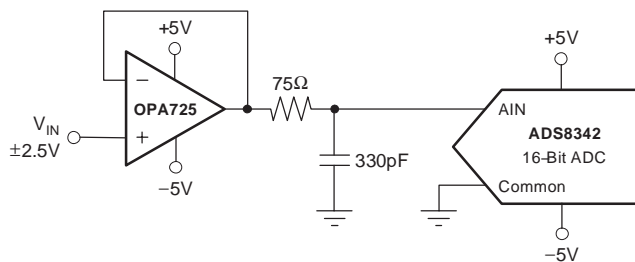
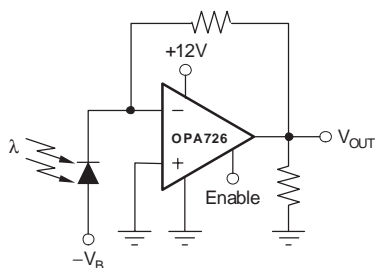
## DESCRIPTION

The OPA725 and OPA726 series op amps use a state-of-the-art 12V analog CMOS process, and combine outstanding ac performance with low bias current and excellent CMRR, PSRR, and A<sub>OL</sub>. The 20MHz Gain-Bandwidth (GBW) Product is achieved by using a proprietary and patent-pending output stage design. These characteristics allow excellent 16-bit settling times for driving 16-bit Analog-to-Digital converters (ADCs).

Excellent ac characteristics, such as 20MHz GBW, 30V/μs slew rate and 0.0003% THD+N make the OPA725 and OPA726 well-suited for communication, high-end audio, and active filter applications. With a bias current of less than 200pA, they are well-suited for use as transimpedance (I/V-conversion) amplifiers for monitoring optical power in ONET applications.

The OPA725 and OPA726 op amps can be used in single-supply applications from 4V up to 12V, or dual-supply from ±2V to ±6V. The output swings to within 150mV of the rails, maximizing dynamic range. The shutdown versions (OPAx726) reduce the quiescent current to less than 6μA and feature a reference pin for easy shutdown operation with standard CMOS logic in dual-supply applications.

The OPA725 (single) is available in SOT23-5 and SO-8 packages, and the OPA2725 (dual) is available in MSOP-8 and SO-8 packages. The OPA726 (single with shutdown) is available in MSOP-8 and SO-8. The OPA2726 (dual with shutdown) is available in MSOP-10. All versions are specified for operation from -40°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

**ORDERING INFORMATION**

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
<b>Non-Shutdown</b>						
OPA725	SOT23-5	DBV	-40°C to +125°C	OALI	OPA725AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA725AIDBVR	Tape and Reel, 3000
OPA725	SO-8	D	-40°C to +125°C	OPA725A	OPA725AID	Rails, 100
"	"	"	"	"	OPA725AIDR	Tape and Reel, 2500
OPA2725	SO-8	D	-40°C to +125°C	OPA2725A	OPA2725AID	Rails, 100
"	"	"	"	"	OPA2725AIDR	Tape and Reel, 2500
OPA2725	MSOP-8	DGK	-40°C to +125°C	BGM	OPA2725AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2725AIDGKR	Tape and Reel, 2500
<b>Shutdown</b>						
OPA726	SO-8	D	-40°C to +125°C	OPA726A	OPA726AID	Rails, 100
"	"	"	"	"	OPA726AIDR	Tape and Reel, 2500
OPA726	MSOP-8	DGK	-40°C to +125°C	BHC	OPA726AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA726AIDGKR	Tape and Reel, 2500
OPA2726	MSOP-10	DGS	-40°C to +125°C	BHB	OPA2726AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2726AIDGSR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

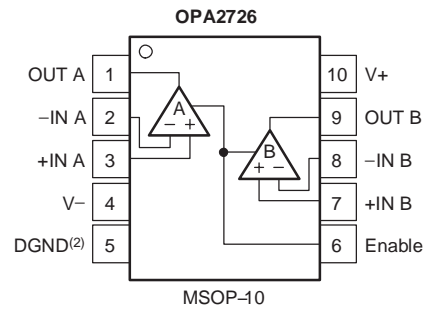
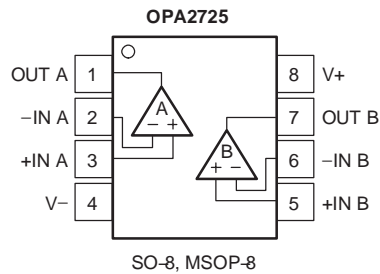
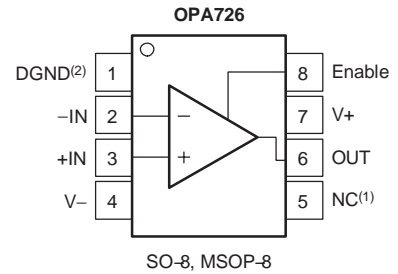
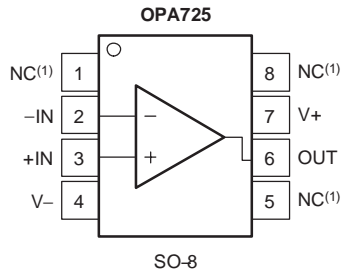
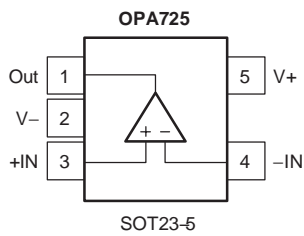
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ABSOLUTE MAXIMUM RATINGS(1)**

Supply Voltage	+13.2V
Signal Input Terminals, Voltage <sup>(2)</sup>	-0.5V to (V+) + 0.5V
Current <sup>(2)</sup>	±10mA
Output Short Circuit <sup>(3)</sup>	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model)	1000 V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

## PIN CONFIGURATIONS



(1) NC denotes no internal connection.

(2) DGND = reference voltage for Enable Reference pin. Voltage on this pin will be the voltage to which the Enable Reference pin is referenced.

**ELECTRICAL CHARACTERISTICS:  $V_S = +4V$  to  $+12V$  or  $V_S = \pm 2V$  to  $\pm 6V$**

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ C$  to  $+125^\circ C$ .

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA725, OPA726, OPA2725, OPA2726			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage $V_{OS}$	$V_S = \pm 6V, V_{CM} = 0V$		1.2	3	mV
OPA725, OPA726	$V_S = \pm 6V, V_{CM} = 0V$		1.5	5	mV
OPA2725, OPA2726			<b>4</b>		$\mu V/^\circ C$
Drift			30	100	$\mu V/V$
vs Power Supply	$V_S = \pm 2V$ to $\pm 6V, V_{CM} = V-$			<b>150</b>	$\mu V/V$
<b>Over Temperature</b>					
Channel Separation, DC			1		$\mu V/V$
<b>INPUT BIAS CURRENT</b>					
Input Bias Current $I_B$			30	200	pA
<b>Over Temperature</b>			See Typical Characteristics		
Input Offset Current $I_{OS}$			10	50	pA
<b>NOISE</b>					
Input Voltage Noise, $f = 0.1Hz$ to $10Hz$	$V_S = \pm 6V, V_{CM} = 0V$		10		$\mu V_{PP}$
Input Voltage Noise Density, $f = 10kHz$	$V_S = \pm 6V, V_{CM} = 0V$		10		$nV/\sqrt{Hz}$
Input Voltage Noise Density, $f = 100kHz$	$V_S = \pm 6V, V_{CM} = 0V$		6		$nV/\sqrt{Hz}$
Input Current Noise Density, $f = 1kHz$	$V_S = \pm 6V, V_{CM} = 0V$		2.5		$fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range $V_{CM}$		(V-)		(V+) - 2	V
Common-Mode Rejection Ratio $CMRR$	$(V-) \leq V_{CM} \leq (V+) - 2V$	88	94		dB
<b>Over Temperature</b>	<b><math>(V-) \leq V_{CM} \leq (V+) - 2V</math></b>	<b>84</b>			<b>dB</b>
	$(V-) \leq V_{CM} \leq (V+) - 3V$	94	100		dB
<b>Over Temperature</b>	<b><math>(V-) \leq V_{CM} \leq (V+) - 3V</math></b>	<b>84</b>			<b>dB</b>
<b>INPUT IMPEDANCE</b>					
Differential			$10^{11}    5$		$\Omega    pF$
Common-Mode			$10^{11}    4$		$\Omega    pF$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain $A_{OL}$					
OPA725, OPA726	$R_L = 100k\Omega, 0.15V < V_O < (V+) - 0.15V$	110	120		dB
<b>Over Temperature</b>	<b><math>R_L = 100k\Omega, 0.15V &lt; V_O &lt; (V+) - 0.15V</math></b>	<b>100</b>			<b>dB</b>
OPA2725, OPA2726	$R_L = 100k\Omega, 0.175V < V_O < (V+) - 0.175V$	110	120		dB
<b>Over Temperature</b>	<b><math>R_L = 100k\Omega, 0.175V &lt; V_O &lt; (V+) - 0.175V</math></b>	<b>100</b>			<b>dB</b>
OPA725, OPA726	$R_L = 1k\Omega, 0.25V < V_O < (V+) - 0.25V$	106	116		dB
<b>Over Temperature</b>	<b><math>R_L = 1k\Omega, 0.25V &lt; V_O &lt; (V+) - 0.25V</math></b>	<b>96</b>			<b>dB</b>
OPA2725, OPA2726	$R_L = 2k\Omega, 0.25V < V_O < (V+) - 0.25V$	106	116		dB
<b>Over Temperature</b>	<b><math>R_L = 2k\Omega, 0.25V &lt; V_O &lt; (V+) - 0.25V</math></b>	<b>96</b>			<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	$C_L = 20pF$				
GBW			20		MHz
Slew Rate	$G = +1$		30		V/ $\mu s$
SR			350		ns
Settling Time, 0.1%	$V_S = \pm 6V, 5V$ Step, $G = +1$		450		ns
0.01%	$V_S = \pm 6V, 5V$ Step, $G = +1$		50		ns
Overload Recovery Time	$V_{IN} \cdot \text{Gain} > V_S$		50		ns
THD+N	$V_S = \pm 6V, V_{OUT} = 2V_{RMS}, R_L = 600\Omega, G = +1, f = 1kHz$		0.0003		%

**ELECTRICAL CHARACTERISTICS:  $V_S = +4V$  to  $+12V$  or  $V_S = \pm 2V$  to  $\pm 6V$  (continued)**

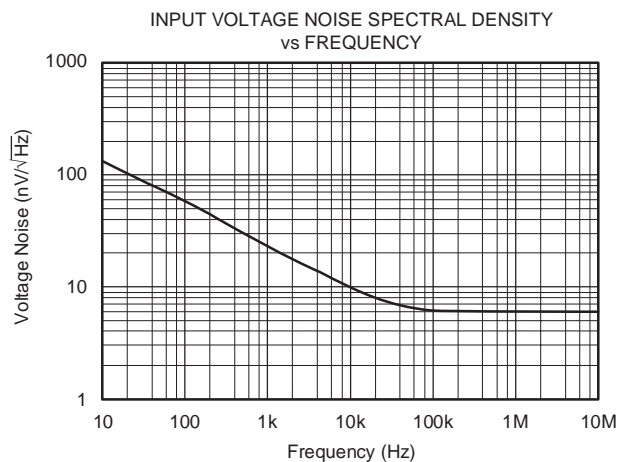
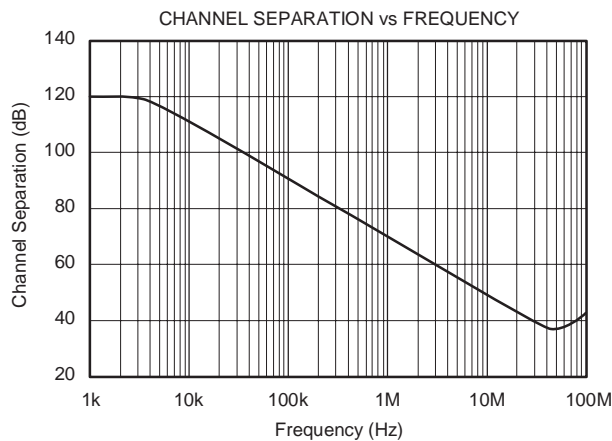
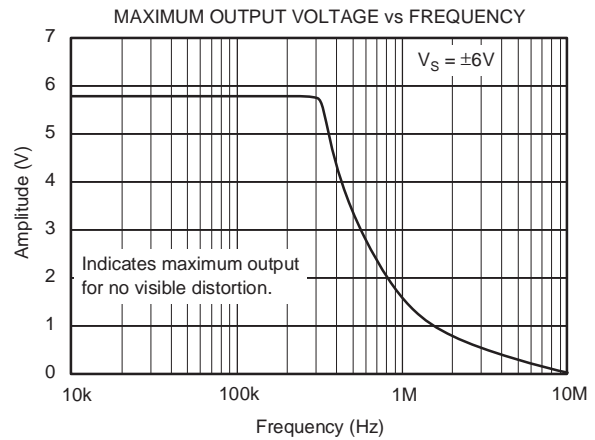
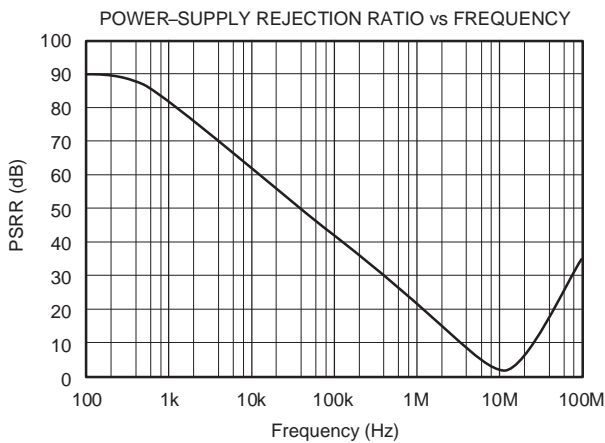
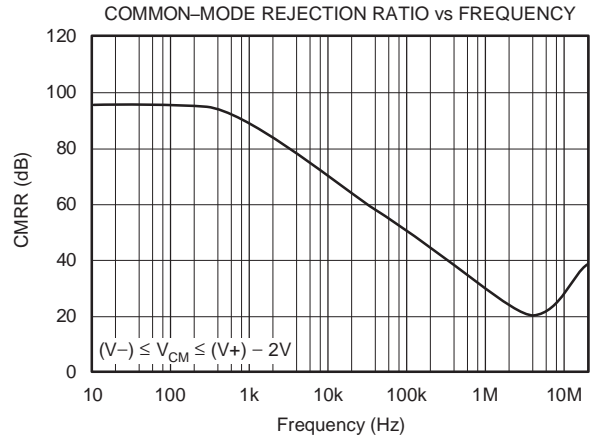
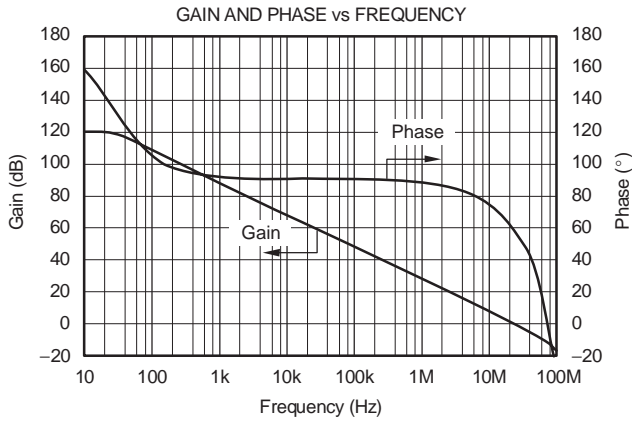
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA725, OPA726, OPA2725, OPA2726			UNIT
		MIN	TYP	MAX	
<b>OUTPUT</b>					
Voltage Output Swing from Rail					
OPA725, OPA726	$R_L = 100\text{k}\Omega$ , $A_{OL} > 110\text{dB}$		100	150	mV
<b>Over Temperature</b>	<b><math>R_L = 100\text{k}\Omega</math>, <math>A_{OL} &gt; 100\text{dB}</math></b>			<b>150</b>	<b>mV</b>
OPA2725, OPA2726	$R_L = 100\text{k}\Omega$ , $A_{OL} > 110\text{dB}$		125	175	mV
<b>Over Temperature</b>	<b><math>R_L = 100\text{k}\Omega</math>, <math>A_{OL} &gt; 100\text{dB}</math></b>			<b>175</b>	<b>mV</b>
OPA725, OPA726	$R_L = 1\text{k}\Omega$ , $A_{OL} > 106\text{dB}$		200	250	mV
<b>Over Temperature</b>	<b><math>R_L = 1\text{k}\Omega</math>, <math>A_{OL} &gt; 96\text{dB}</math></b>			<b>250</b>	<b>mV</b>
OPA2725, OPA2726	$R_L = 2\text{k}\Omega$ , $A_{OL} > 106\text{dB}$		200	250	mV
<b>Over Temperature</b>	<b><math>R_L = 2\text{k}\Omega</math>, <math>A_{OL} &gt; 96\text{dB}</math></b>			<b>250</b>	<b>mV</b>
Output Current	$I_{OUT}$		40		mA
Short-Circuit Current	$I_{SC}$		$\pm 55$		mA
Capacitive Load Drive	$C_{LOAD}$	See Typical Characteristics			
Open-Loop Output Impedance	$f = 1\text{MHz}$ , $I_O = 0$		40		$\Omega$
<b>ENABLE/SHUTDOWN (OPA<sub>x</sub>726)</b>					
$t_{OFF}$			5		$\mu\text{s}$
$t_{ON}$			30		$\mu\text{s}$
Enable Reference (DGND) Voltage Range	$V_{DGND}$	$V^-$		$(V^+) - 2$	V
$V_L$ (shutdown)				$< V_{DGND} + 0.8V$	V
$V_H$ (amplifier is active)		$> V_{DGND} + 2V$			V
Input Disable Current	Ref Pin = Enable Pin = $V^-$		5		$\mu\text{A}$
$I_{QSD}$ (per amplifier)			6	15	$\mu\text{A}$
<b>POWER SUPPLY</b>					
Specified Voltage Range	$V_S$	4		12	V
Operating Voltage Range	$V_S$		3.5 to 13.2		V
Quiescent Current (per amplifier)	$I_Q$		4.3	5.5	mA
<b>Over Temperature</b>				<b>6</b>	<b>mA</b>
<b>TEMPERATURE RANGE</b>					
Specified Range		-40		125	$^\circ\text{C}$
Operating Range		-55		125	$^\circ\text{C}$
Storage Range		-55		150	$^\circ\text{C}$
Thermal Resistance	$\theta_{JA}$				
SOT23-5			200		$^\circ\text{C/W}$
MSOP-8, MSOP-10, SO-8			150		$^\circ\text{C/W}$

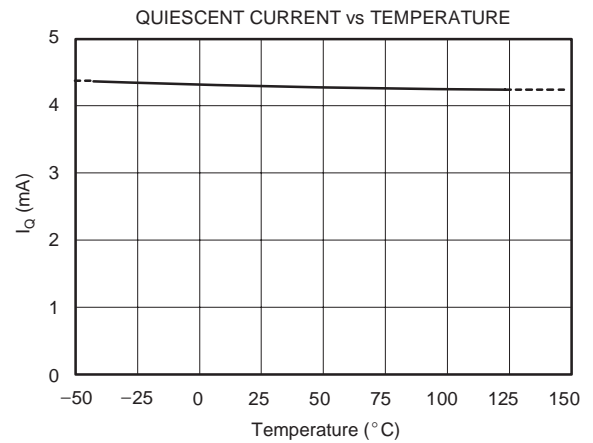
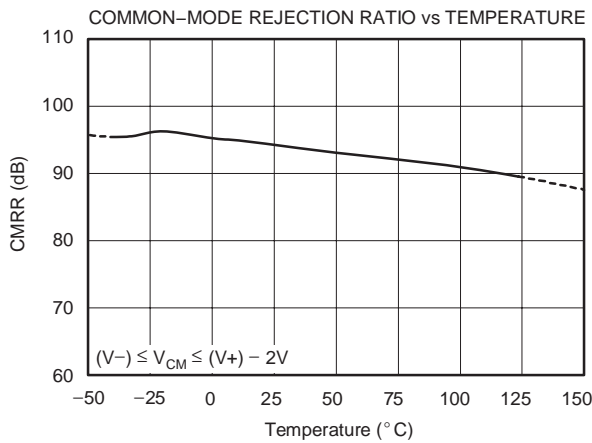
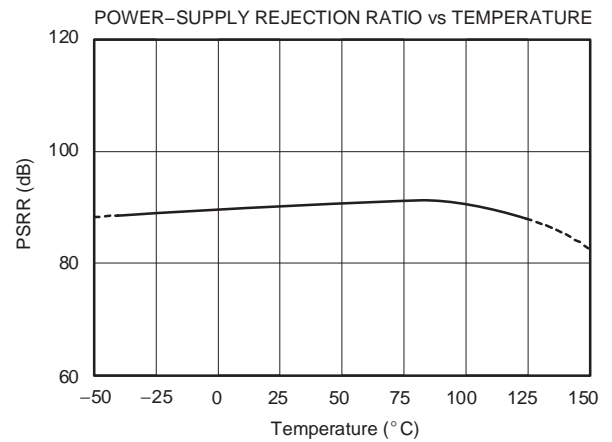
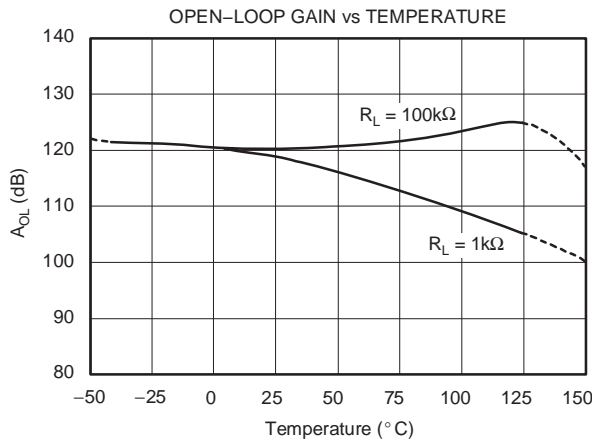
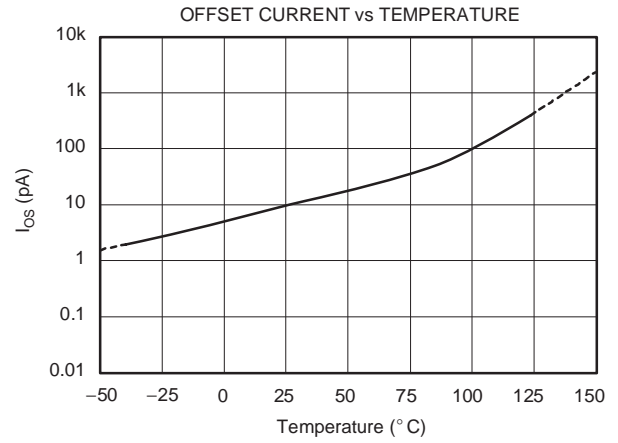
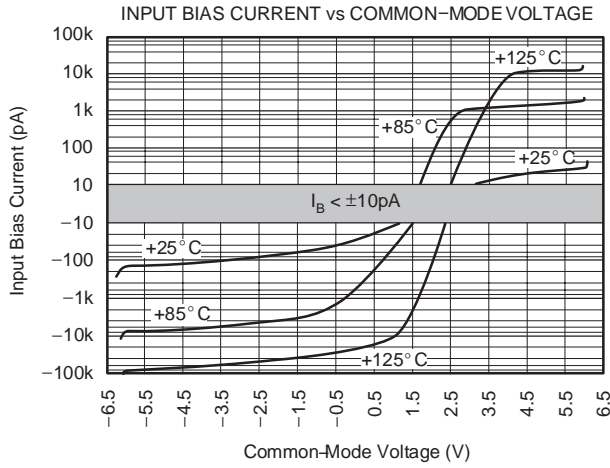
## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



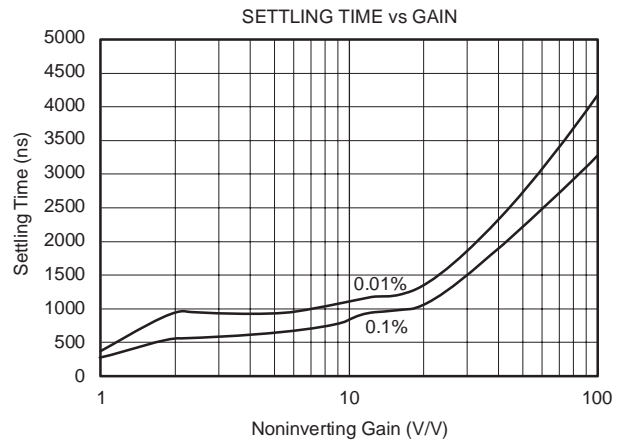
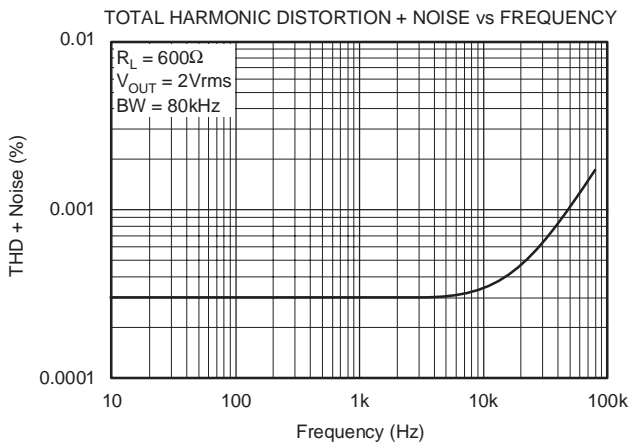
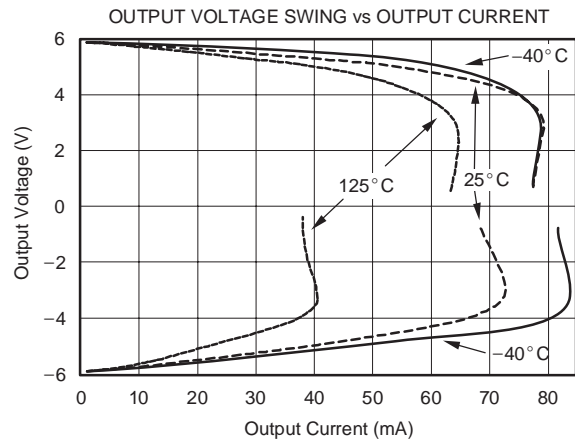
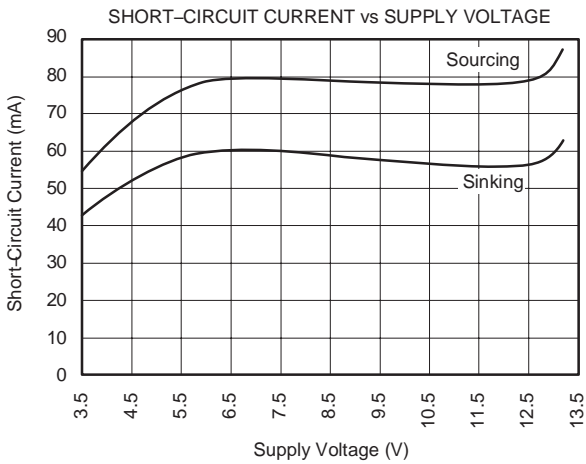
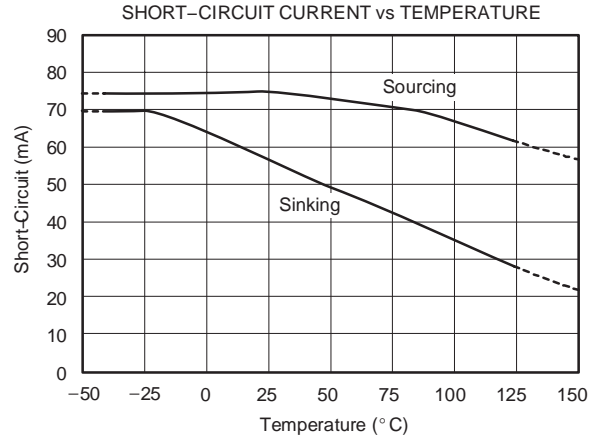
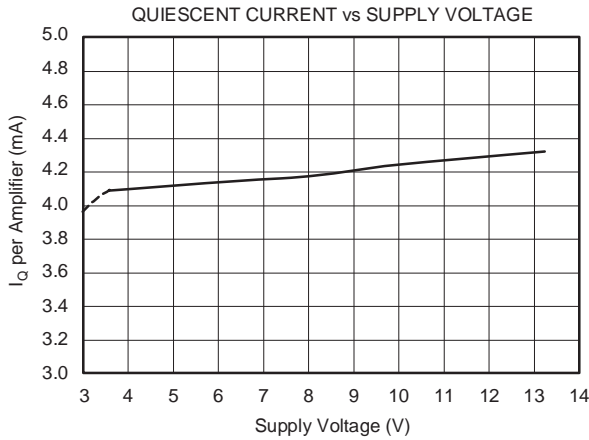
**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**

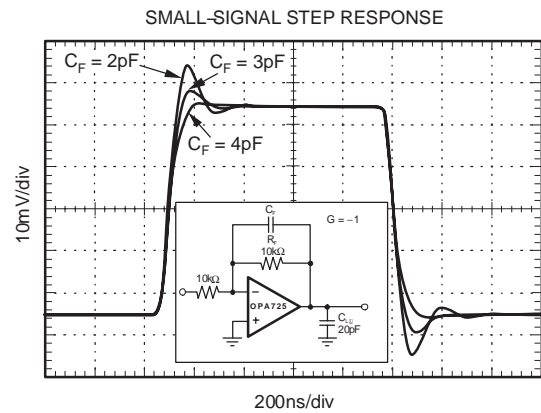
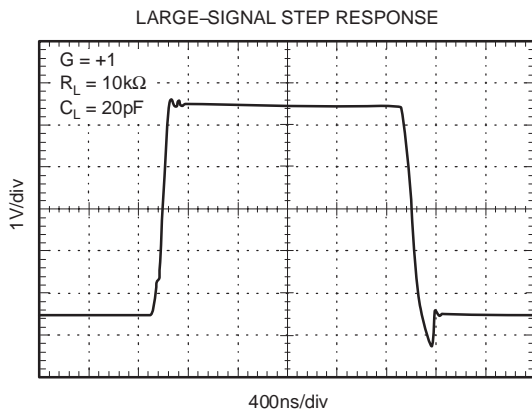
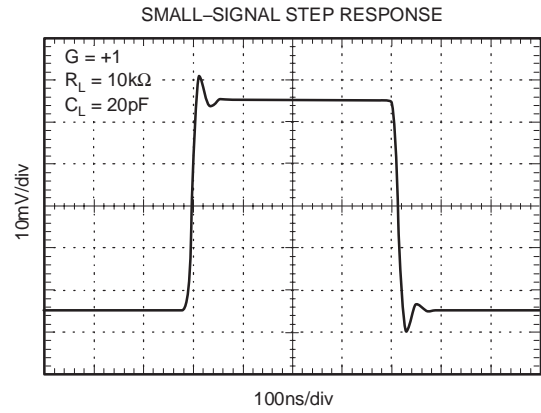
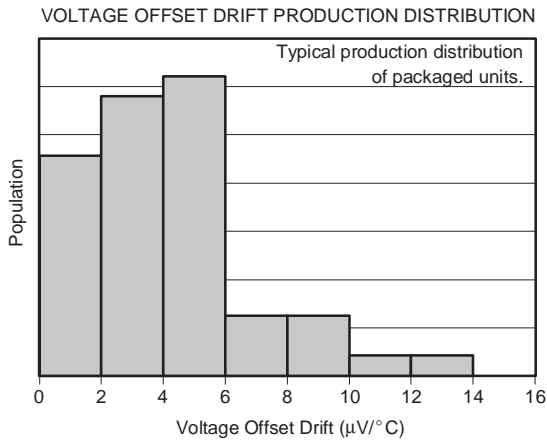
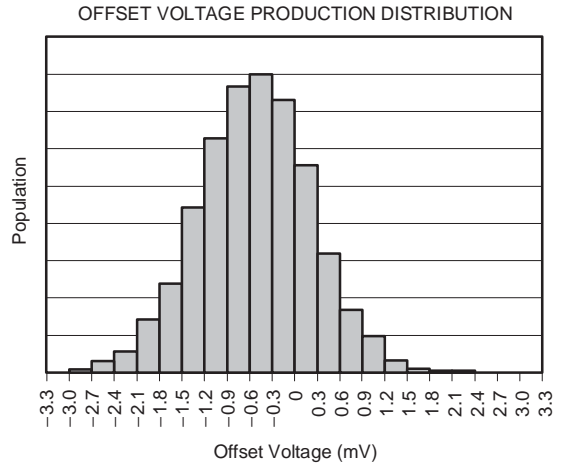
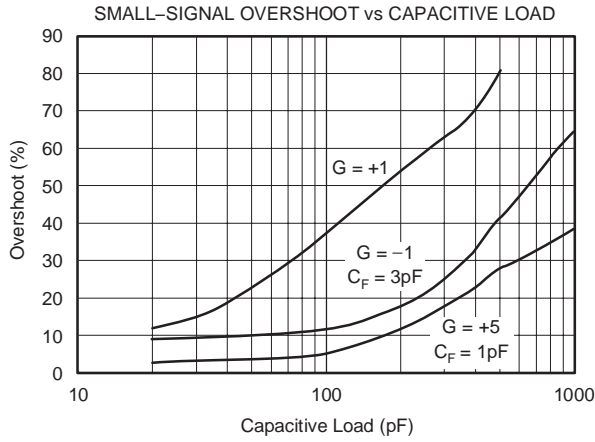
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.





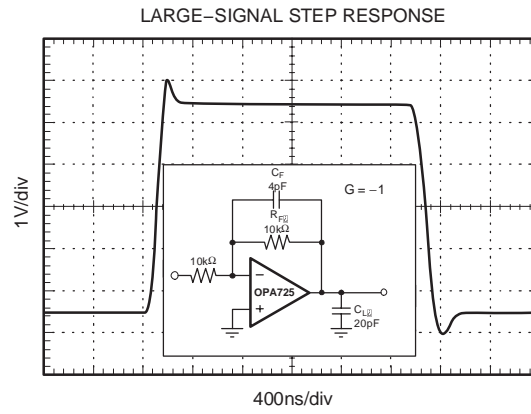
## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



### TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.



## APPLICATIONS INFORMATION

OPA725 and OPA726 series 20MHz CMOS op amps have a fast slew rate, low noise, and excellent PSRR, CMRR, and  $A_{OL}$ . These op amps can operate on typically 4.3mA quiescent current from a single (or split) supply in the range of 4V to 12V ( $\pm 2V$  to  $\pm 6V$ ), making them highly versatile and easy to use. They are stable in a unity-gain configuration.

Power-supply pins should be bypassed with 1nF ceramic capacitors in parallel with 1 $\mu$ F tantalum capacitors.

### OPERATING VOLTAGE

OPA725 series op amps are specified from 4V to 12V supplies over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . They will operate well in  $\pm 5V$  or  $+5V$  to  $+12V$  power-supply systems. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

### ENABLE/SHUTDOWN

OPA725 series op amps require approximately 4.3mA quiescent current. The enable/shutdown feature of the OPA726 allows the op amp to be shut off to reduce this current to approximately 6 $\mu$ A.

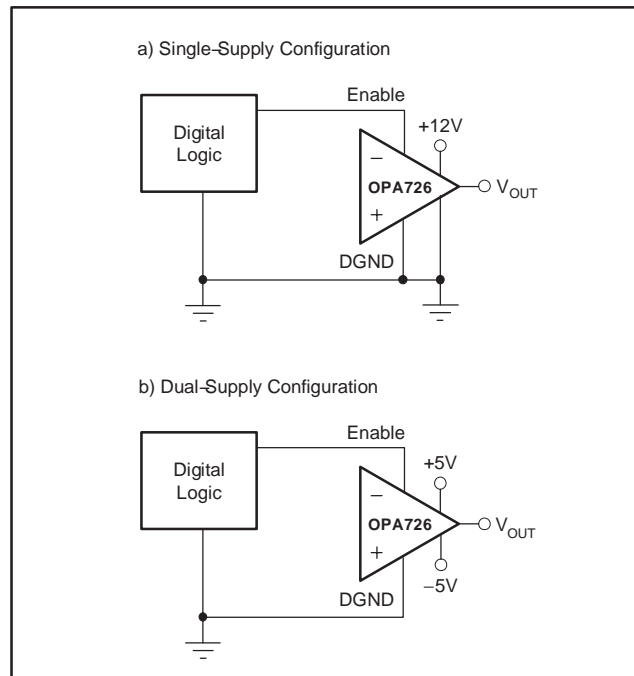
The enable/shutdown input is referenced to the Enable Reference Pin, DGND (see Pin Configurations). This pin can be connected to logic ground in dual-supply op amp configurations to avoid level-shifting the enable logic signal, as shown in Figure 1.

The Enable Reference Pin voltage,  $V_{DGND}$ , must not exceed  $(V+) - 2V$ . It may be set as low as  $V-$ . The amplifier is enabled when the Enable Pin voltage is greater than  $V_{DGND} + 2V$ . The amplifier is disabled (shutdown) if the Enable Pin voltage is less than  $V_{DGND} + 0.8V$ . The Enable Pin is connected to internal pull-up circuitry and will enable the device if left unconnected.

### COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA725 and OPA726 series extends from  $V-$  to  $(V+) - 2V$ .

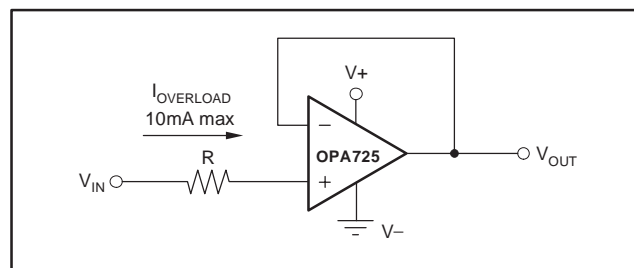
Common-mode rejection is excellent throughout the input voltage range from  $V-$  to  $(V+) - 3V$ . CMRR decreases somewhat as the common-mode voltage extends to  $(V+) - 2V$ , but remains very good and is tested throughout this range. See the Electrical Characteristics table for details.



**Figure 1. Enable Reference Pin Connection for Single- and Dual-Supply Configurations**

### INPUT OVER-VOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current is limited to 10mA. This is easily accomplished with an input resistor in series with the op amp, as shown in Figure 2. The OPA725 series features no phase inversion when the inputs extend beyond supplies, if the input is current limited.



**Figure 2. Input Current Protection for Voltages Exceeding the Supply Voltage**

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving heavy loads connected to any point between  $V+$  and  $V-$ . For light resistive loads ( $> 100\text{k}\Omega$ ), the output voltage can swing to 150mV (175mV for dual) from the supply rail, while still maintaining excellent linearity ( $A_{OL} > 110\text{dB}$ ). With  $1\text{k}\Omega$  ( $2\text{k}\Omega$  for dual) resistive loads, the output is specified to swing to within 250mV from the supply rails with excellent linearity (see the Typical Characteristics curve *Output Voltage Swing vs Output Current*).

## CAPACITIVE LOAD AND STABILITY

Capacitive load drive is dependent upon gain and the overshoot requirements of the application. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see the Typical Characteristics curve *Small-Signal Overshoot vs Capacitive Load*).

One method of improving capacitive load drive in the unity-gain configuration is to insert a  $10\Omega$  to  $20\Omega$  resistor inside the feedback loop, as shown in Figure 3. This reduces ringing with large capacitive loads while maintaining DC accuracy.

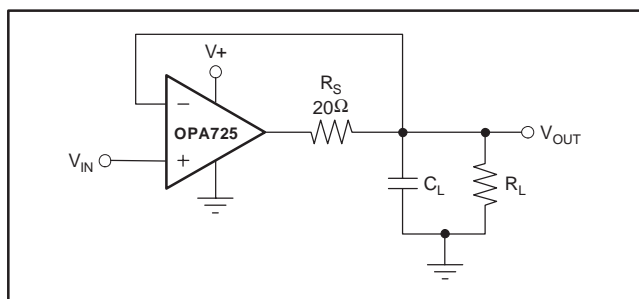


Figure 3. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

## DRIVING FAST 16-BIT ADCs

The OPA725 series is optimized for driving fast 16-bit ADCs such as the ADS8342. The OPA725 op amps buffer the converter input capacitance and resulting charge injection, while providing signal gain. Figure 4 shows the OPA725 in a single-ended method of interfacing to the ADS8342 16-bit, 250kSPS, 4-channel ADC with an input range of  $\pm 2.5\text{V}$ . The OPA725 has demonstrated excellent settling time to the 16-bit level within the 600ns acquisition time of the ADS8342. The RC filter, shown in Figure 4, has been carefully tuned for best noise and settling performance. It may need to be adjusted for different op amp configurations. Please refer to the ADS8342 data sheet (available for download at [www.ti.com](http://www.ti.com)) for additional information on this product.

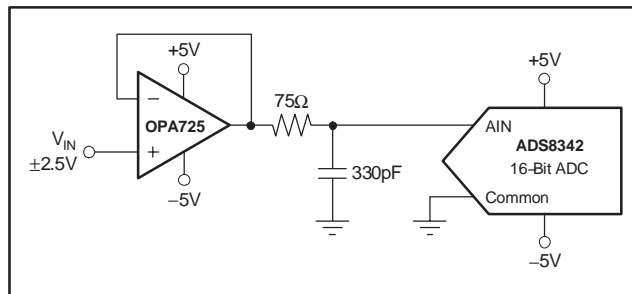


Figure 4. OPA725 Driving an ADC

## TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA725 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 5, are the expected diode capacitance ( $C_D$ ), which should include the parasitic input common-mode and differential-mode input capacitance ( $4\text{pF} + 5\text{pF}$  for the OPA725); the desired transimpedance gain ( $R_F$ ); and the GBW for the OPA725 (20MHz). With these three variables set, the feedback capacitor value ( $C_F$ ) can be set to control the frequency response.  $C_F$  includes the stray capacitance of  $R_F$ , which is  $0.2\text{pF}$  for a typical surface-mount resistor.

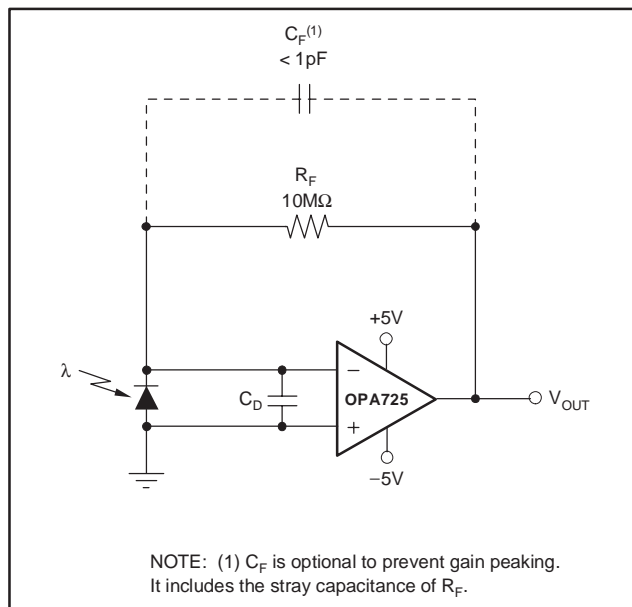


Figure 5. Dual-Supply Transimpedance Amplifier

To achieve a maximally-flat, 2nd-order Butterworth frequency response, the feedback pole should be set to:

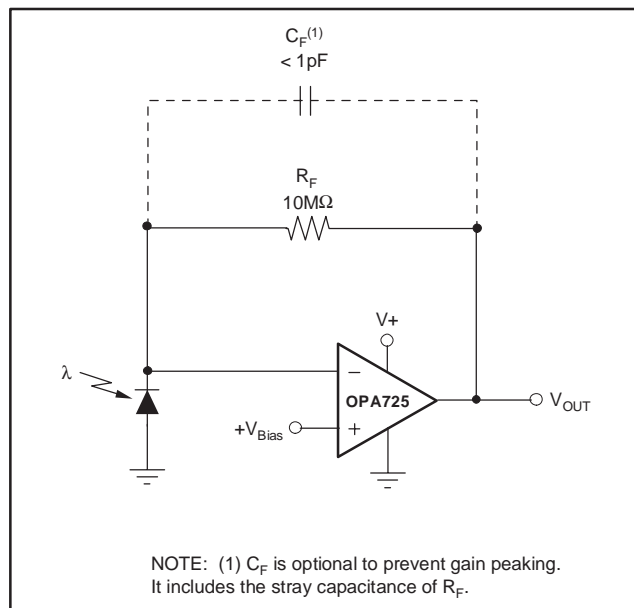
$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \quad (1)$$

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA354 (100MHz GBW), OPA300 (180 MHz GBW), OPA355 (200MHz GBW), or OPA656, OPA657 (400MHz GBW) may be used.

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. (Refer to Figure 6.) This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



**Figure 6. Single-Supply Transimpedance Amplifier**

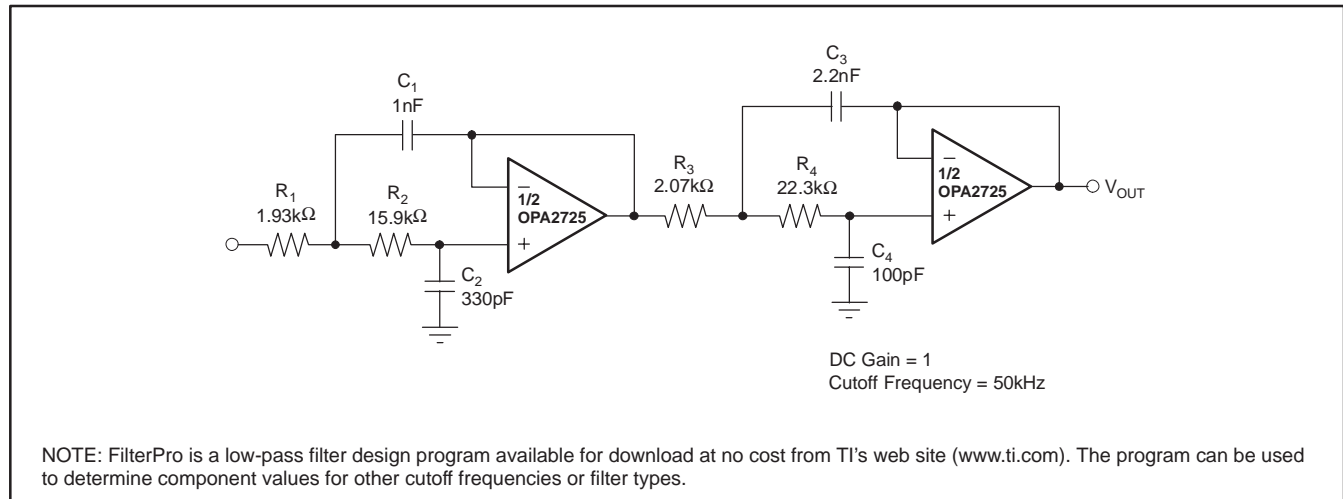
For additional information, refer to Application Bulletin SBOA055, *Compensate Transimpedance Amplifiers Intuitively*, available for download at [www.ti.com](http://www.ti.com).

## OPTIMIZING THE TRANSIMPEDANCE CIRCUIT

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select  $R_F$  to create the total required gain. Using a lower value for  $R_F$  and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by  $R_F$  increases with the square-root of  $R_F$ , whereas the signal increases linearly. Therefore, signal-to-noise ratio is improved when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the  $R_F$  to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the Application Bulletins *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066), available for download at the TI web site.



**Figure 7. Four-Pole Butterworth Sallen-Key Low-Pass Filter**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA2725AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2725AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2726AIDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2726AIDGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2726AIDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2726AIDGSTG4	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA725AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA726AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA726AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2725AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2725AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2725AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2726AIDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA725AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA725AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA725AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA726AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA726AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2725AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA2725AIDGKT	MSOP	DGK	8	250	190.5	212.7	31.8
OPA2725AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA2726AIDGST	MSOP	DGS	10	250	190.5	212.7	31.8
OPA725AIDBVR	SOT-23	DBV	5	3000	190.5	212.7	31.8
OPA725AIDBVT	SOT-23	DBV	5	250	190.5	212.7	31.8
OPA725AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA726AIDGKT	MSOP	DGK	8	250	190.5	212.7	31.8
OPA726AIDR	SOIC	D	8	2500	346.0	346.0	29.0

DBV (R-PDSO-G5)

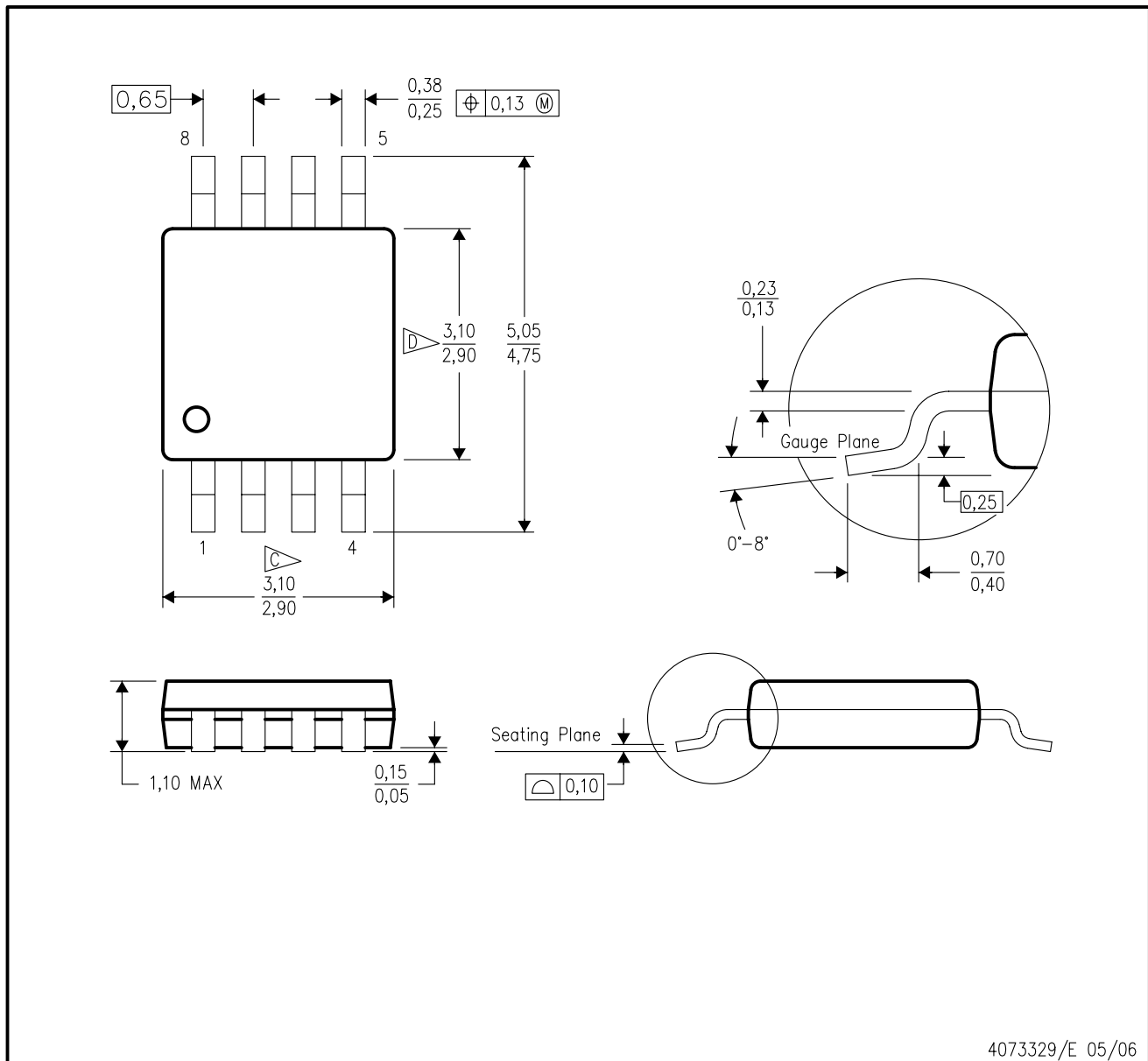
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DGK (S-PDSO-G8)

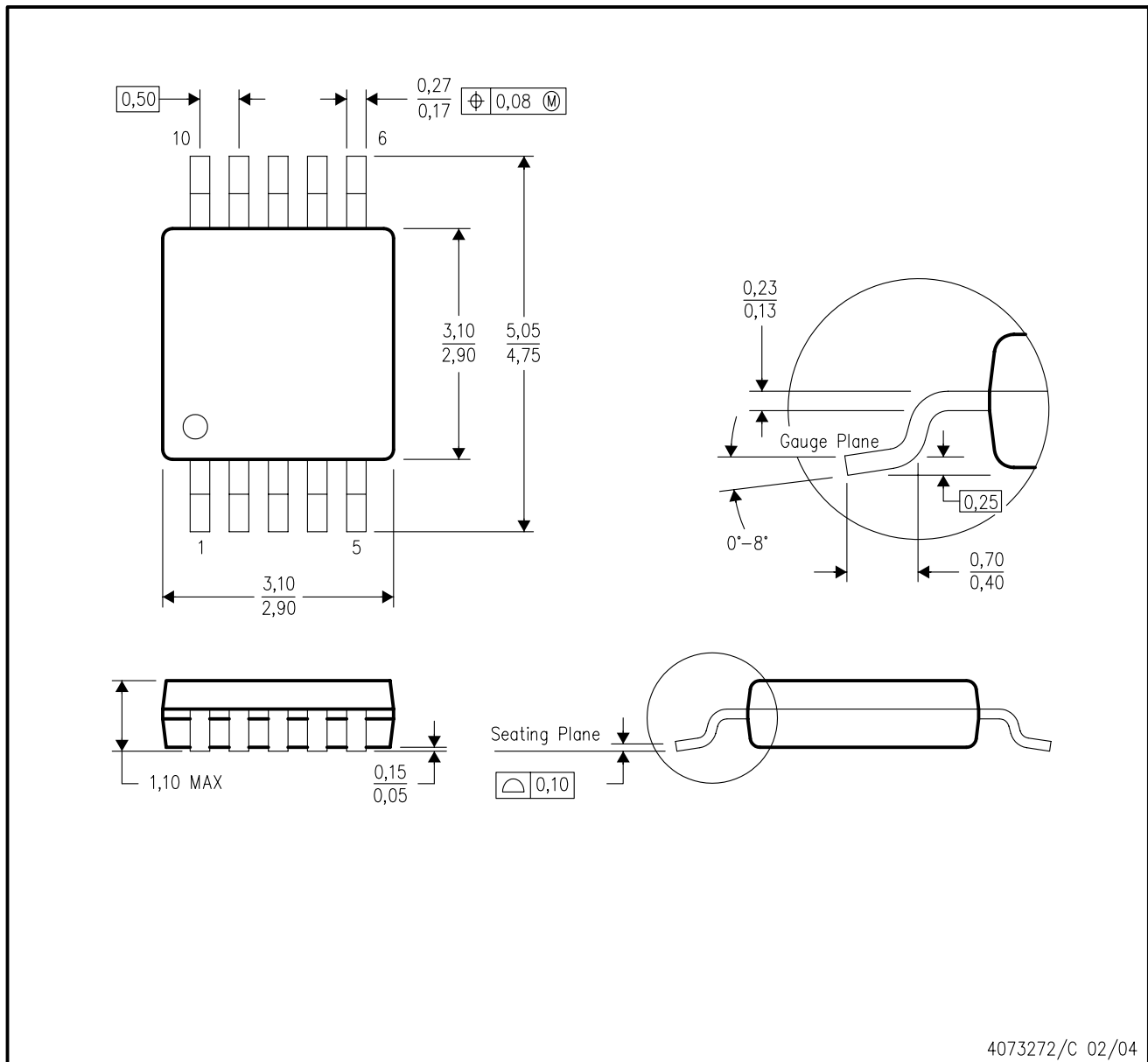
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGS (S-PDSO-G10)

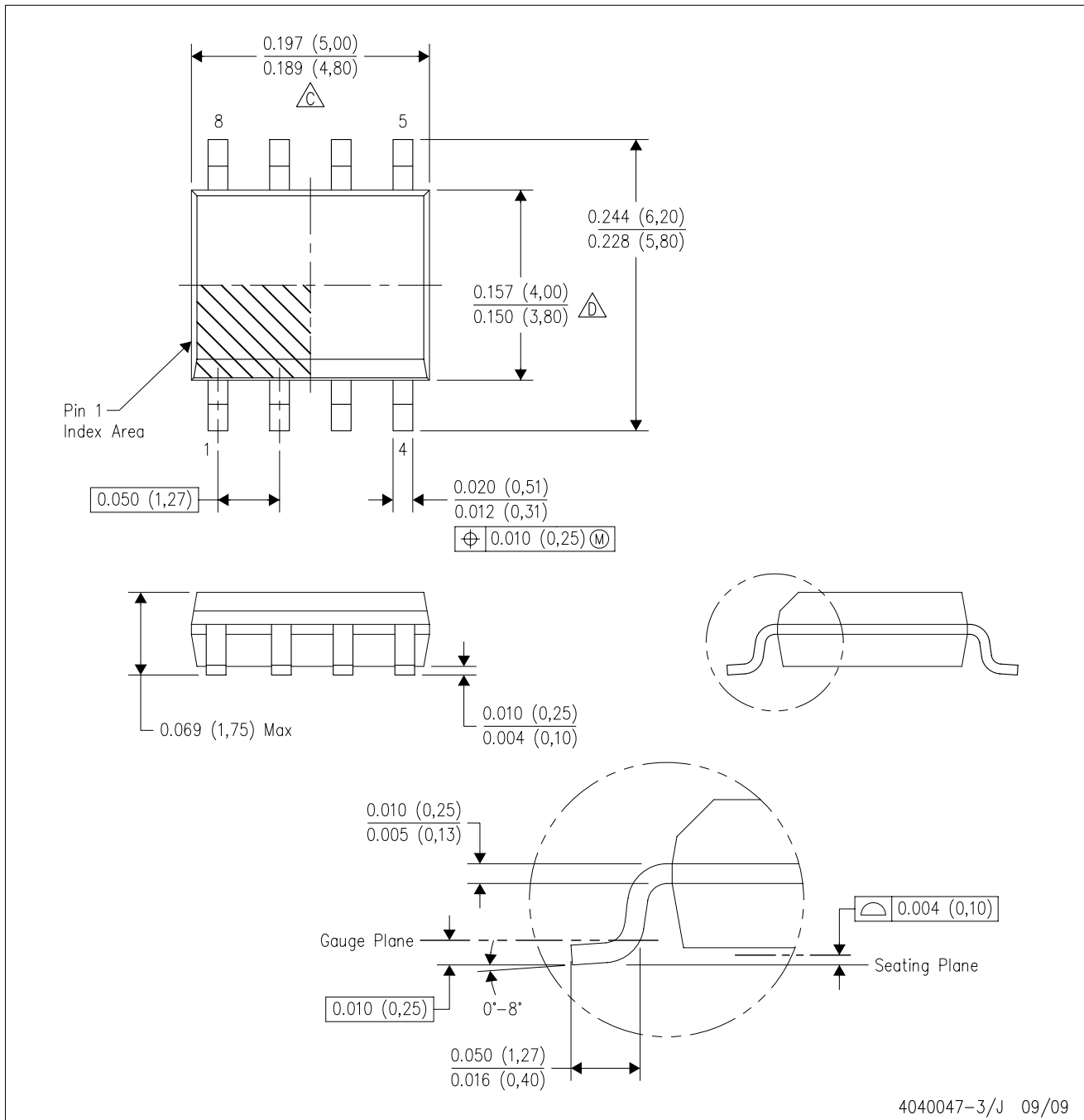
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated