EMC OPTIMIZED CAN TRANSCEIVER

Check for Samples: SN65HVD1050

FEATURES

- **Improved Replacement for the TJA1050**
- **High Electromagnetic Immunity (EMI)**
- **Very Low Electromagnetic Emissions (EME)**
- **Meets or Exceeds the Requirements of ISO 11898-2**
- **Bus-Fault Protection of –27 V to 40 V**
- **Dominant Time-Out Function**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance with Low V_{CC}**
  - **Monotonic Outputs During Power Cycling**

APPLICATIONS

- **Industrial Automation**
  - **DeviceNet™ Data Buses (Vendor ID #806)**
- **SAE J2284 High Speed CAN for Automotive Applications**
- **SAE J1939 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**

DESCRIPTION

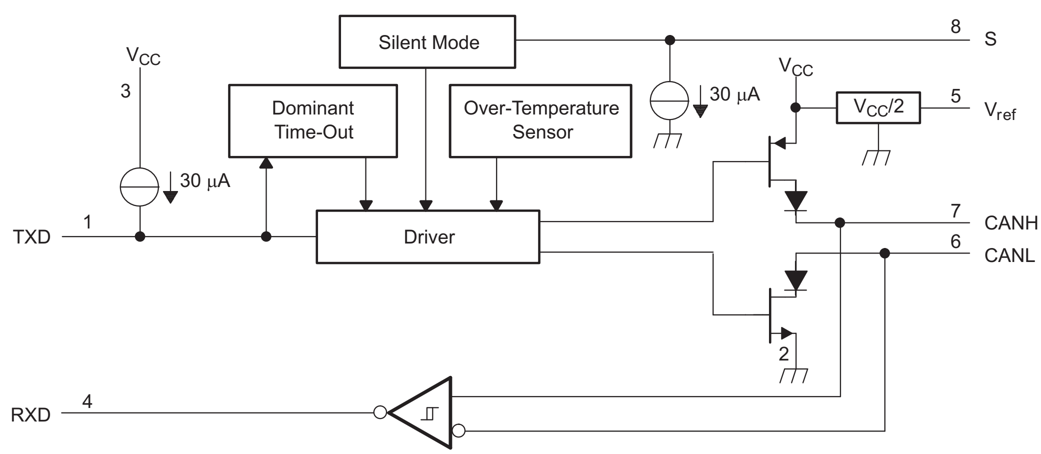
The SN65HVD1050 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN).

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)(1).

Designed for operation is especially harsh environments, the HVD1050 features cross-wire, over-voltage and loss of ground protection from -27 V to 40V, over-temperature shut down, a -12 V to 12 V common-mode range, and will withstand voltage transients from -200 V to 200 V according to ISO 7637.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTION BLOCK DIAGRAM



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Pin 8 provides for two different modes of operation: high-speed or silent mode. The high-speed mode of operation is selected by connecting S (pin 8) to ground.

If a high logic level is applied to the S pin of the SN65HVD1050, the device enters a listen-only silent mode during which the driver is switched off while the receiver remains fully functional.

In silent mode, all bus activity is passed by the receiver output to the local protocol controller. When data transmission is required, the local protocol controller reverses this low-current silent mode by placing a logic-low on the S pin to resume full operation.

A dominant-time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

V_{ref} (pin 5) is available as a $V_{CC}/2$ voltage reference.

The SN65HVD1050 is characterized for operation from –40°C to 125°C.

SN65HVD1050

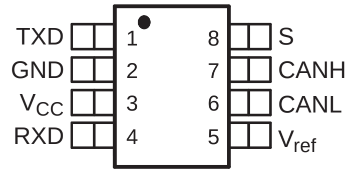


Table 1. ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKED AS	ORDERING NUMBER
SN65HVD1050	SOIC-8	VP1050	SN65HVD1050D (rail)
			SN65HVD1050DR (reel)

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
V_{CC}	Supply voltage(2)	–0.3 V to 7 V
	Voltage range at any bus terminal (CANH, CANL, V_{ref})	–27 V to 40 V
I_O	Receiver output current	20 mA
V_I	Voltage input, transient pulse(3) (CANH, CANL)	-200 V to 200 V
V_I	Voltage input range (TXD, S)	-0.5 V to 6 V
T_J	Junction temperature	–55°C to 170°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

ELECTROSTATIC DISCHARGE PROTECTION(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VALUE
IEC Contact Discharge	IEC 61000-4-2	Bus terminals vs GND	±6 kV
Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus terminals vs GND	±8 kV
		All pins	±4 kV
Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1.5 kV
Machine Model	ANSI/ESDS5.2-1996		±200 V

(1) All typical values at 25°C.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12		12	V
V_{IH}	High-level input voltage	TXD, S	2.1		V_{CC}	V
V_{IL}	Low-level input voltage	TXD, S	0		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			2	
T_J	Junction temperature	See *Thermal Characteristics* table, 1 Mbps minimum signaling rate with R_L = 54Ω	–40		150	°C
	Signaling Rate		20			kbps

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	5-V Supply current	Silent mode	S at V_{CC}, V_I = V_{CC}			6	10	mA
		Dominant	V_I = 0 V, 60 Ω Load, S at 0 V	4.75V < V_{CC} < 5.25V		50	70	
				4.5V < V_{CC} < 5.5V			75	
		Recessive	V_I = V_{CC}, No Load, S at 0 V			6	10	

DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	Figure 9, S at 0V	4.75V < V_{CC} < 5.25V	90		190	ns
			4.5V < V_{CC} < 5.5V	85		195	
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		4.75V < V_{CC} < 5.25V	90		190	
			4.5V < V_{CC} < 5.5V	85		195	

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0 V, S at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	4.75V < V_{CC} < 5.25V	2.9	3.4	4.5	V
				4.5V < V_{CC} < 5.5V	2.75		5.2	
		CANL		4.75V < V_{CC} < 5.25V	0.8		1.5	
				4.5V < V_{CC} < 5.5V			1.6	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3 V, S at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	4.75V < V_{CC} < 5.25V	2	2.3	3	V
				4.5V < V_{CC} < 5.5V	1.8		3	
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0 V, R_L = 60 Ω, S at 0 V, See Figure 1, Figure 2, and Figure 3	4.75V < V_{CC} < 5.25V	1.5		3	V
				4.5V < V_{CC} < 5.5V	1.4		3	
			V_I = 0 V, R_L = 45 Ω, S at 0 V, See Figure 1, Figure 2, and Figure 3	4.75V < V_{CC} < 5.25V	1.4		3	V
				4.5V < V_{CC} < 5.5V	1.3		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3 V, S at 0 V, See Figure 1 and Figure 2		–0.012		0.012	V
			V_I = 3 V, S at 0 V, No Load		–0.5		0.05	
$V_{OC(ss)}$	Steady state common-mode output voltage		S at 0 V, Figure 8	4.75V < V_{CC} < 5.25V	2	2.3	3	V
				4.5V < V_{CC} < 5.5V	1.9		3	
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage					30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}		–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V		–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V				1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = -12 V, CANL Open, See Figure 11		–105	–72		mA
			V_{CANH} = 12 V, CANL Open, SeeFigure 11			0.36	1	
			V_{CANL} = -12 V, CANH Open, See Figure 11		–1	–0.5		
			V_{CANL} = 12 V, CANH Open, See Figure 11			71	105	
C_O	Output capacitance		See receiver input capacitance					

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0 V, See Figure 4		25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	45	90	
t_r	Differential output signal rise time				25		
t_f	Differential output signal fall time				50		
t_{en}	Enable time from silent mode to dominant	See Figure 7				1	µs
$t_{(dom)}$	Dominant time-out	↓V_I, See Figure 10	4.75V < V_{CC} < 5.25V	300	450	700	µs
			4.5V < V_{CC} < 5.5V	280		700	

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	S at 0 V, See Table 4			800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			100	125		
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 6	4.75V < V_{CC} < 5.25V	4	4.6		V
			4.5V < V_{CC} < 5.5V	3.8			
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 6			0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5 V, Other pin at 0 V, V_{CC} at 0 V, TXD at 0 V			165	250	μA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V				20	μA
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V			13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)			5		
R_{ID}	Differential input resistance	TXD at 3 V, S at 0 V		30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)			15	30	40	
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] x 100%	$V_{(CANH)} = V_{(CANL)}$		–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0 V or V_{CC}, See Figure 6	4.75V < V_{CC} < 5.25V	60	100	130	ns
			4.5V < V_{CC} < 5.5V	60		135	
t_{PHL}	Propagation delay time, high-to-low-level output		4.75V < V_{CC} < 5.25V	45	70	90	
			4.5V < V_{CC} < 5.5V	45		95	
t_r	Output signal rise time				8		
t_f	Output signal fall time				8		

S-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	S at 2 V	20	40	70	μA
I_{IL}	Low level input current	S at 0.8 V	5	20	30	

VREF-PIN CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	–50 μA < I_O < 50 μA	0.4 V_{CC}	0.5 V_{CC}	0.6 V_{CC}	V

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-Air	Low-K thermal resistance[1]		211		°C/W
		High-K thermal resistance		131		
θ_{JB}	Junction-to-Board Thermal Resistance			53		
θ_{JC}	Junction-to-Case Thermal Resistance			79		
P_D	Average power dissipation	V_{CC} = 5.0 V, T_j = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF		112		mW
		V_{CC} = 5.5 V, T_j = 130°C, R_L = 45 Ω, S at 0 V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF			170	
$T_{J\_shutdown}$	Junction temperature, thermal shutdown[2]			190		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.
(2) Extended operation in thermal shutdown may affect device reliability, see APPLICATIONS INFORMATION.

FUNCTION TABLES

Table 2. DRIVER

INPUTS		OUTPUTS		BUS STATE
TXD[1]	S[1]	CANH[1]	CANL[1]	
L	L or Open	H	L	DOMINANT
H	X	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 3. RECEIVER

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	OUTPUT RXD[1]	BUS STATE
$V_{ID} \geq 0.9$ V	L	DOMINANT
0.5 V < V_{ID} < 0.9 V	?	?
$V_{ID} \leq 0.5$ V	H	RECESSIVE
Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

PARAMETER MEASUREMENT INFORMATION

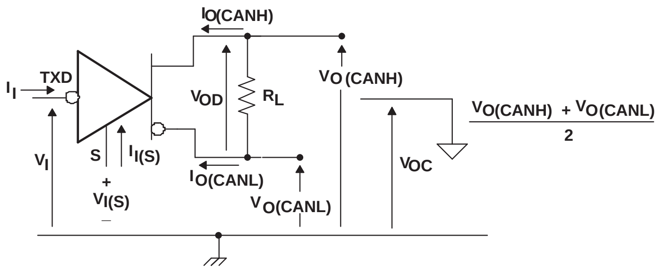


Figure 1. Driver Voltage, Current, and Test Definition

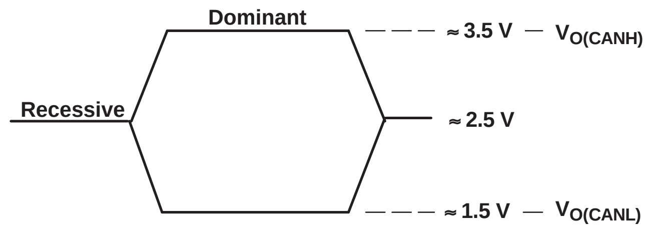


Figure 2. Bus Logic State Voltage Definitions

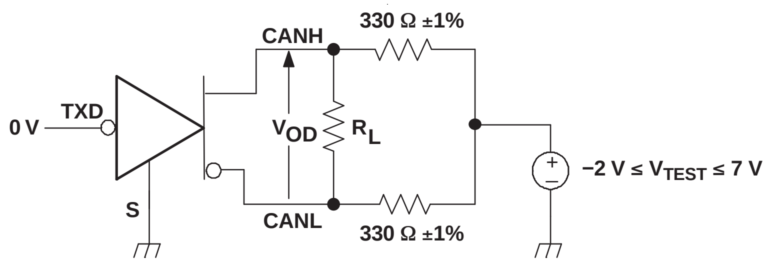


Figure 3. Driver V_{OD} Test Circuit

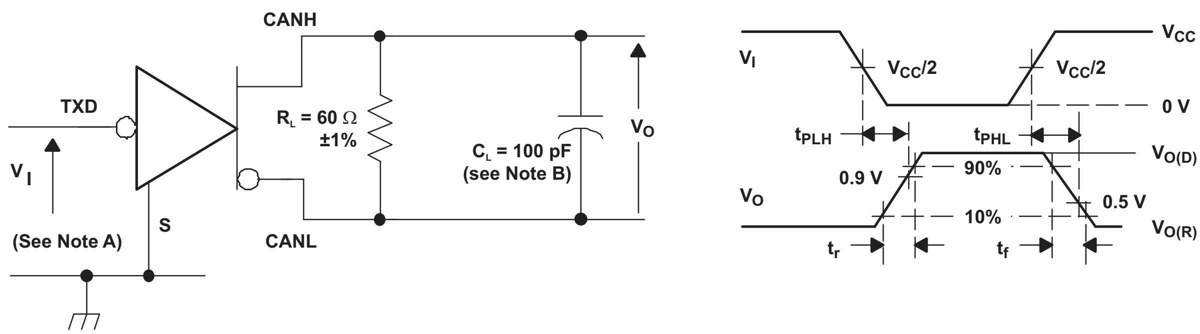


Figure 4. Driver Test Circuit and Voltage Waveforms

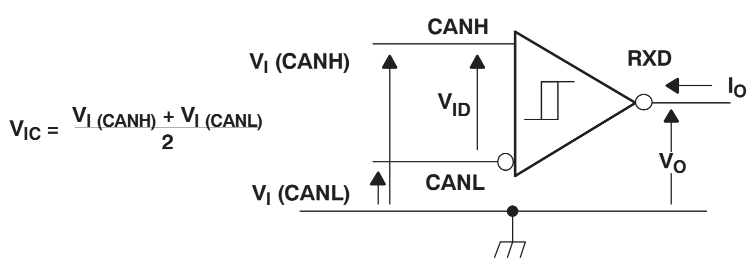
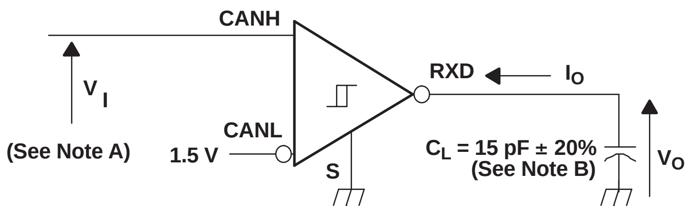
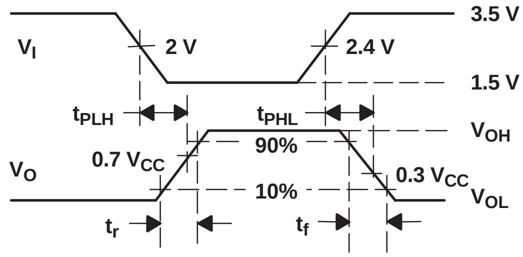


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)





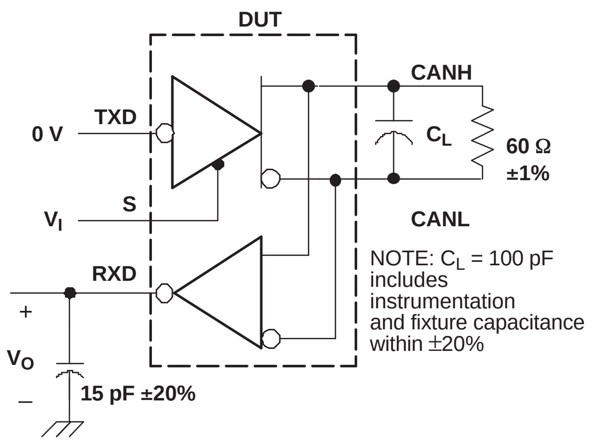
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

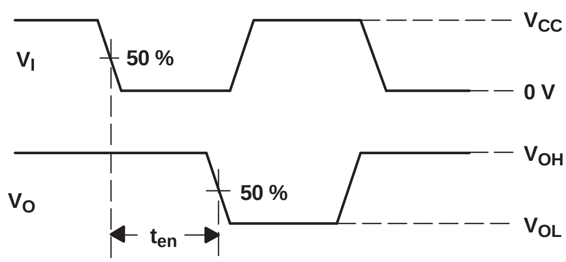
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 4. Differential Input Voltage Threshold Test

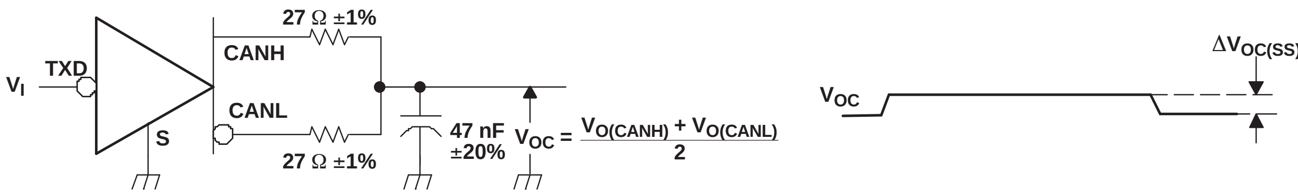
INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	





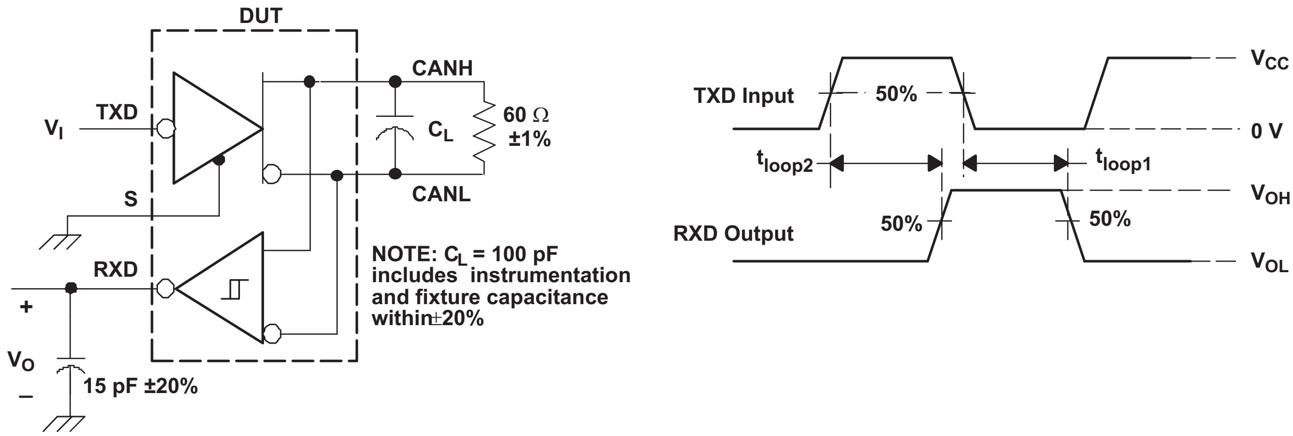
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle

Figure 7. t_{en} Test Circuit and Waveform



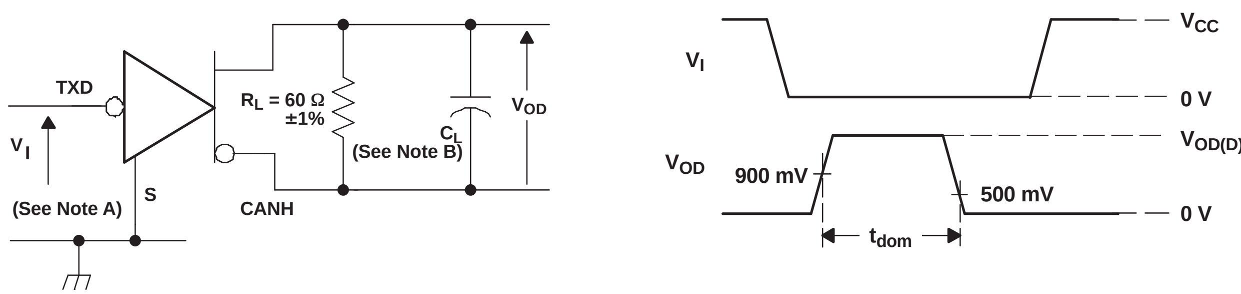
NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common Mode Output Voltage Test and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Time-Out Test Circuit and Waveforms

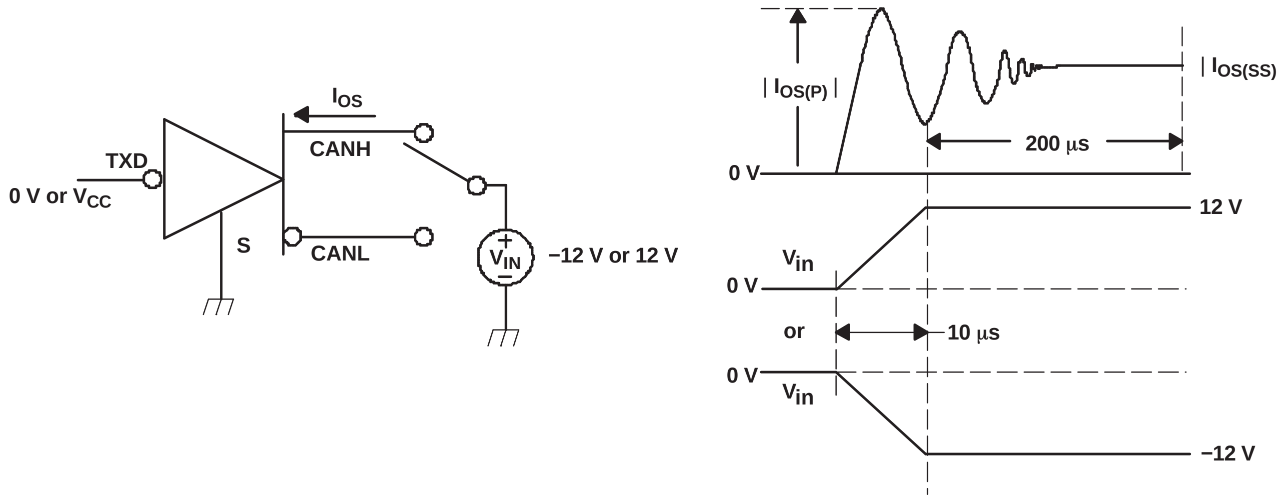


Figure 11. Driver Short-Circuit Current Test and Waveform

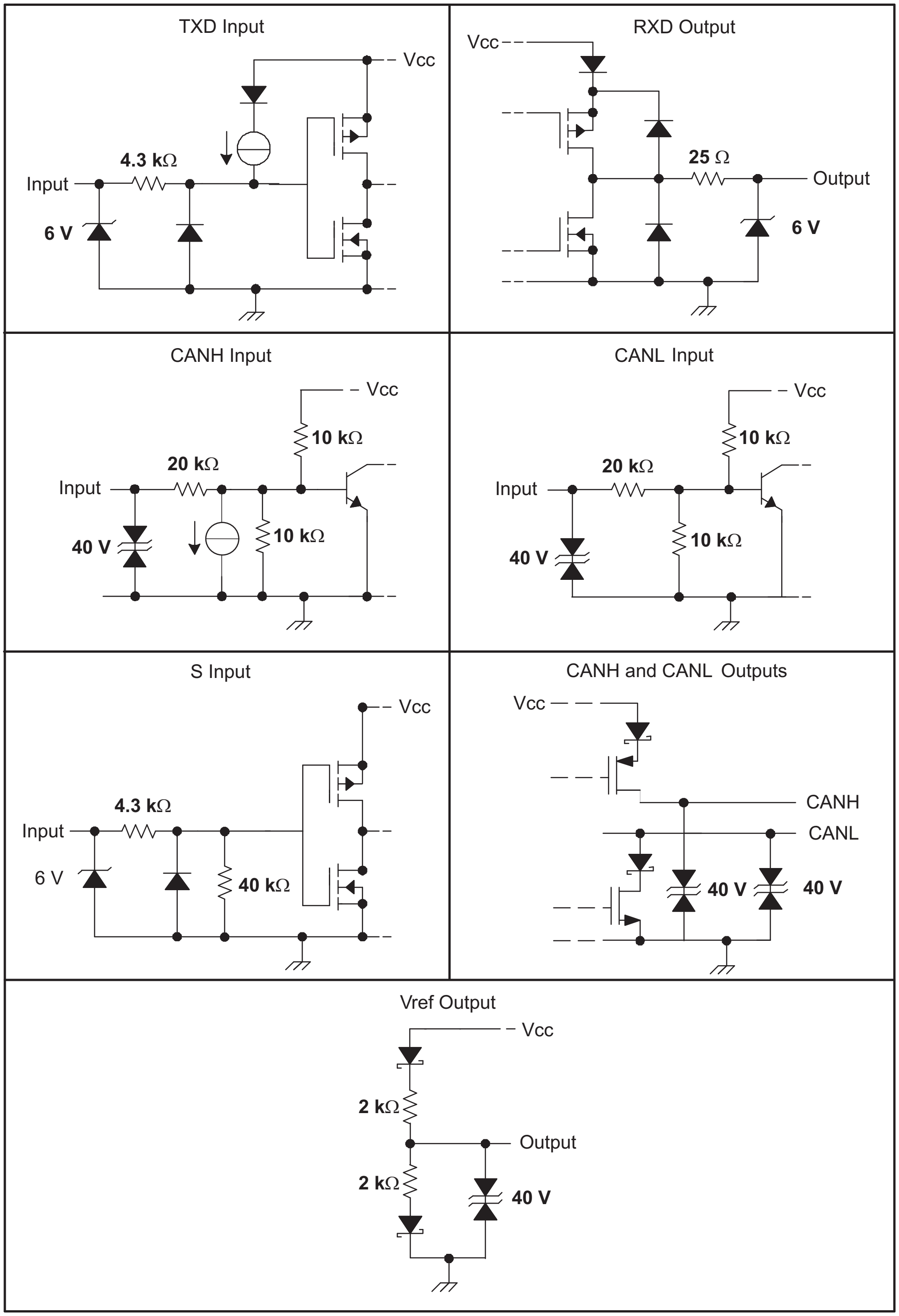
DEVICE INFORMATION

Table 5. Parametric Cross Reference With the TJA1050

TJA1050 (1)	PARAMETER	HVD1050
TRANSMITTER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
BUS SECTION		
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{i(dif)(hys)}$	Diffrential input hysteresis	Receiver V_{hys}
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{O(dif)(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(dif)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
C_i	Input capacitance to ground	Receiver C_I
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
Vref PIN SECTION		
V_{ref}	Reference output voltage	V_O
TIMING SECTION		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
	$t_{d(TXD-BUSon)} + t_{d(BUSon-RXD)}$	Device t_{LOOP1}
	$t_{d(TXD-BUSoff)} + t_{d(BUSoff-RXD)}$	Device t_{LOOP2}
$t_{dom(TXD)}$	Dominant time out	Driver $t_{(dom)}$
S PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1050 Product Specification, Philips Semiconductors, 2002 May 16.

Equivalent Input and Output Schematic Diagrams



TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

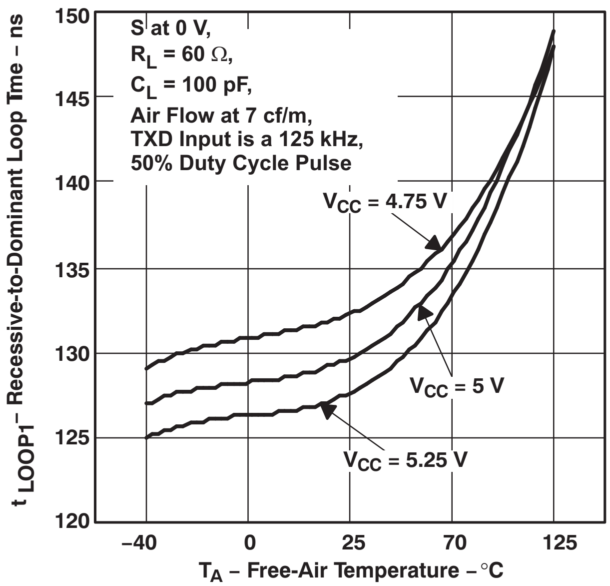


Figure 12.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

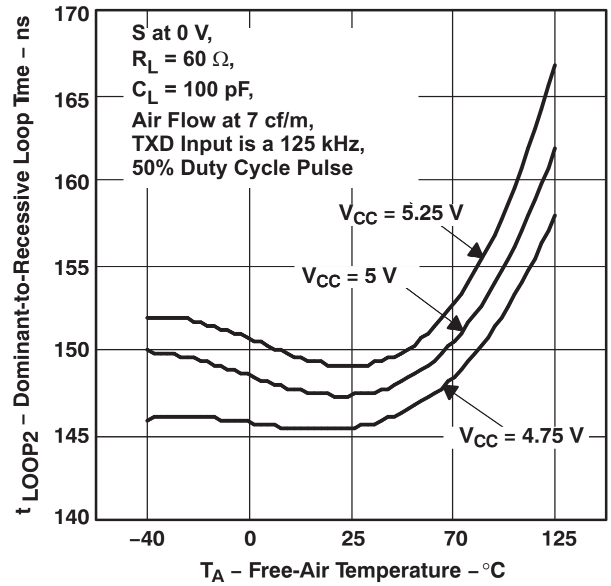


Figure 13.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE

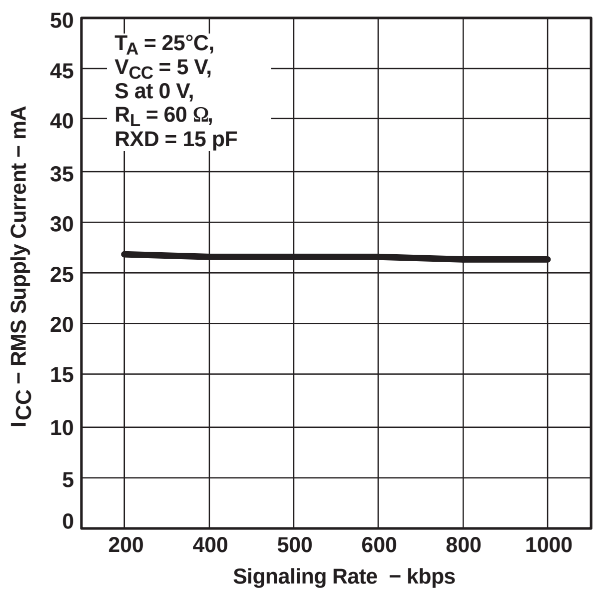


Figure 14.

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

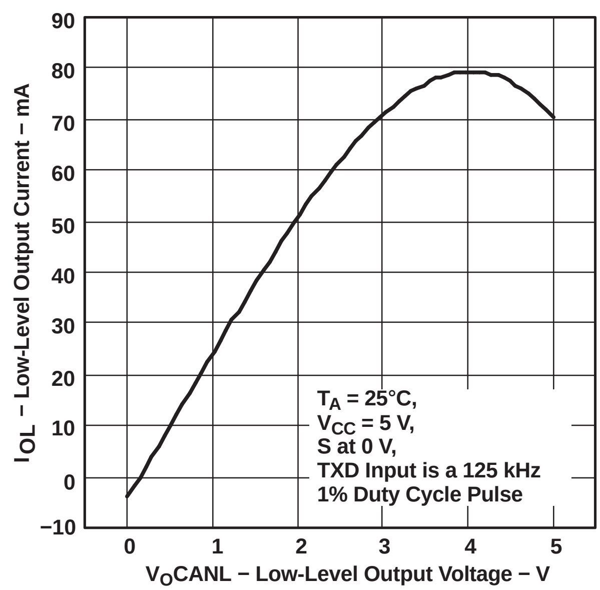


Figure 15.

TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

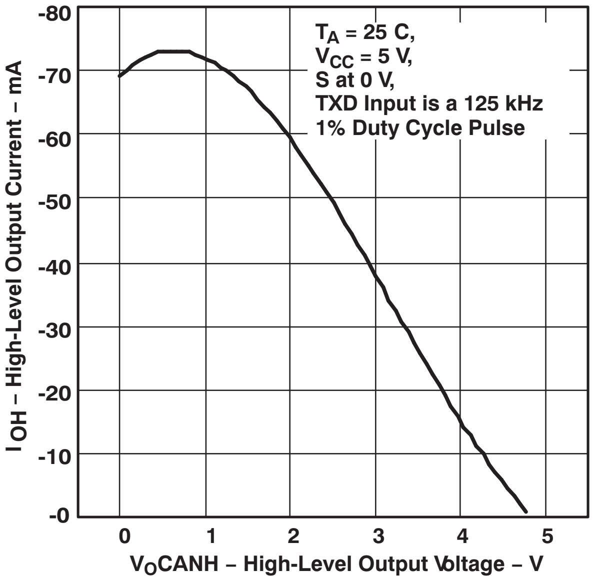


Figure 16.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE (across V_{CC})

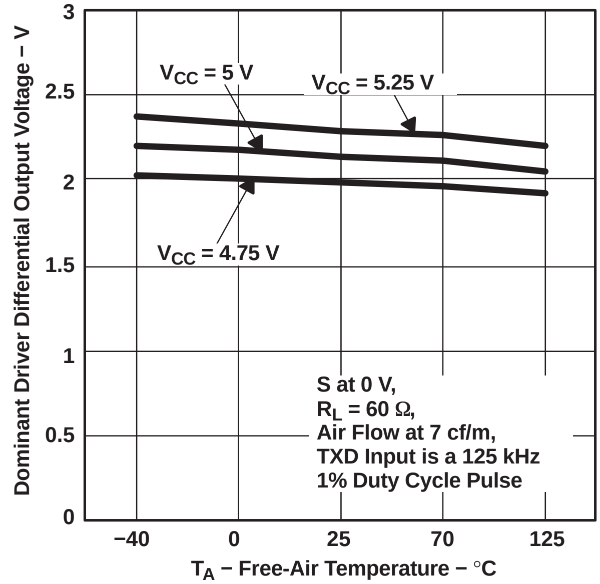


Figure 17.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

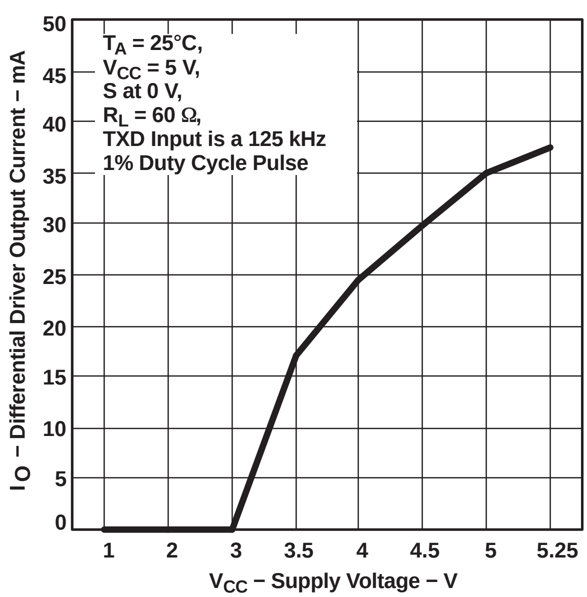


Figure 18.

RECEIVER OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

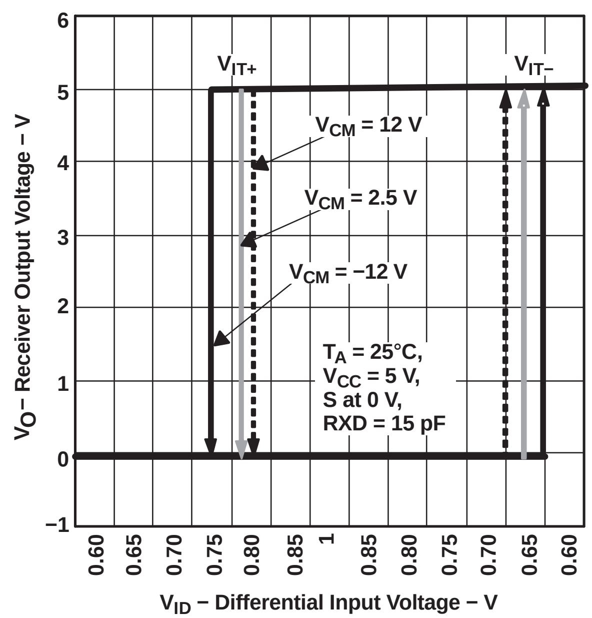


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TYPICAL ELECTROMAGNETIC EMISSIONS UP TO 50 MHZ (Peak Amplitude)

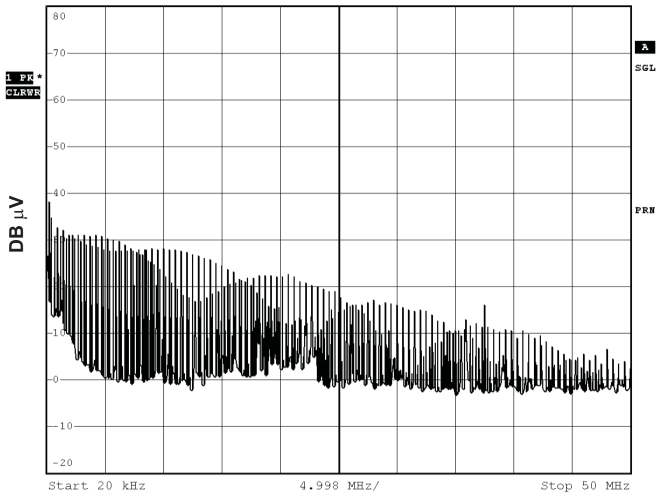


Figure 20. Frequency Spectrum of Common-Mode Emissions

TYPICAL ELECTROMAGNETIC IMMUNITY PERFORMANCE

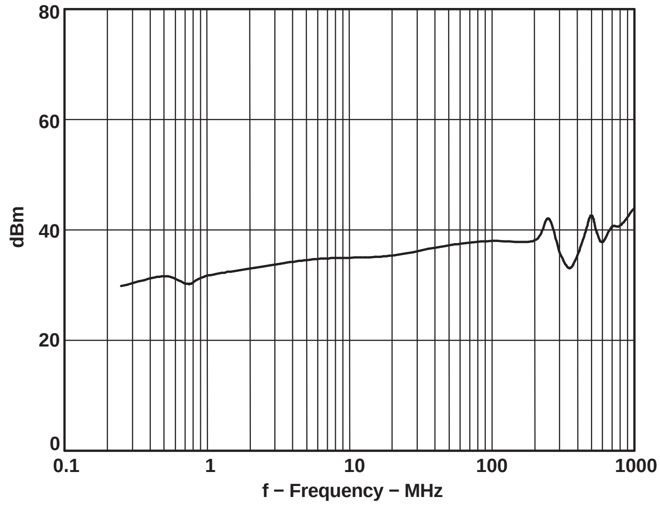


Figure 21. Direct Power Injection (DPI) Response vs Frequency

APPLICATION INFORMATION

Thermal Shutdown

The SN65HVD1050 has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an SN65HVD1050 is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

Bus Loading

Q: *How many HVD1050 nodes can be connected on a bus?*

A: In the CAN standard ISO 11898-2 the driver differential output is specified with a 60Ω load (must be greater than 1.5V) and with a fully-loaded bus (must be greater than 1.2V). The HVD1050 is specified to meet the 1.5V requirement with a 60Ω load, and 1.4V with a 45Ω load. The differential input resistance of the HVD1050 is a minimum of 30kΩ. If 167 transceivers are in parallel on a bus, this is equivalent to a 180Ω differential load. That transceiver load of 180Ω in parallel with the 60Ω (two 120Ω termination resistors) gives a total 45Ω. Therefore, the HVD1050 supports over 167 transceivers on a single bus segment, with margin to the 1.2V CAN requirement.

Dominant Time-Out Feature

A dominant-time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication in the event of a hardware or software failure of the local CAN controller. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD. This feature prevents a faulty local CAN controller from corrupting the entire network with a “stuck” dominant state. The dominant time-out timer is selected to pass all normal CAN messages; however, non-standard applications may inadvertently trigger the dominant time-out if long strings of dominant bits are attempted at slow data rates.

REVISION HISTORY

Changes from Revision A (May 2007) to Revision B **Page**

- Deleted sentence, "The device is also qualified for use in ISO 11898-2 automotive applications in accordance with AEC-Q100." and footnote, "The device is available with Q100 qualification as the SN65HVD1050Q." 1
- Changed V_{CC} min/max range from 4.75-5.25V to 4.5-5.5V 3
- Changed V_{IH} max from 5.25V to 5.5V 3
- Added rows for various parameters showing parameters with V_{CC} ±5% and ±10% 3
- Added Signaling Rate spec, min 20kbps 3
- Changed V_{IH} min from 2 to 2.1V 3
- Changed Bus output voltage (Dominant) CANH 4.5V < V_{CC} < 5.5V from 4.75 to 5.2 4
- Added Bus Loading application discussion. 16
- Added Dominant Time-Out Feature discussion. 16