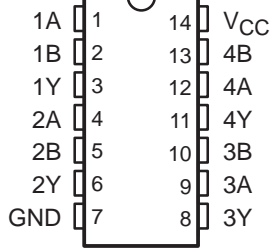


# SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

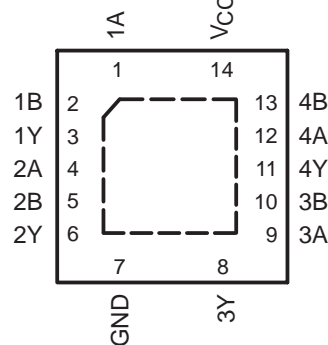
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

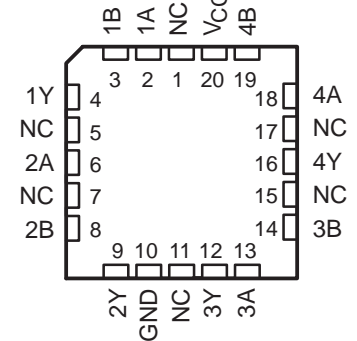
SN54LVC00A ... J OR W PACKAGE  
SN74LVC00A ... D, DB, NS, OR PW PACKAGE  
(TOP VIEW)



SN74LVC00A ... RGY PACKAGE  
(TOP VIEW)



SN54LVC00A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN54LVC00A quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC00A quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The 'LVC00A devices perform the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC00ARGYR	LC00A
	SOIC – D	Tube of 50	SN74LVC00AD	LVC00A
		Reel of 2500	SN74LVC00ADR	
		Reel of 250	SN74LVC00ADT	
	SOP – NS	Reel of 2000	SN74LVC00ANSR	LVC00A
	SSOP – DB	Reel of 2000	SN74LVC00ADBR	LC00A
–55°C to 125°C	TSSOP – PW	Tube of 90	SN74LVC00APW	LC00A
		Reel of 2000	SN74LVC00APWR	
		Reel of 250	SN74LVC00APWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC00AJ	SNJ54LVC00AJ
	CFP – W	Tube of 150	SNJ54LVC00AW	SNJ54LVC00AW
	LCCC – FK	Tube of 55	SNJ54LVC00AFK	SNJ54LVC00AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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# SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	86°C/W
(see Note 3): DB package .....	96°C/W
(see Note 3): NS package .....	76°C/W
(see Note 3): PW package .....	113°C/W
(see Note 4): RGY package .....	47°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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## recommended operating conditions (see Note 5)

		SN54LVC00A		SN74LVC00A				UNIT		
		–55 TO 125°C		T <sub>A</sub> = 25°C		–40 TO 85°C				
		MIN	MAX	MIN	MAX	MIN	MAX			
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	1.65	3.6	1.65	3.6	V
			Data retention only		1.5		1.5		1.5	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V				0.65×V <sub>CC</sub>		0.65×V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V				1.7		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		2		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V				0.35×V <sub>CC</sub>		0.35×V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V				0.7		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	0.8		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V				–4		–4		mA
		V <sub>CC</sub> = 2.3 V				–8		–8		
		V <sub>CC</sub> = 2.7 V			–12	–12		–12		
		V <sub>CC</sub> = 3 V			–24	–24		–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V				4		4		mA
		V <sub>CC</sub> = 2.3 V				8		8		
		V <sub>CC</sub> = 2.7 V			12	12		12		
		V <sub>CC</sub> = 3 V			24	24		24		

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC00A		SN74LVC00A			UNIT	
			-55 TO 125°C		T <sub>A</sub> = 25°C				
			MIN	MAX	MIN	TYP	MAX		MIN
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V			V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2	V	
		2.7 V to 3.6 V	V <sub>CC</sub> -0.2						
	I <sub>OH</sub> = -4 mA	1.65 V		1.29		1.2			
	I <sub>OH</sub> = -8 mA	2.3 V		1.9		1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2	2.2	2.2	2.2			
		3 V	2.4	2.4	2.4	2.4			
I <sub>OH</sub> = -24 mA	3 V	2.2	2.3	2.3	2.2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.1		0.2	V	
		2.7 V to 3.6 V		0.2					
	I <sub>OL</sub> = 4 mA	1.65 V			0.24		0.45		
	I <sub>OL</sub> = 8 mA	2.3 V			0.3		0.7		
	I <sub>OL</sub> = 12 mA	2.7 V		0.4	0.4	0.4	0.4		
3 V			0.55	0.55	0.55	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V		±5		±1		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V		10		1		10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500		500		500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				5			pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC00A		UNIT
				-55 TO 125°C		
				MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.7 V		5.1	ns
			3.3 V ± 0.3 V	1	4.3	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC00A				UNIT	
				T <sub>A</sub> = 25°C			-40 TO 85°C		
				MIN	TYP	MAX	MIN		MAX
t <sub>pd</sub>	A or B	Y	1.8 V ± 0.15 V	1	6	12	1	12.5	ns
			2.5 V ± 0.2 V	1	4.6	5.9	1	6.4	
			2.7 V	1	4.3	4.9	1	5.1	
			3.3 V ± 0.3 V	1	3.5	4.1	1	4.3	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V				1	ns	



# SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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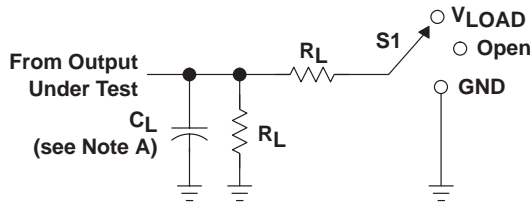
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	18	pF
			2.5 V	18	
			3.3 V	19	

# SN54LVC00A, SN74LVC00A QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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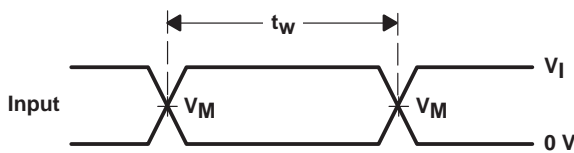
## PARAMETER MEASUREMENT INFORMATION



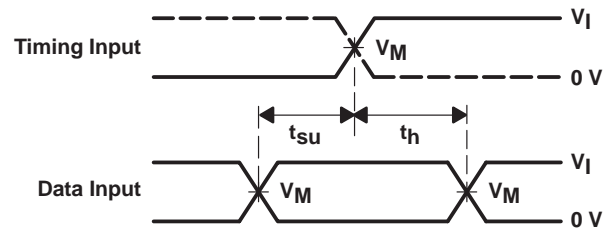
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

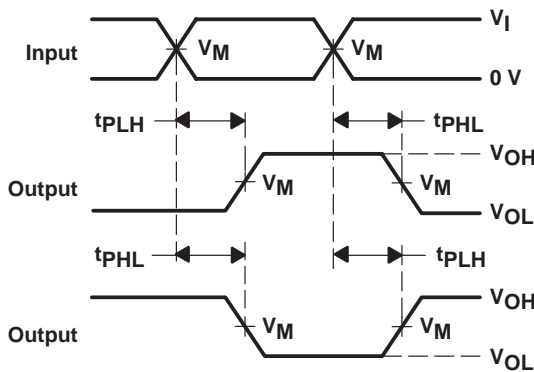
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



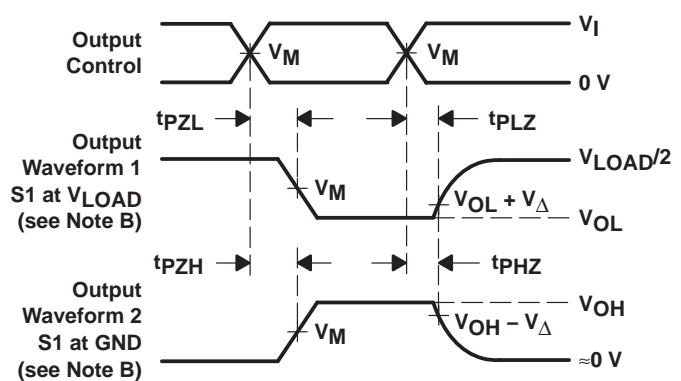
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

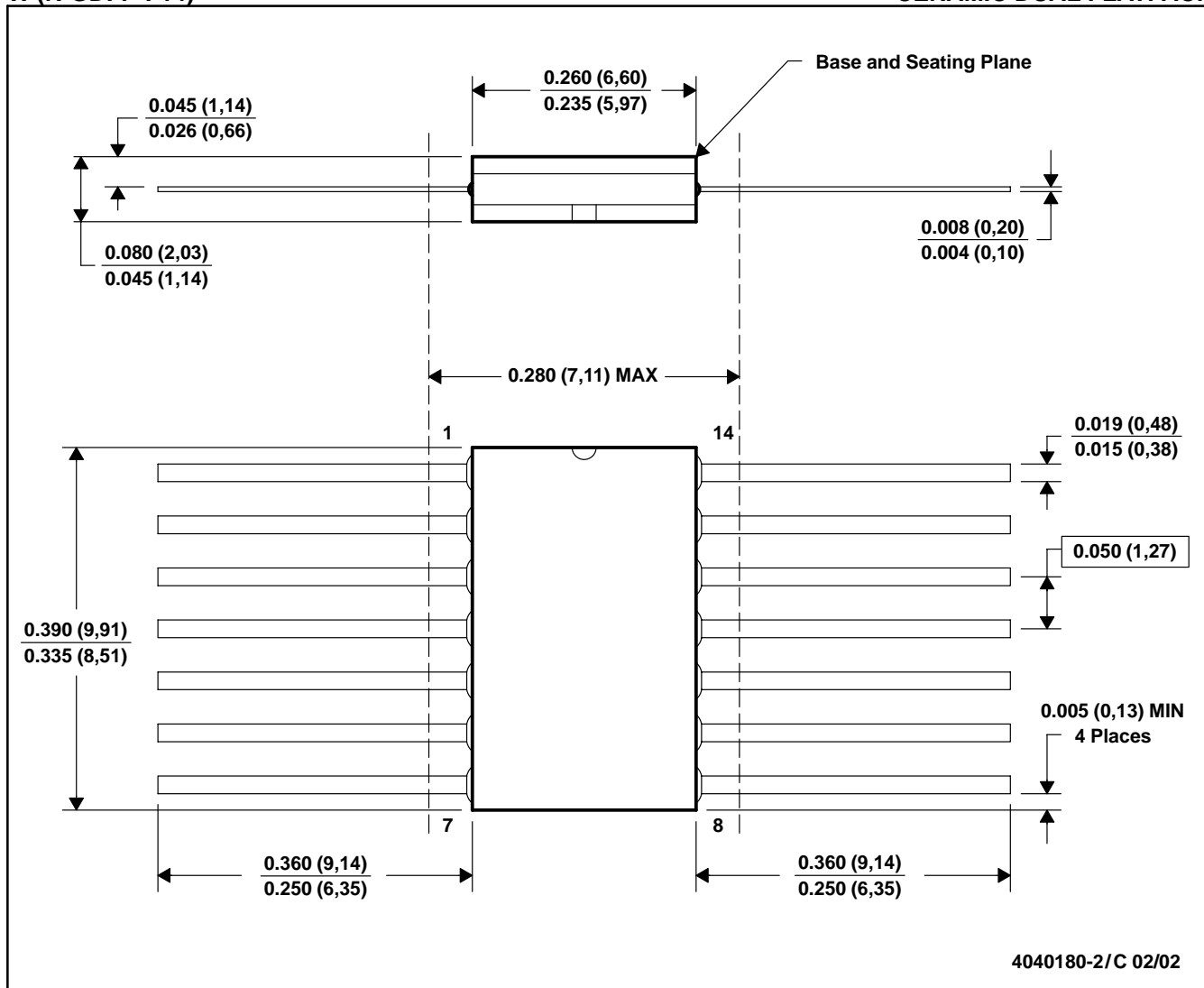


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/C 02/02

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

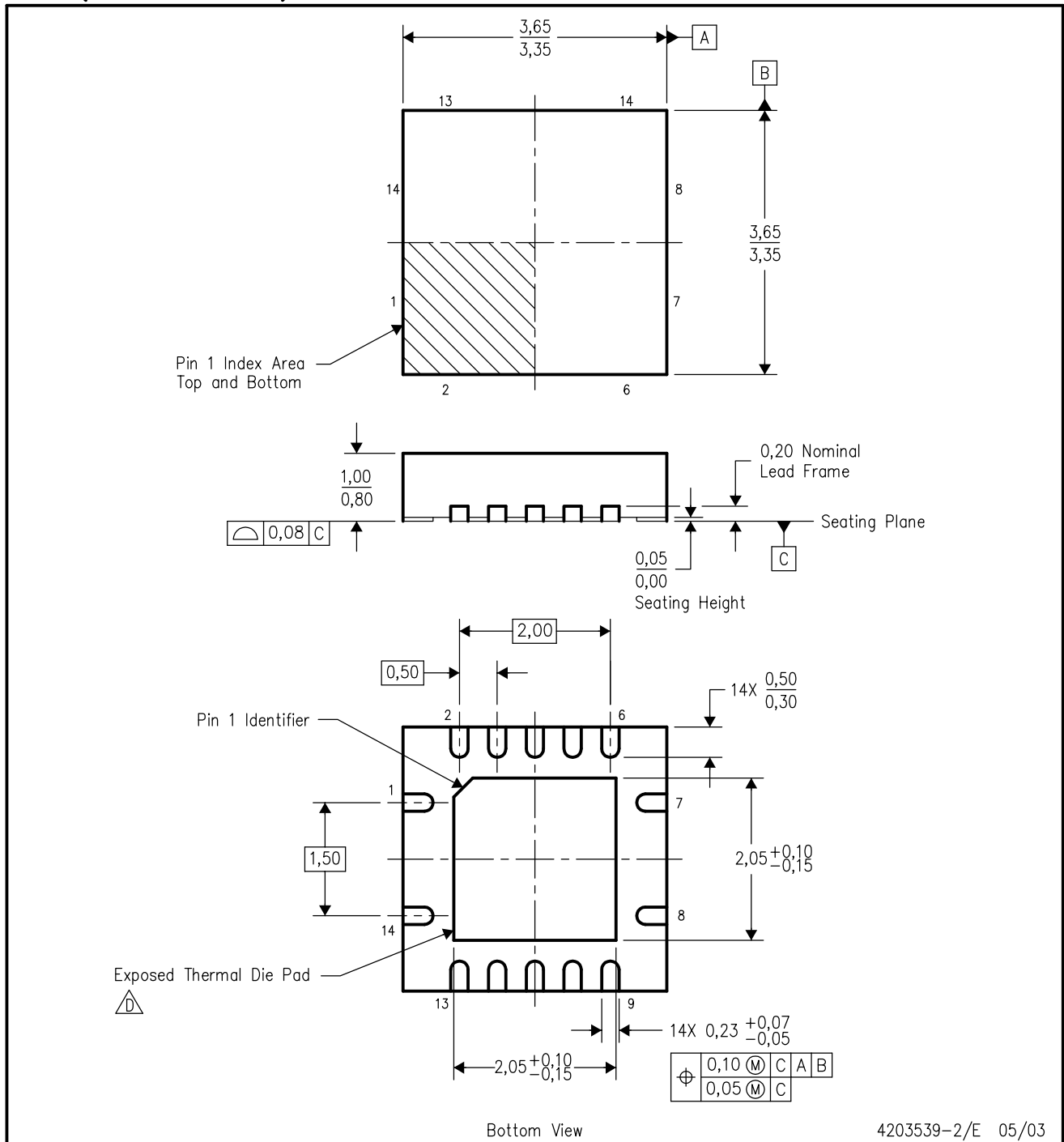
28 TERMINAL SHOWN




- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK

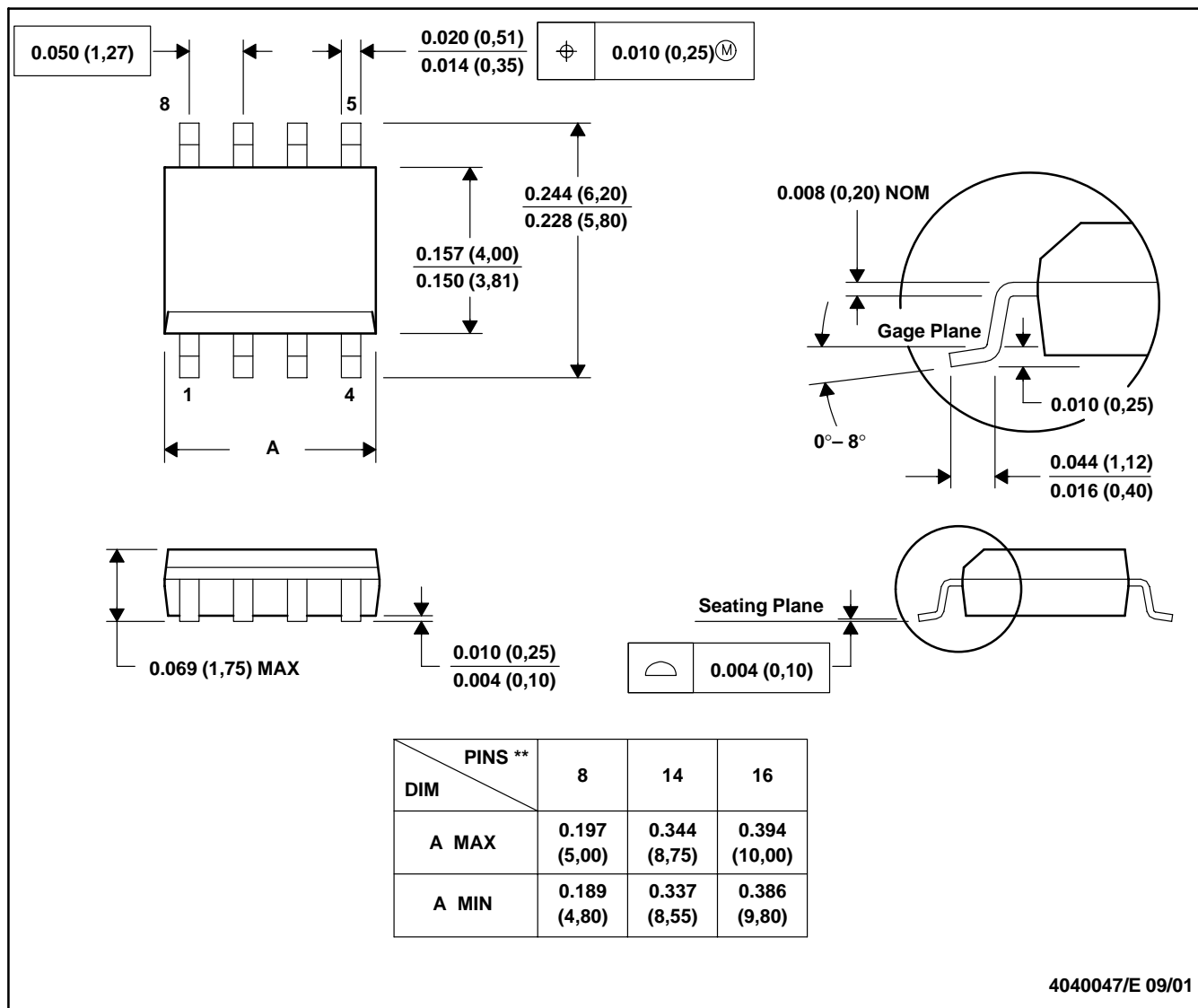


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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