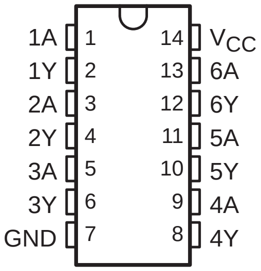
SN54LVC04A, SN74LVC04A
HEX INVERTERS

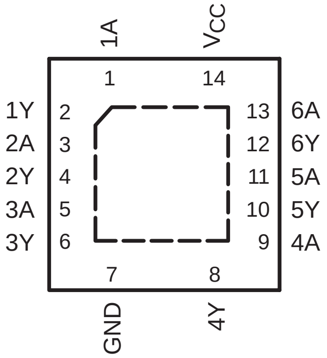
SCAS281P − JANUARY 1993 − REVISED SEPTEMBER 2003

- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 4.5 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **− 2000-V Human-Body Model (A114-A)**
  - **− 200-V Machine Model (A115-A)**
  - **− 1000-V Charged-Device Model (C101)**

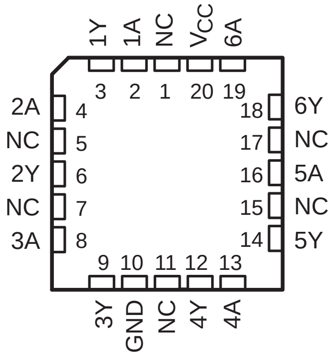
SN54LVC04A . . . J OR W PACKAGE
SN74LVC04A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC04A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC04A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN54LVC04A hex inverter contains six independent inverters designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC04A hex inverter contains six independent inverters designed for 1.65-V to 3.6-V V_{CC} operation. The ’LVC04A devices perform the Boolean function $Y = \overline{A}$.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Reel of 1000	SN74LVC04ARGYR	LC04A
	SOIC − D	Tube of 50	SN74LVC04AD	LVC04A
		Reel of 2500	SN74LVC04ADR	
		Reel of 250	SN74LVC04ADT	
	SOP − NS	Reel of 2000	SN74LVC04ANSR	LVC04A
	SSOP − DB	Reel of 2000	SN74LVC04ADBR	LC04A
	TSSOP − PW	Tube of 90	SN74LVC04APW	LC04A
		Reel of 2000	SN74LVC04APWR	
		Reel of 250	SN74LVC04APWT	
	TVSOP − DGV	Reel of 2000	SN74LVC04ADGVR	LC04A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LVC04AJ	SNJ54LVC04AJ
	CFP − W	Tube of 150	SNJ54LVC04AW	SNJ54LVC04AW
	LCCC − FK	Tube of 55	SNJ54LVC04AFK	SNJ54LVC04AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

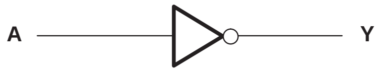
description/ordering information (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	−0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): DGV package	127°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVC04A		SN74LVC04A				UNIT
			−55 TO 125°C		T_A = 25°C		−40 TO 85°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.65×V_{CC}		0.65×V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V			1.7		1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				0.35×V_{CC}		0.35×V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V				0.7		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4		−4	mA
		V_{CC} = 2.3 V				−8		−8	
		V_{CC} = 2.7 V		−12		−12		−12	
		V_{CC} = 3 V		−24		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4		4	mA
		V_{CC} = 2.3 V				8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVC04A		SN74LVC04A					UNIT
			−55 TO 125°C		T_A = 25°C			−40 TO 85°C		
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = −100 µA	1.65 V to 3.6 V			V_{CC}−0.2			V_{CC}−0.2		V
		2.7 V to 3.6 V	V_{CC}−0.2							
	I_{OH} = −4 mA	1.65 V			1.29			1.2		
	I_{OH} = −8 mA	2.3 V			1.9			1.7		
	I_{OH} = −12 mA	2.7 V	2.2		2.2			2.2		
		3 V	2.4		2.4			2.4		
	I_{OH} = −24 mA	3 V	2.2		2.3			2.2		
V_{OL}	I_{OL} = 100 µA	1.65 V to 3.6 V					0.1		0.2	V
		2.7 V to 3.6 V		0.2						
	I_{OL} = 4 mA	1.65 V					0.24		0.45	
	I_{OL} = 8 mA	2.3 V					0.3		0.7	
	I_{OL} = 12 mA	2.7 V		0.4			0.4		0.4	
	I_{OL} = 24 mA	3 V		0.55			0.55		0.55	
I_I	V_I = 5.5 V or GND	3.6 V		±5			±1		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V		10			1		10	µA
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V		500			500		500	µA
C_i	V_I = V_{CC} or GND	3.3 V				5				pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54LVC04A		UNIT
				−55 TO 125°C		
				MIN	MAX	
t_{pd}	A	Y	2.7 V		5.5	ns
			3.3 V ± 0.3 V	0.5	4.5	

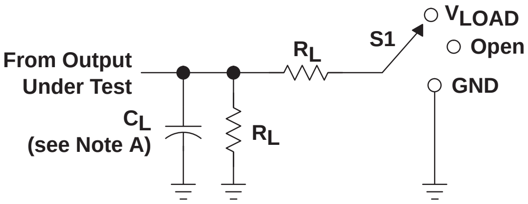
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74LVC04A					UNIT
				T_A = 25°C			−40 TO 85°C		
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	1.8 V ± 0.15 V	1	4.1	7.5	1	8	ns
			2.5 V ± 0.2 V	1	3.6	7	1	7.5	
			2.7 V	1	3	5.3	1	5.5	
			3.3 V ± 0.3 V	1	2.5	4.3	1	4.5	
$t_{sk(o)}$			3.3 V ± 0.3 V					1	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	6	pF
			2.5 V	7	
			3.3 V	8	

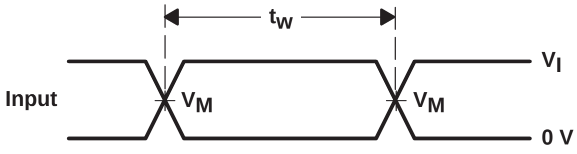
PARAMETER MEASUREMENT INFORMATION



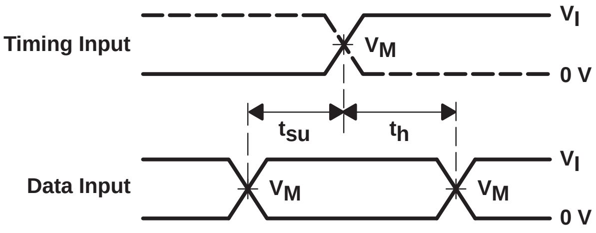
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

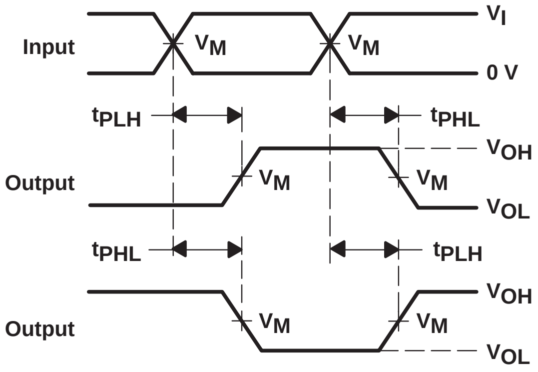
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



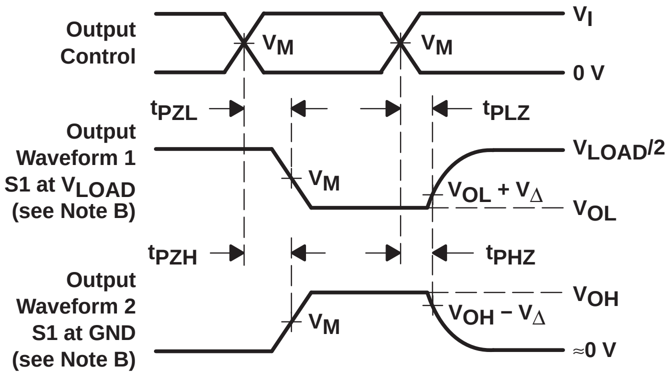
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



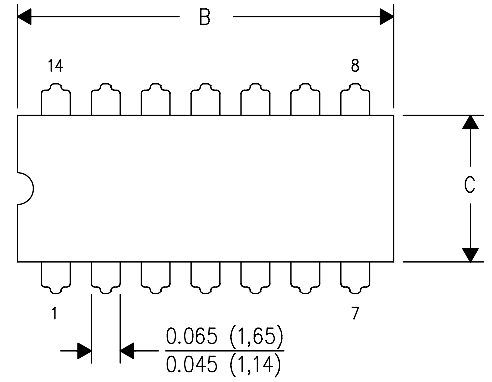
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

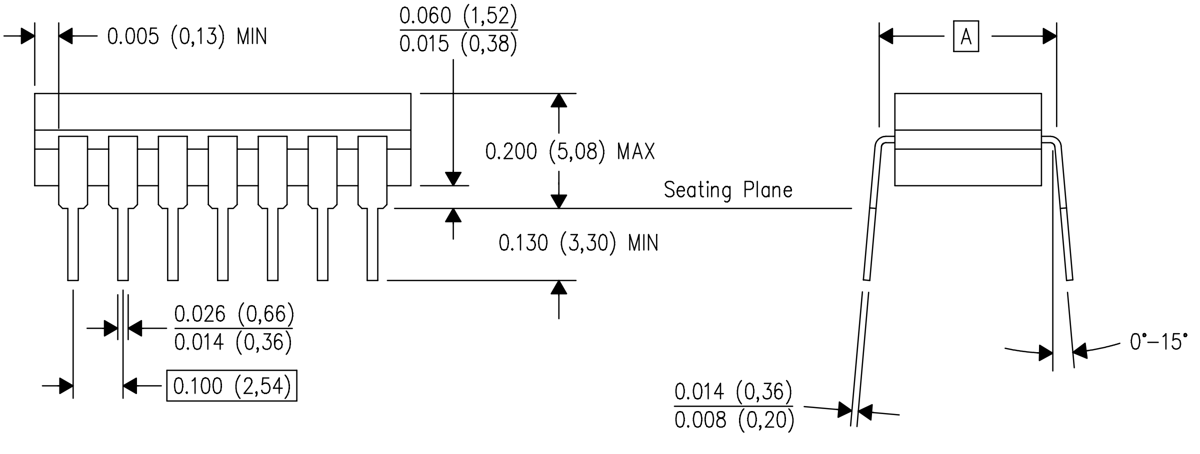
Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



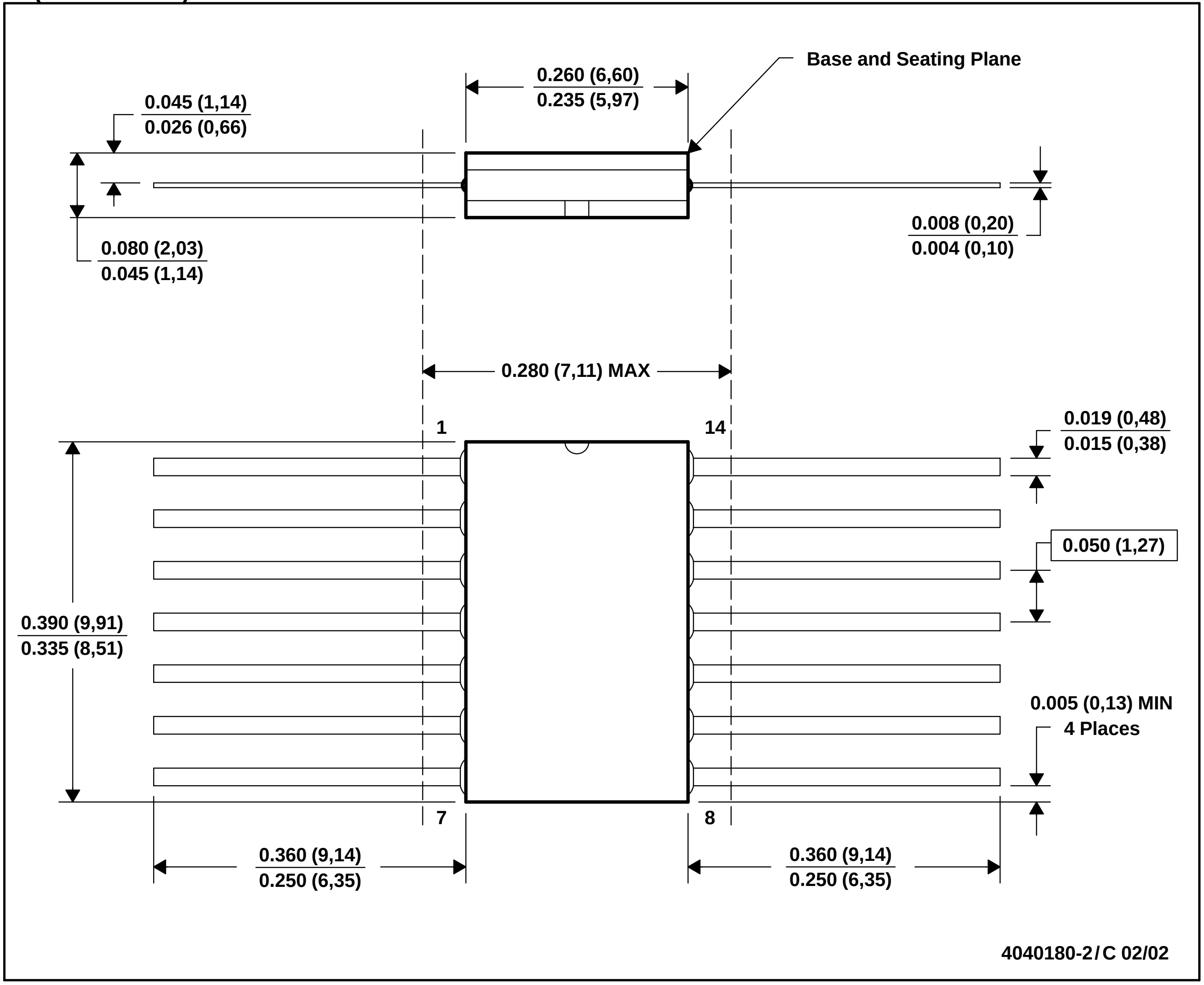
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

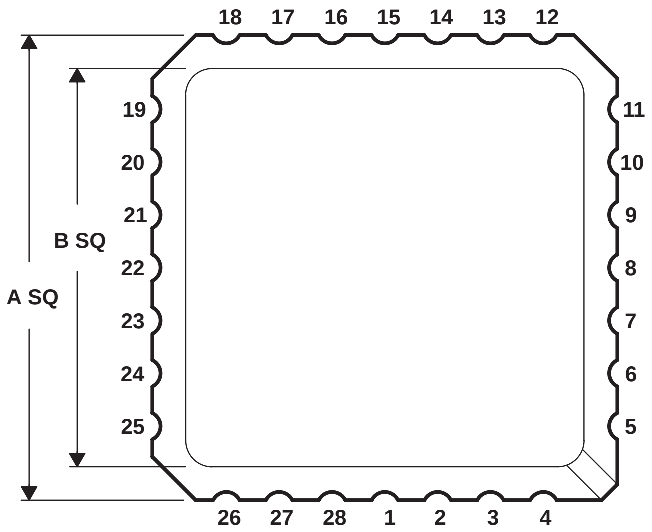
W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



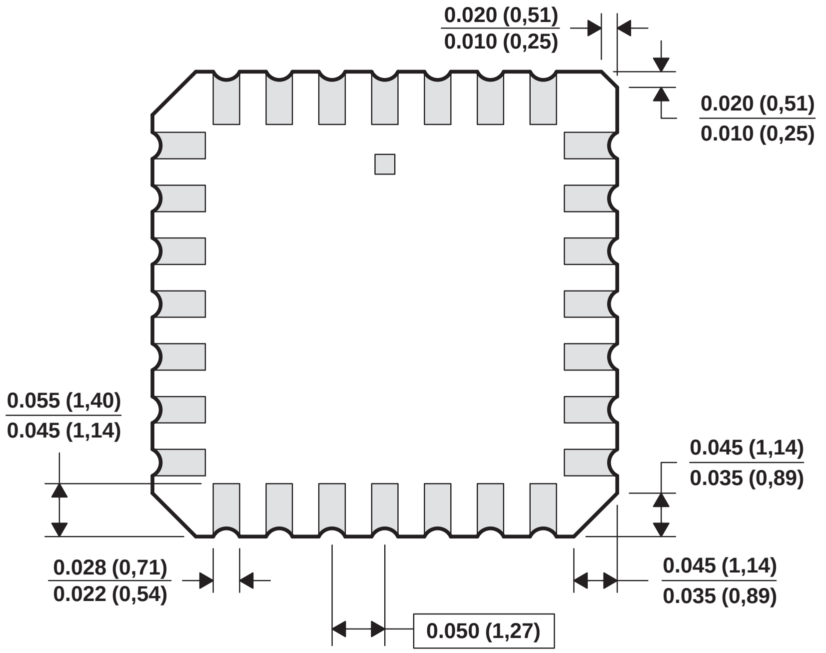
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

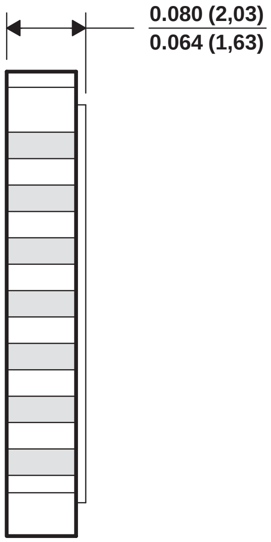
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



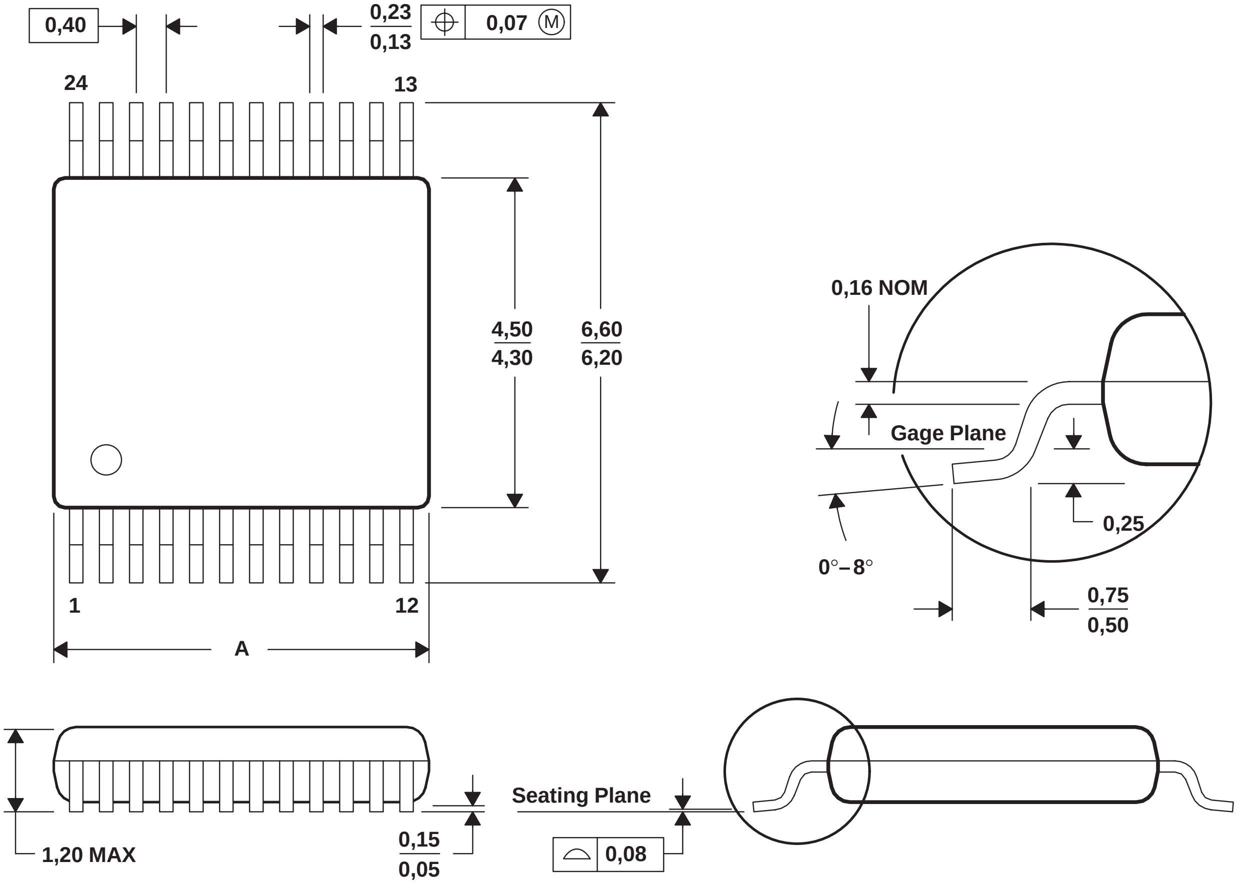


4040140 / D 10/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

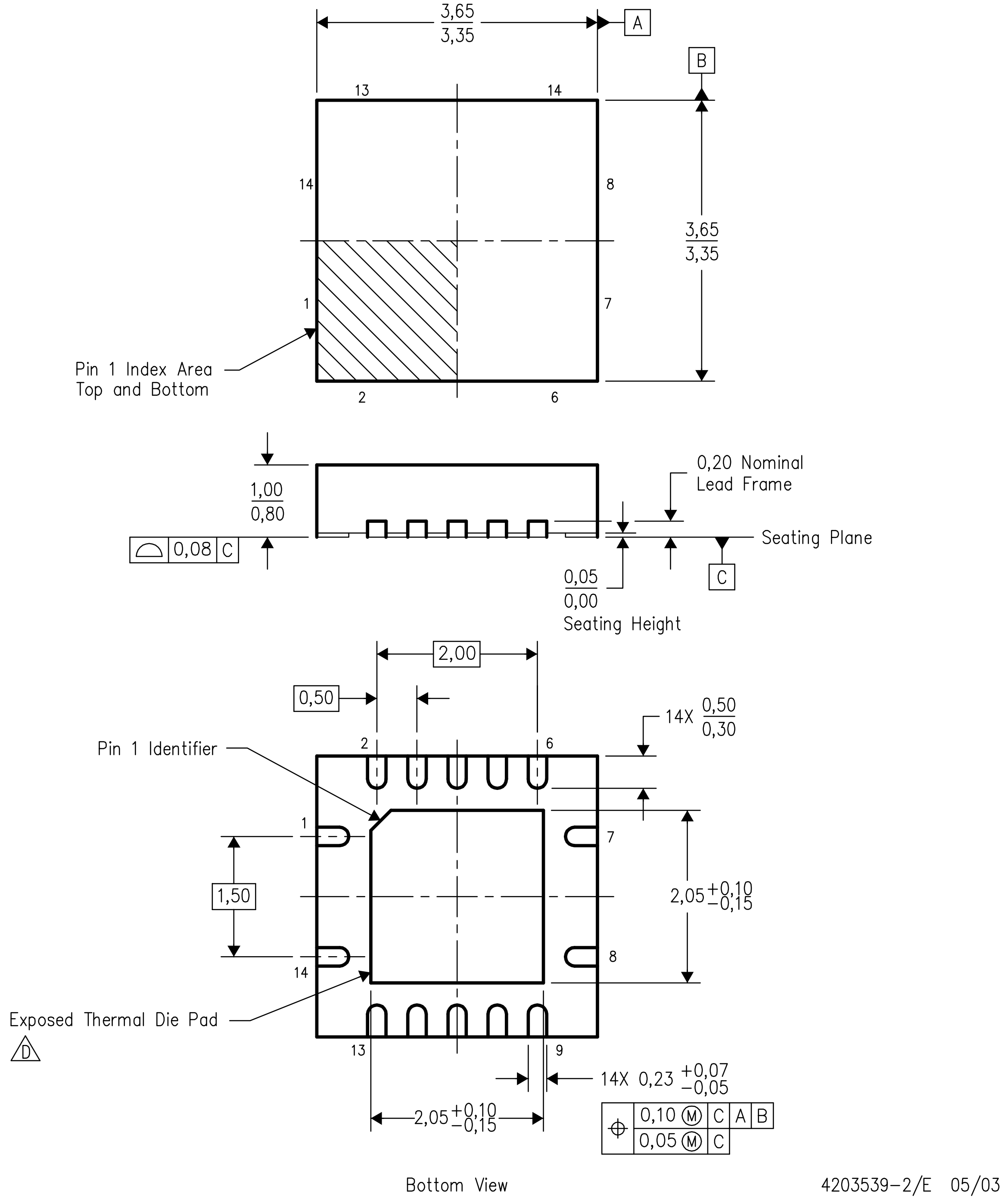


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

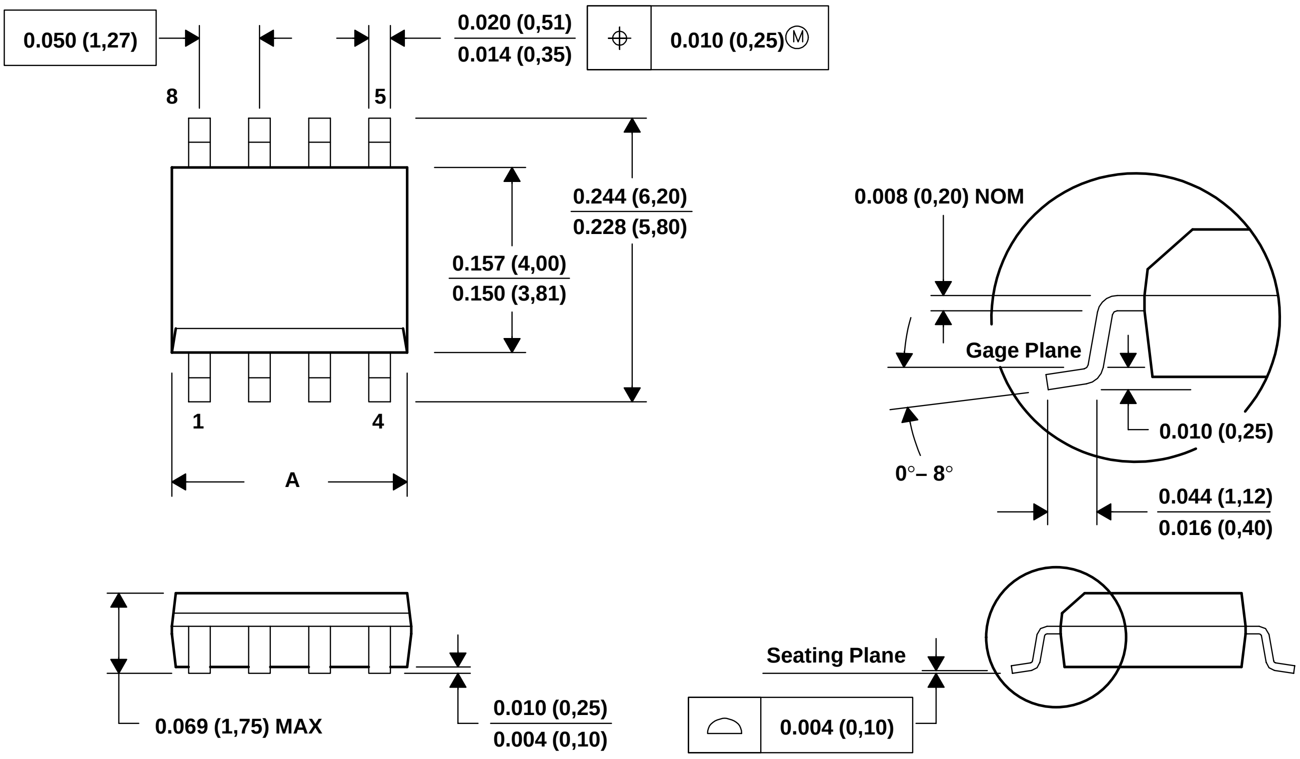
RGY (S–PQFP–N14) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
- E. Package complies to JEDEC MO–241 variation BA.

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

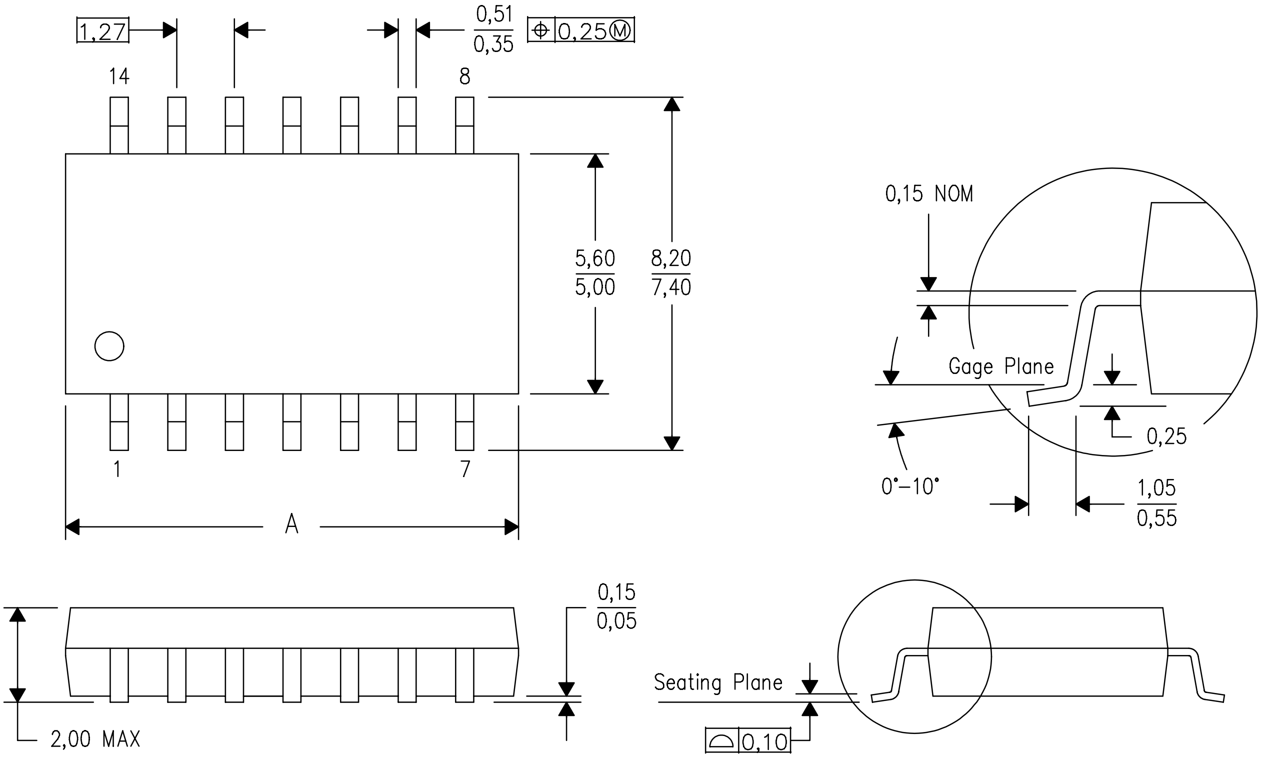
4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



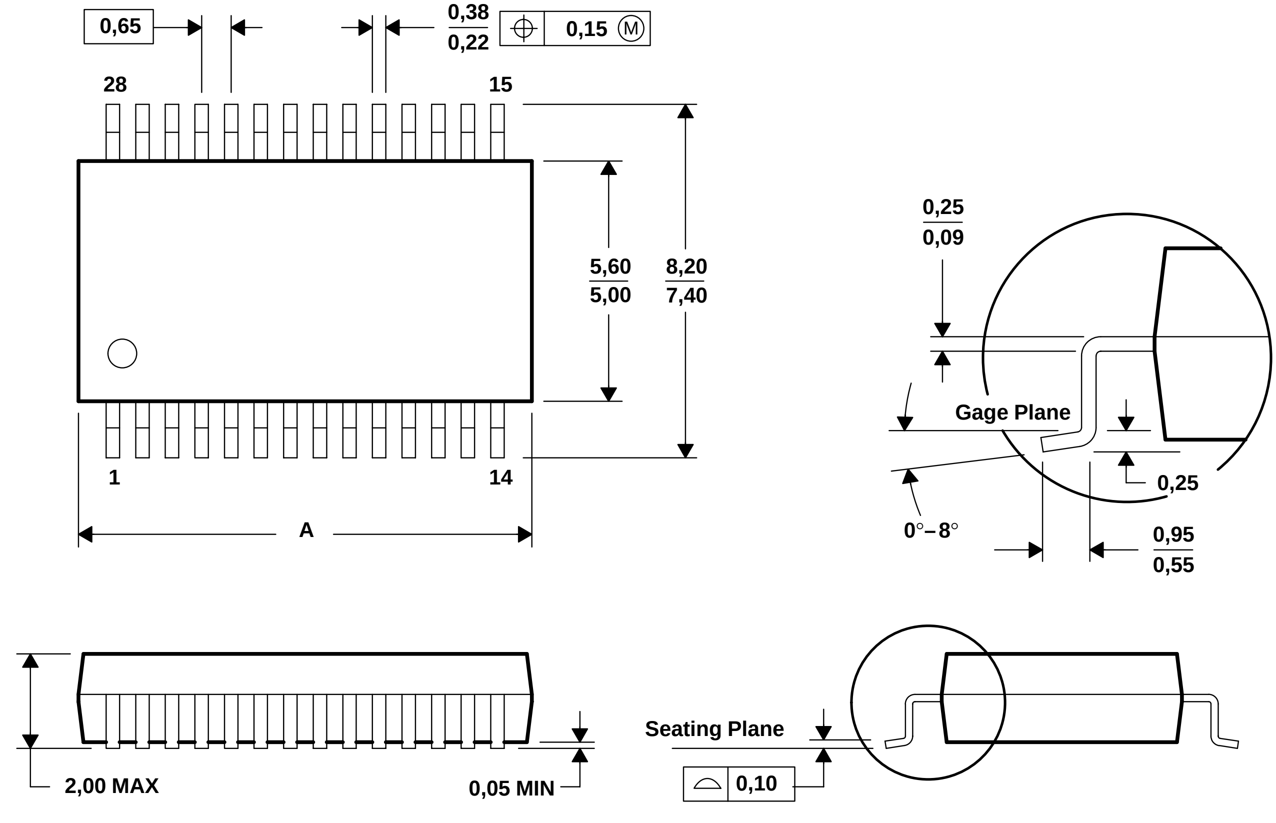
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



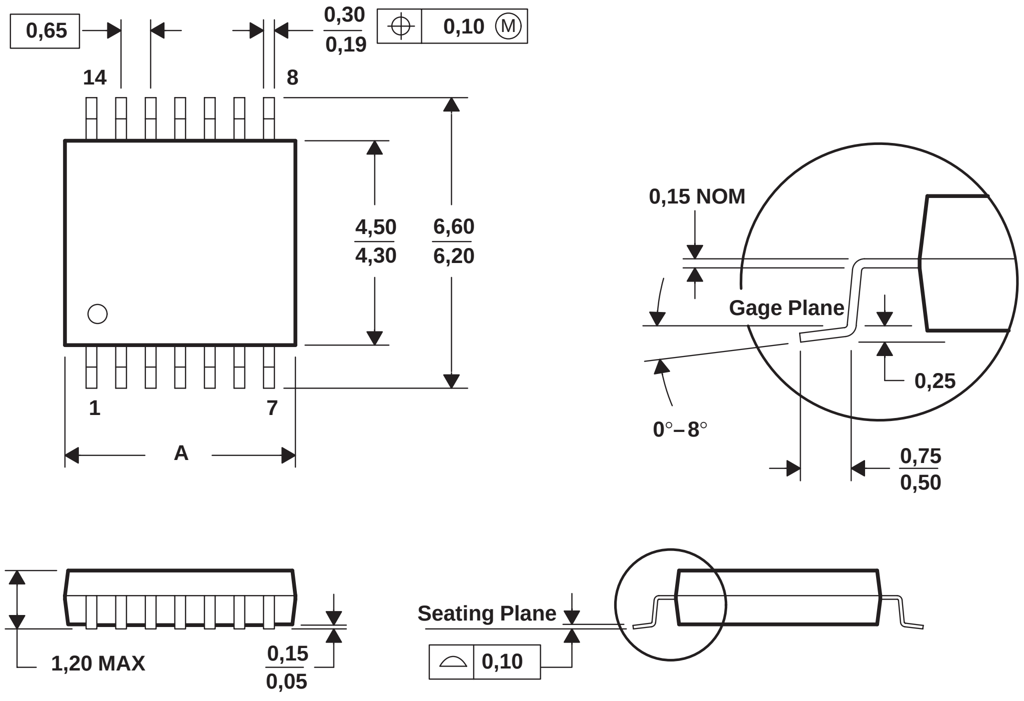
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM / PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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