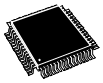
STM32F405xx
STM32F407xx

ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Features

- Core: ARM 32-bit Cortex™-M4F CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 1 Mbyte of Flash memory
  - Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
  - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.8 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M4F Embedded Trace Macrocell™



LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 × 24 mm)

UFBGA176
(10 × 10 mm)

- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 84 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
  - Up to 3 × I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPIs (37.5 Mbits/s), 2 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - 2 × CAN interfaces (2.0B Active)
  - SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Analog random number generator
- CRC calculation unit, 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F405xx	STM32F405RG, STM32F405VG, STM32F405ZG
STM32F407xx	STM32F407VG, STM32F407IG, STM32F407ZG, STM32F407VE, STM32F407ZE, STM32F407IE

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1 Introduction

This datasheet provides the description of the STM32F405xx and STM32F407xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F405xx and STM32F407xx datasheet should be read in conjunction with the STM32F4xx reference manual.

For information on programming, erasing and protection of the internal Flash memory, please refer to the STM32F4xx Flash programming manual (PM0081).

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex™-M4F core please refer to the Cortex™-M4F Technical Reference Manual, available from the *www.arm.com* website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0439b/.

2 Description

The STM32F405xx and STM32F407xx family is based on the high-performance ARM® Cortex™-M4F 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4F core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F405xx and STM32F407xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true number random generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Three SPIs, two I^2Ss full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F407xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors. Refer to *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts* for the list of peripherals available on each part number.

The STM32F405xx and STM32F407xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range and PDR_ON is connected to V_{SS}. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F405xx and STM32F407xx family offers devices in four packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F405xx and STM32F407xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 5 shows the general block diagram of the device family.

Table 2. STM32F405xx and STM32F407xx: features and peripheral counts

Peripherals		STM32F405RG	STM32F405VG	STM32F405ZG	STM32F407Vx		STM32F407Zx		STM32F407Ix	
Flash memory in Kbytes		1024			512	1024	512	1024	512	1024
SRAM in Kbytes	System	192(112+16+64)								
	Backup	4								
FSMC memory controller		No	Yes							
Ethernet		No			Yes					
Timers	General-purpose	10								
	Advanced-control	2								
	Basic	2								
Random number generator		Yes								
Communication interfaces	SPI / I^2S	3/2 (full duplex)								
	I^2C	3								
	USART/UART	4/2								
	USB OTG FS	Yes								
	USB OTG HS	Yes								
	CAN	2								
Camera interface		No			Yes					
GPIOs		51	82	114	82		114		140	
12-bit ADC Number of channels		3								
		16	16	24	16		24		24	
12-bit DAC Number of channels		Yes 2								
Maximum CPU frequency		168 MHz								
Operating voltage		1.8 to 3.6 V(1)								

Table 2. STM32F405xx and STM32F407xx: features and peripheral counts (continued)

Peripherals	STM32F405RG	STM32F405VG	STM32F405ZG	STM32F407Vx	STM32F407Zx	STM32F407Ix
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C					
	Junction temperature: –40 to + 125 °C					
Package	LQFP64	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176 LQFP176

1. V_{DD} minimum value of 1.7 V is obtained when the device operates in the 0 to 70 °C temperature range and PDR_ON is connected to V_{SS}.

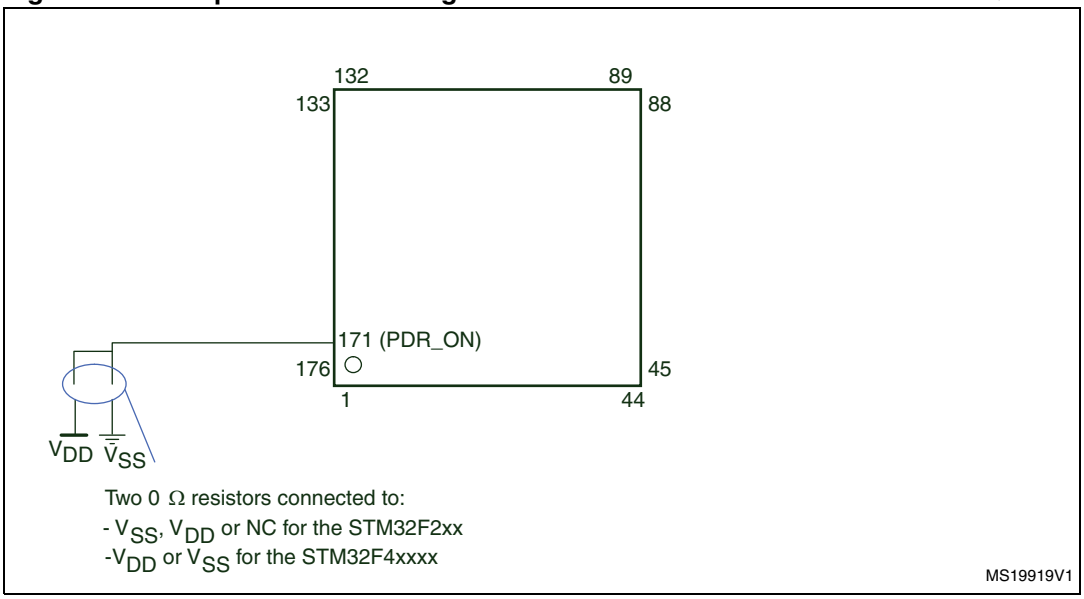
2.1 Full compatibility throughout the family

The STM32F405xx and STM32F407xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F405xx and STM32F407xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F405xx and STM32F407xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F40x family remains simple as only a few pins are impacted.

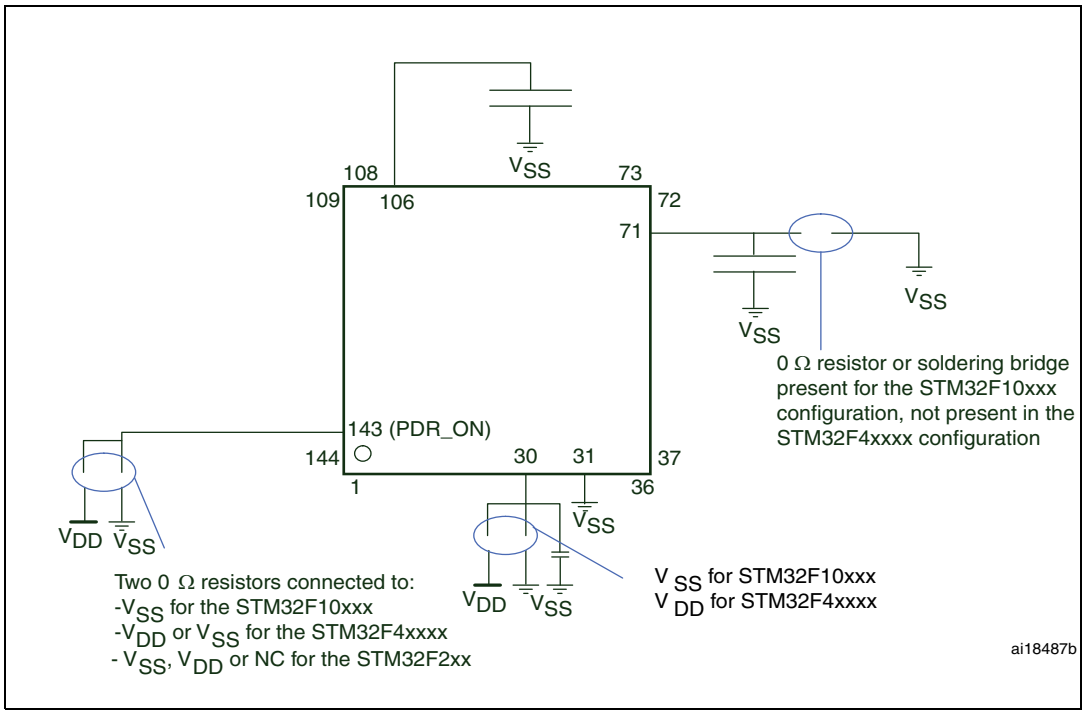
Figure 1, *Figure 2*, *Figure 3*, and *Figure 4* give compatible board designs between the STM32F40x, STM32F2xxx, and STM32F10xxx families.

Figure 1. Compatible board design between STM32F2xx and STM32F4xx: LQFP176



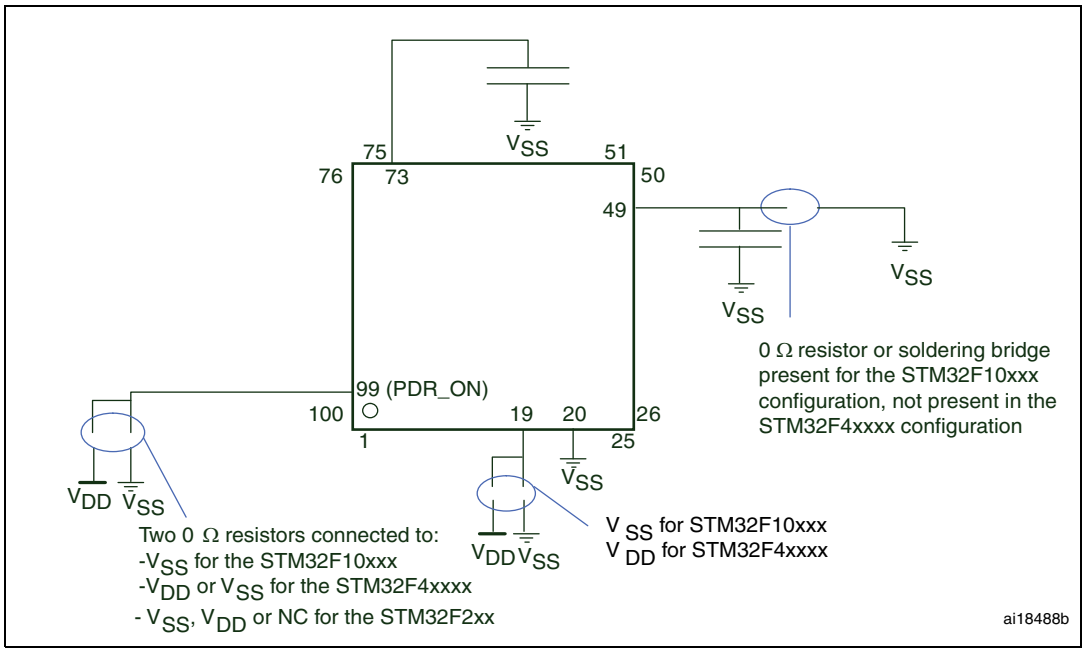
1. By default, PDR_ON (pin 171) should be connected to V_{DD}.
2. Pin 171 is RFU for STM32F2xx.

Figure 2. Compatible board design between STM32F1xx/STM32F2xx/ STM32F4xx: LQFP144



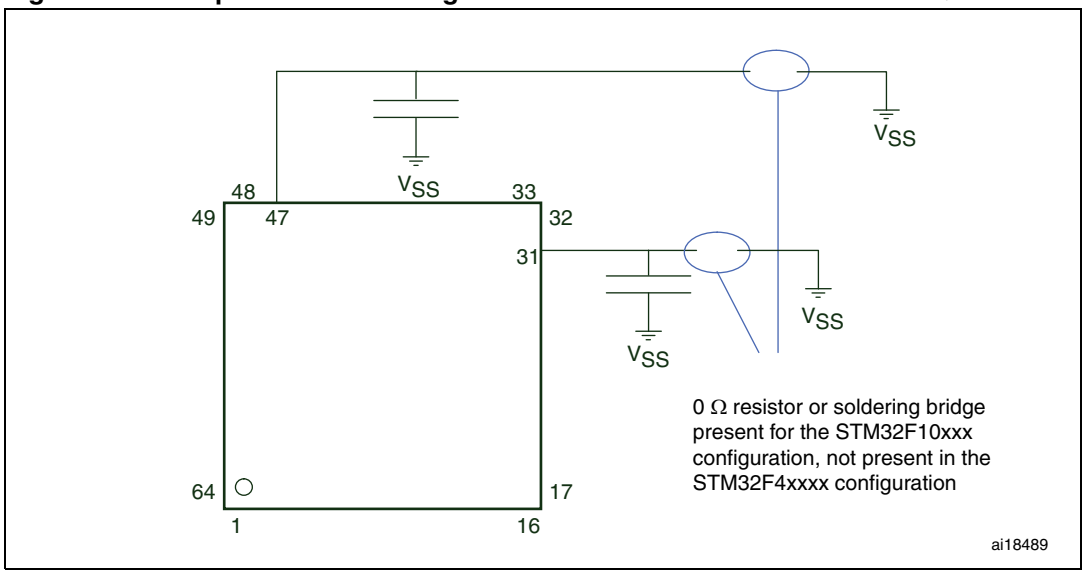
1. By default, PDR_ON (pin 143) should be connected to V_{DD}.
2. Pin 143 is RFU for STM32F2xx.

Figure 3. Compatible board design STM32F1xx/STM32F2xx/ STM32F4xx: LQFP100



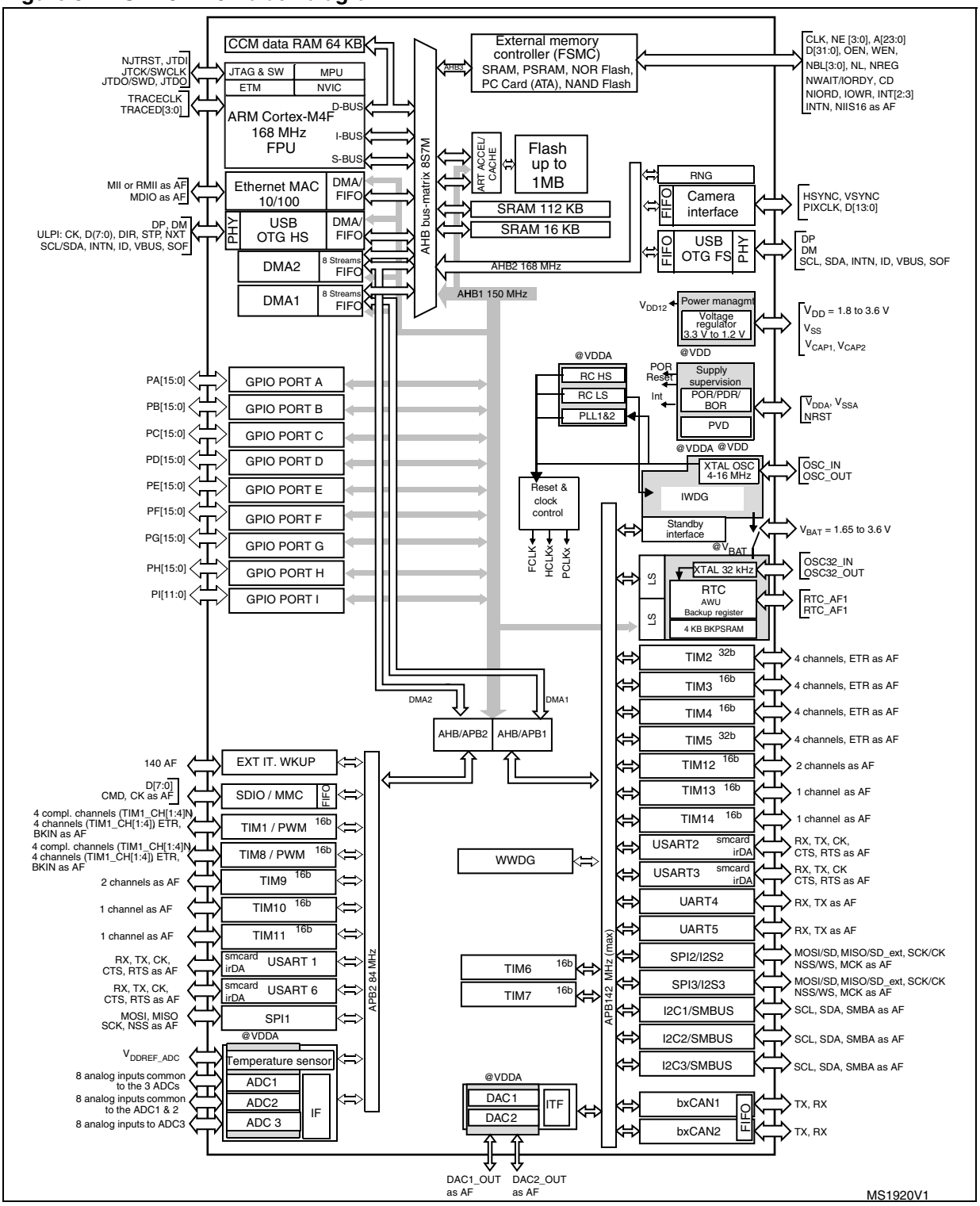
1. By default, PDR_ON (pin 99) should be connected to V_{DD}.
2. Pin 99 is RFU for STM32F2xx.

Figure 4. Compatible board design between STM32F1xx/STM32F4xx: LQFP64



2.2 Device overview

Figure 5. STM32F40x block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 168 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 84 MHz.

2.2.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F405xx and STM32F407xx family is compatible with all ARM tools and software.

Figure 5 shows the general block diagram of the STM32F40x family.

Note: Cortex-M4F is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex™-M4F processors. It balances the inherent performance advantage of the ARM Cortex-M4F over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F40x devices embed a Flash memory of 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

All STM32F40x products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

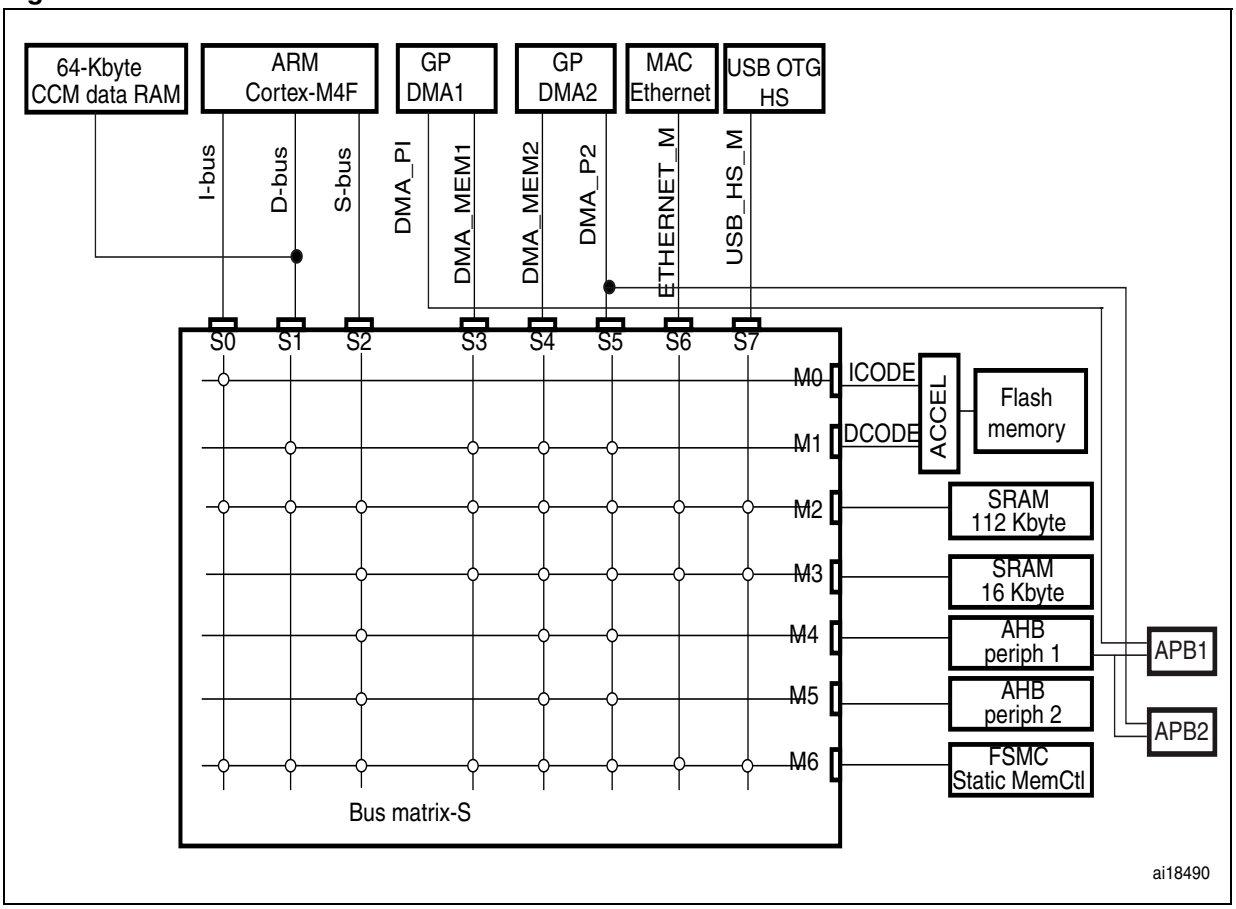
  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. Multi-AHB matrix



2.2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC.

2.2.9 Flexible static memory controller (FSMC)

The FSMC is embedded in the STM32F405xx and STM32F407xx family. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Maximum frequency (f_{CLK}) for external access is 60 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.2.10 Nested vectored interrupt controller (NVIC)

The STM32F405xx and STM32F407xx embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 87 maskable interrupt channels plus the 16 interrupt lines of the Cortex™-M4F.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.2.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a

pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

2.2.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select the system clock between the RC oscillator and an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 168 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB6), USB OTG FS in Device mode (PA9/PA11/PA12) through DFU (device firmware upgrade).

2.2.14 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to *Figure 18: Power supply scheme* for more details.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in the 0 to 70 °C temperature range with PDR_ON connected to V_{SS}.

2.2.15 Power supply supervisor

The power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

All packages, except the LQFP64, offer the internal reset is controlled through the PDR_ON signal.

2.2.16 Voltage regulator

The regulator has eight operating modes:

- Regulator ON/internal reset ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator ON/internal reset OFF
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF/internal reset ON
- Regulator OFF/internal reset OFF

Regulator ON

- Regulator ON/internal reset ON

  The regulator ON/internal reset ON mode is always enabled on LQFP64 package.

  On LQFP100 and LQFP144 packages, this mode is activated by setting PDR_ON to V_{DD}.

  On UFBGA176 package, the internal regulator must be activated by connecting BYPASS_REG to $V_{SS,}$ and PDR_ON to V_{DD}.

  On LQFP176 packages, the internal reset must be activated by connecting PDR_ON to V_{DD}.

V_{DD} minimum value is 1.8 V[(a)].

There are three low-power modes:

– MR is used in the nominal regulation mode (Run)

– LPR is used in the Stop modes

– Power-down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

- Regulator ON/internal reset OFF

  The regulator ON with internal reset OFF mode is not available on LQFP64 package.

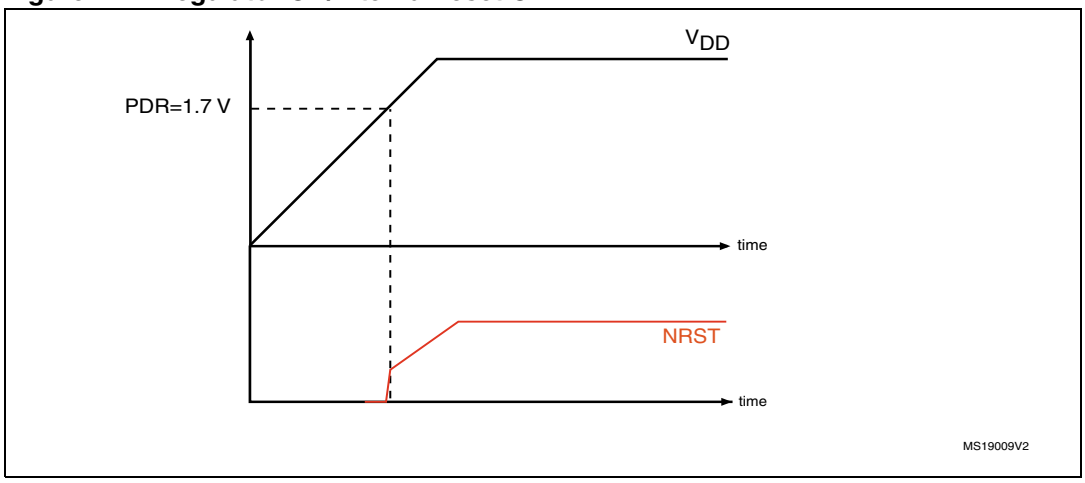
  On LQFP100 and LQFP144 packages, the internal reset is controlled by setting PDR_ON pin to V_{SS}.

  On UFBGA176 package, the internal regulator must be activated by connecting BYPASS_REG to V_{SS}, and PDR_ON to V_{SS}.

  On LQFP176 packages, the internal reset must be activated by connecting PDR_ON to V_{SS}.

  The NRST pin should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.8 V (see *Figure 7*).

Figure 7. Regulator ON/internal reset OFF



a. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in the 0 to 70 °C temperature range and PDR_ON is connected to V_{SS}.

Regulator OFF

This mode allows to power the device as soon as V_{DD} reaches 1.8 V.

- Regulator OFF/internal reset ON

  This mode is available only on UFBGA package. It is activated by setting BYPASS_REG and PDR_ON pins to V_{DD}.

  The regulator OFF/internal reset ON mode allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

  The following conditions must be respected:

  – V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.

  – If the time for V_{CAP_1} and V_{CAP_2} to reach 1.08 V is faster than the time for V_{DD} to reach 1.8 V[(a)], then PA0 should be connected to the NRST pin (see *Figure 8*). Otherwise, PA0 should be asserted low externally during POR until V_{DD} reaches 1.8 V (see *Figure 9*).

  – If V_{CAP_1} and V_{CAP_2} go below 1.08 V and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

  In regulator OFF/internal reset ON mode, PA0 cannot be used as a GPIO pin since it allows to reset the part of the 1.2 V logic which is not reset by the NRST pin, when the internal voltage regulator in off.

- Regulator OFF/internal reset OFF

  This mode is available only on UFBGA package. It is activated by setting BYPASS_REG pin to V_{DD} and by applying an inverted reset signal to PDR_ON, and allows to supply externally a 1.2 V voltage source through V_{CAP_1} and V_{CAP_2} pins, in addition to V_{DD}.

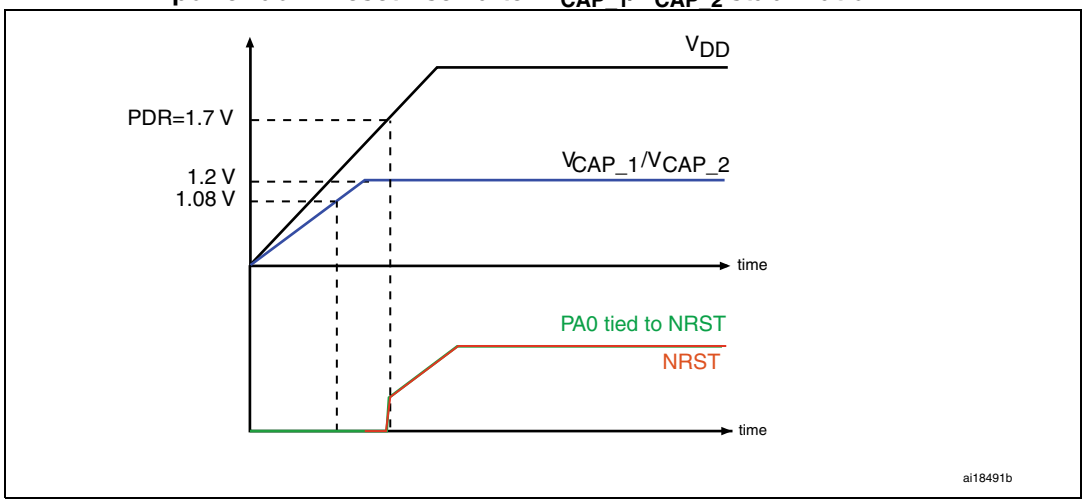
  The following conditions must be respected:

  – V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.

  – PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach 1.08 V and until V_{DD} reaches 1.8 V (see *Figure 8*).

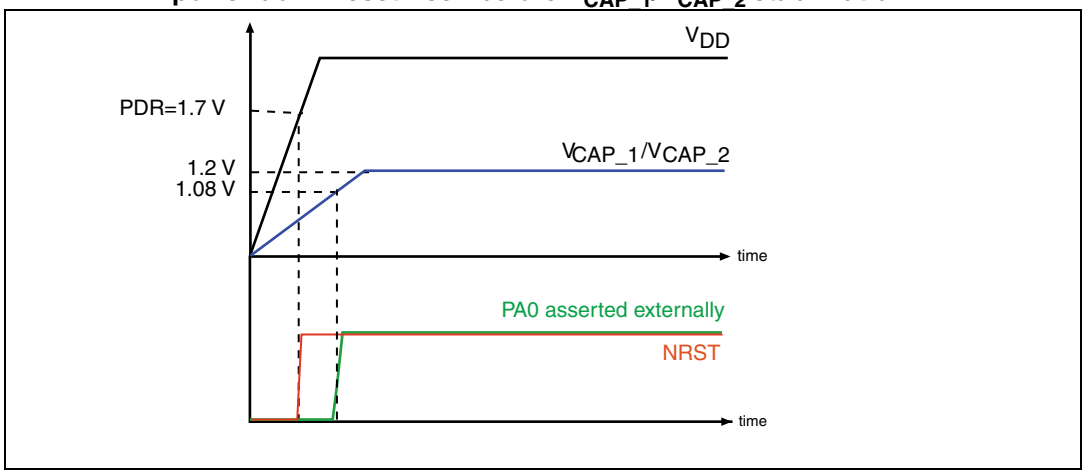
  – NRST should be controlled by an external reset controller to keep the device under reset when V_{DD} is below 1.8 V (see *Figure 9*).

Figure 8. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (on or off).

Figure 9. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (on or off).

2.2.17 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F405xx and STM32F407xx includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled by default to minimize power consumption (see *Section 2.2.18: Low-power modes*). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 2.2.18: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

2.2.18 Low-power modes

The STM32F405xx and STM32F407xx support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

Note: 1 When in Standby mode, only an RTC alarm/event or an external reset can wake up the device provided V_{DD} is supplied by an external battery.

2.2.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

2.2.20 Timers and watchdogs

The STM32F405xx and STM32F407xx devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	84	168
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	84	168
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	84	168
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	42	84
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	42	84
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	42	84

Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F40x devices (see *Table 3* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F40x include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

2.2.21 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.22 Universal synchronous/asynchronous receiver transmitters (USART)

The STM32F405xx and STM32F407xx embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The other available interfaces communicate at up to 5.25 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 4. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART3	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART4	X	-	-	-	-	-	2.62	5.25	APB1 (max. 42 MHz)
USART5	X	-	-	-	-	-	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)

2.2.23 Serial peripheral interface (SPI)

The STM32F40x feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 37.5 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.2.24 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

2.2.25 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

2.2.26 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.27 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F407xx devices.

The STM32F407xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F407xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F407xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the STM32F407xx.

The STM32F407xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F46x reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.2.28 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

2.2.29 Universal serial bus on-the-go full-speed (OTG_FS)

The STM32F405xx and STM32F407xx embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Internal FS OTG PHY support
- External FS OTG PHY support through an I^2C connection

2.2.30 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F405xx and STM32F407xx devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External FS OTG PHY support through an I^2C connection
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.2.31 Digital camera interface (DCMI)

The camera interface is *not* available in STM32F405xx devices.

STM32F407xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.2.32 Random number generator (RNG)

All STM32F405xx and STM32F407xx products embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.2.33 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 84 MHz.

2.2.34 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

2.2.35 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.2.36 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.2.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.2.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F40x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

3 Pinouts and pin description

Figure 10. STM32F40x LQFP64 pinout

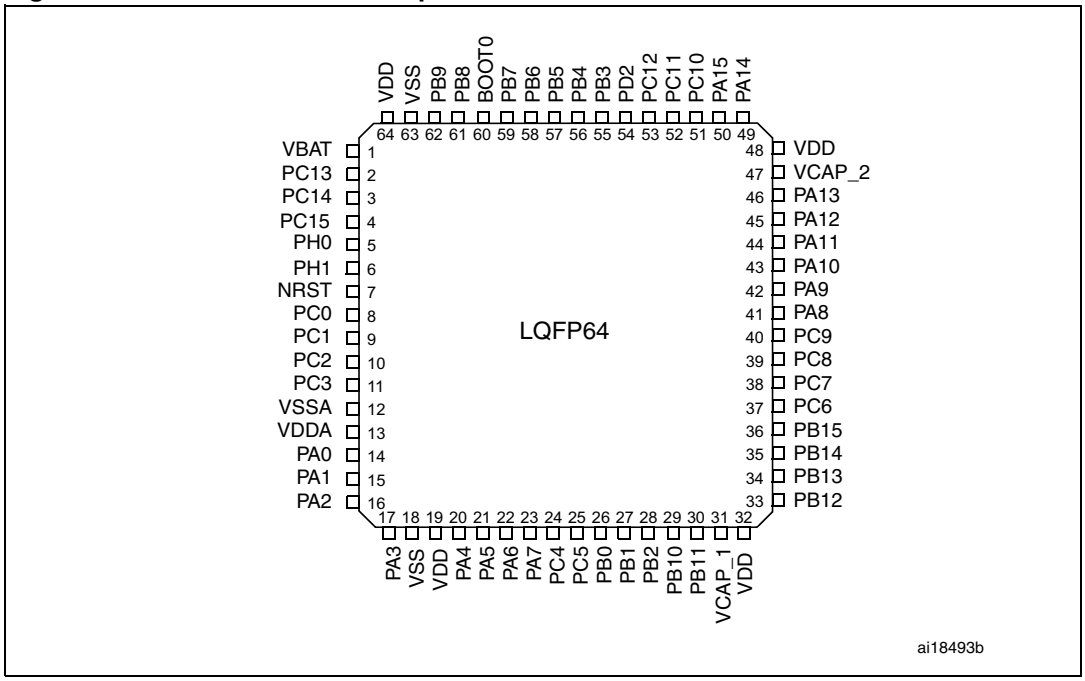


Figure 11. STM32F40x LQFP100 pinout

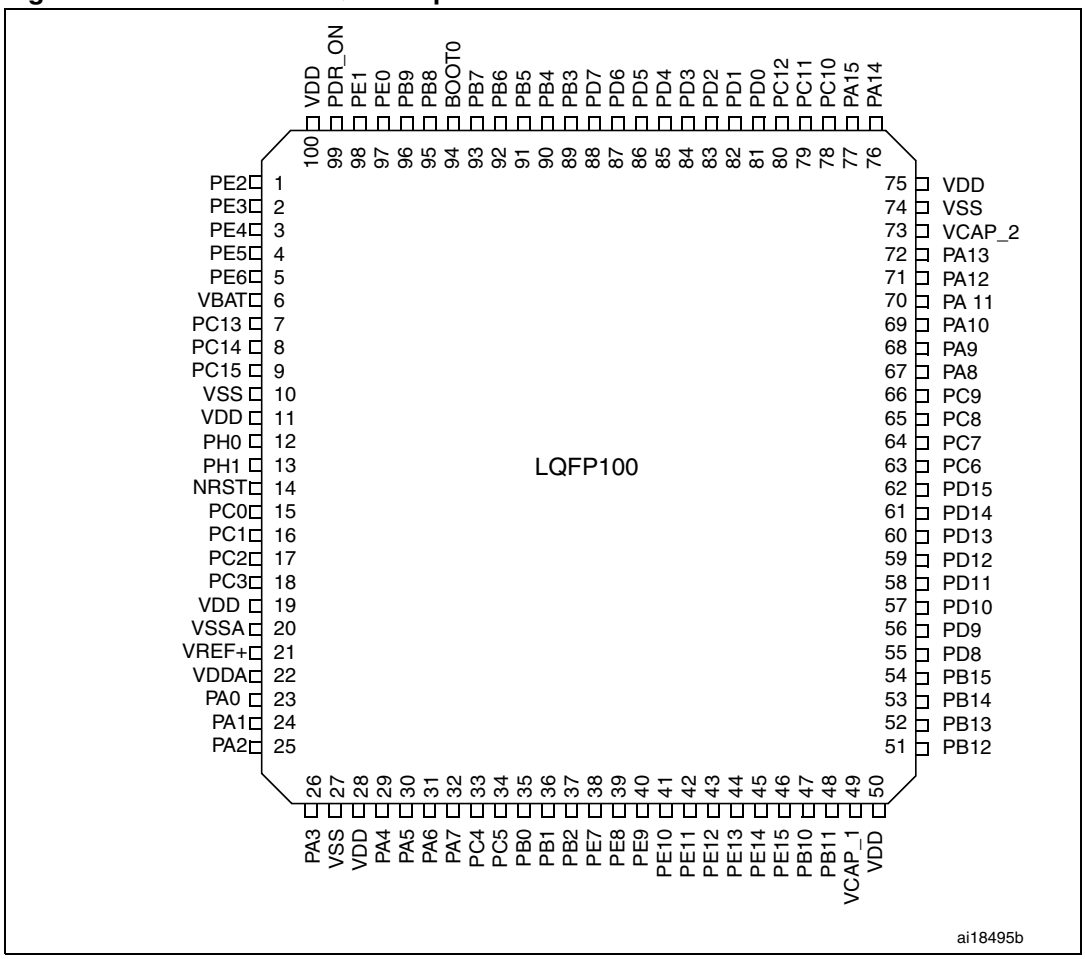


Figure 12. STM32F40x LQFP144 pinout

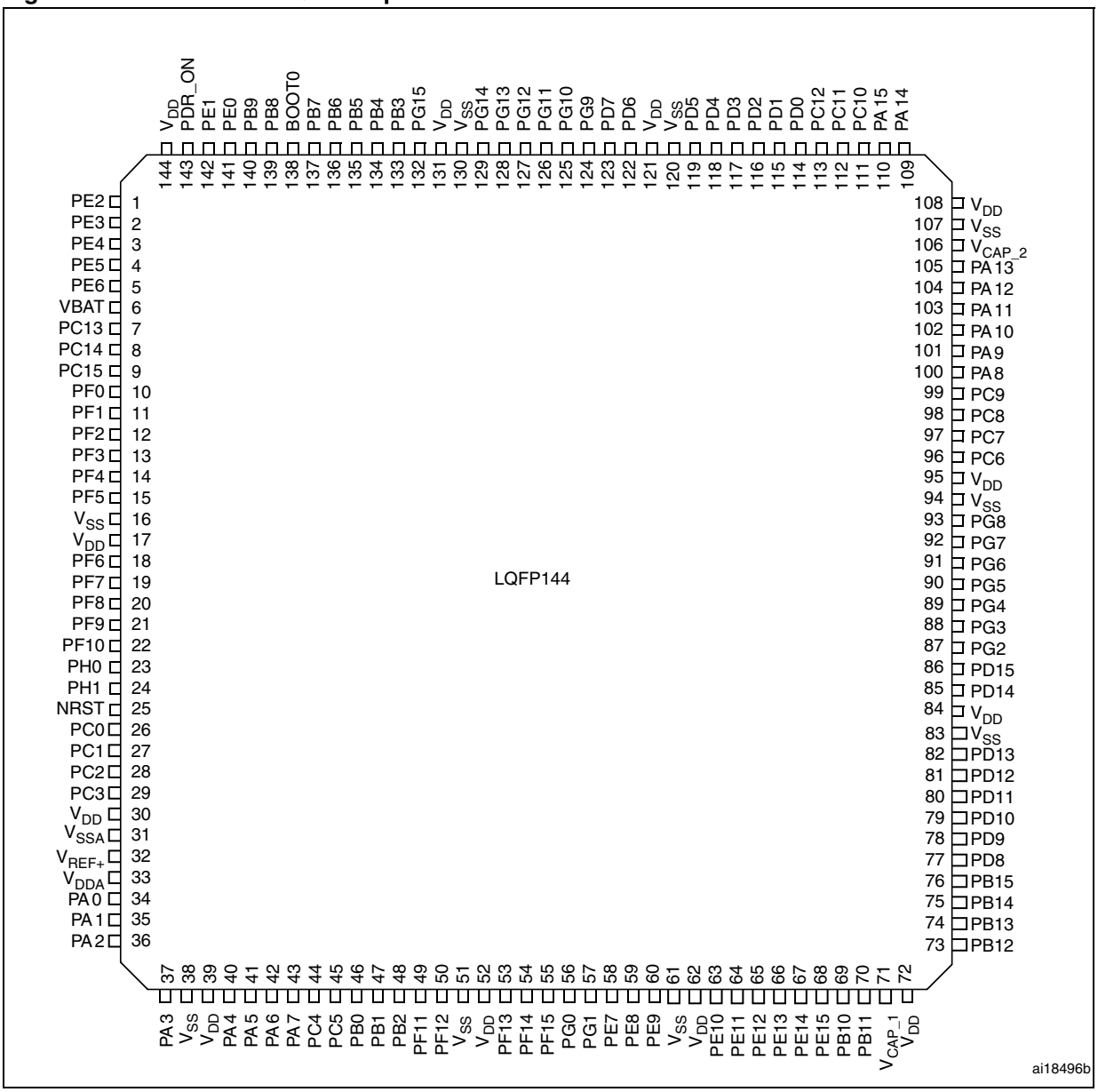


Figure 13. STM32F40x LQFP176 pinout

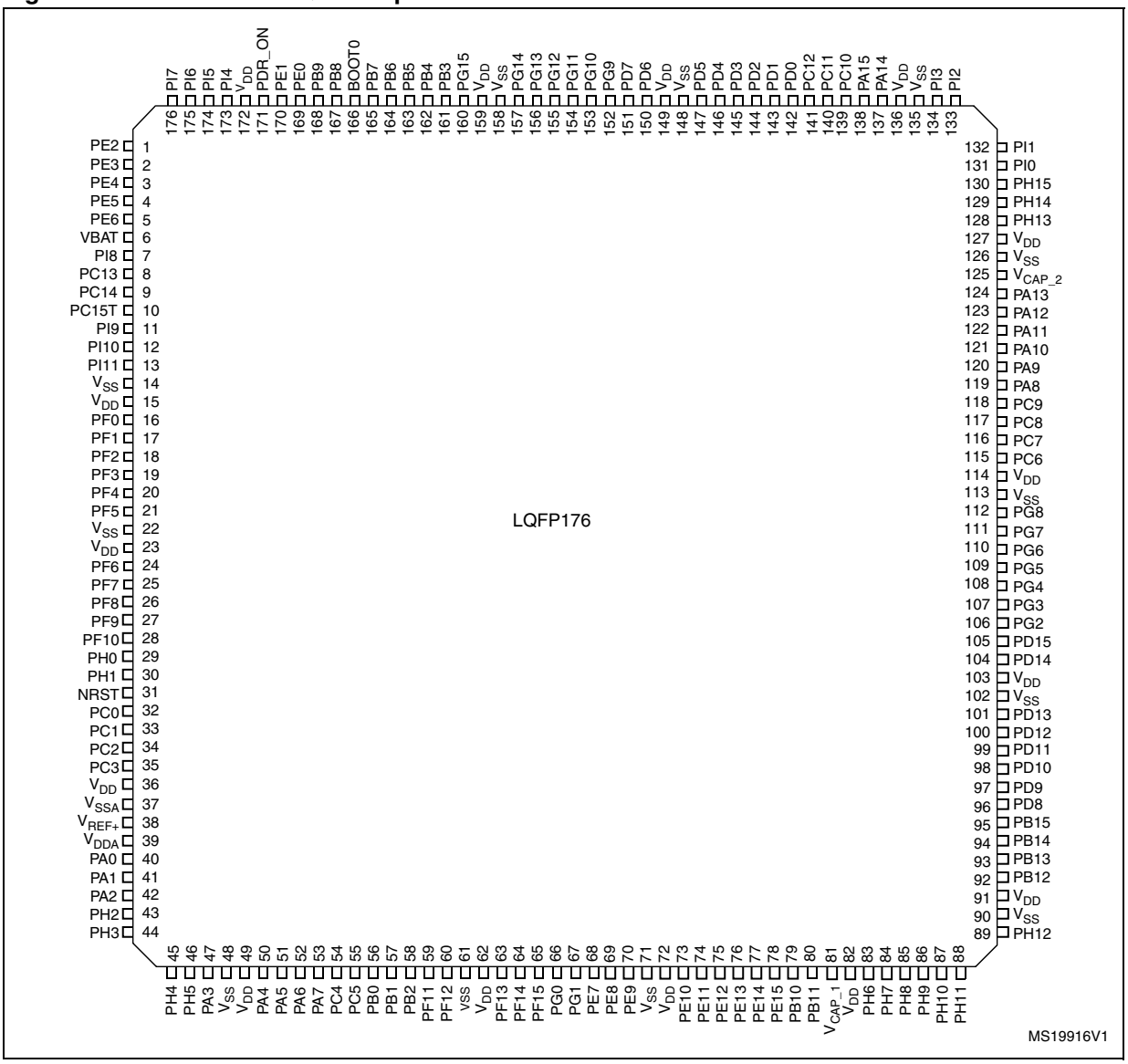


Figure 14. STM32F40x UFBGA176 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP_2	PC9	PA8
G	PH0	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	BYPASS_REG								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2	PC3	PB2	PG1	VSS	VSS	VCAP_1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

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Table 5. STM32F40x pin and ball definitions

Pins					Pin name	I / O Level	Function(1) after reset	Alternate functions(2)
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176				
-	1	1	A2	1	PE2	FT	PE2	TRACECLK/ FSMC_A23 / ETH_MII_TXD3
-	2	2	A1	2	PE3	FT	PE3	TRACED0/FSMC_A19
-	3	3	B1	3	PE4	FT	PE4	TRACED1/FSMC_A20 / DCMI_D4
-	4	4	B2	4	PE5	FT	PE5	TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6
-	5	5	B3	5	PE6	FT	PE6	TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7
1	6	6	C1	6	V_{BAT}		V_{BAT}	
-	-	-	D2	7	PI8(3)	FT	PI8(4)	**RTC_AF2**
2	7	7	D1	8	PC13(3)	FT	PC13(4)	**RTC_AF1**
3	8	8	E1	9	PC14(3)-OSC32_IN(5)	FT	PC14(4)	OSC32_IN
4	9	9	F1	10	PC15(3)-OSC32_OUT(5)	FT	PC15(4)	**OSC32_OUT**
-	-	-	D3	11	PI9	FT	PI9	CAN1_RX
-	-	-	E3	12	PI10	FT	PI10	ETH_MII_RX_ER
-	-	-	E4	13	PI11	FT	PI11	OTG_HS_ULPI_DIR
-	-	-	F2	14	V_{SS}		V_{SS}	
-	-	-	F3	15	V_{DD}		V_{DD}	
-	-	10	E2	16	PF0	FT	PF0	FSMC_A0 / I2C2_SDA
-	-	11	H3	17	PF1	FT	PF1	FSMC_A1 / I2C2_SCL
-	-	12	H2	18	PF2	FT	PF2	FSMC_A2 / I2C2_SMBA
-	-	13	J2	19	PF3(5)	FT	PF3	FSMC_A3/**ADC3_IN9**
-	-	14	J3	20	PF4(5)	FT	PF4	FSMC_A4/**ADC3_IN14**
-	-	15	K3	21	PF5(5)	FT	PF5	FSMC_A5/**ADC3_IN15**
-	10	16	G2	22	V_{SS}		V_{SS}	
-	11	17	G3	23	V_{DD}		V_{DD}	
-	-	18	K2	24	PF6(5)	FT	PF6	TIM10_CH1 / FSMC_NIORD/**ADC3_IN4**
-	-	19	K1	25	PF7(5)	FT	PF7	TIM11_CH1/FSMC_NREG/**ADC3_IN5**
-	-	20	L3	26	PF8(5)	FT	PF8	TIM13_CH1 / FSMC_NIOWR/**ADC3_IN6**
-	-	21	L2	27	PF9(5)	FT	PF9	TIM14_CH1 / FSMC_CD/**ADC3_IN7**
-	-	22	L1	28	PF10(5)	FT	PF10	FSMC_INTR
5	12	23	G1	29	PH0(5)-OSC_IN	FT	PH0	**OSC_IN**
6	13	24	H1	30	PH1(5)-OSC_OUT	FT	PH1	**OSC_OUT**
7	14	25	J1	31	NRST		NRST	
8	15	26	M2	32	PC0(5)	FT	PC0	OTG_HS_ULPI_STP/**ADC123_IN10**
9	16	27	M3	33	PC1(5)	FT	PC1	ETH_MDC/**ADC123_IN11**
10	17	28	M4	34	PC2(5)	FT	PC2	SPI2_MISO / OTG_HS_ULPI_DIR / TH_MII_TXD2 /I2S2ext_SD/**ADC123_IN12**
11	18	29	M5	35	PC3(5)	FT	PC3	SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK/**ADC123_IN13**

Table 5. STM32F40x pin and ball definitions (continued)

Pins					Pin name	I / O Level	Function[1] after reset	Alternate functions[2]
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176				
-	19	30	G3	36	V_{DD}		V_{DD}	
12	20	31	M1	37	V_{SSA}		V_{SSA}	
-	-	-	N1	-	V_{REF-}		V_{REF-}	
-	21	32	P1	38	V_{REF+}		V_{REF+}	
13	22	33	R1	39	V_{DDA}		V_{DDA}	
14	23	34	N3	40	PA0[6]-WKUP[5]	FT	PA0-WKUP	USART2_CTS/ USART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/**ADC123_IN0/WKUP**
15	24	35	N2	41	PA1[5]	FT	PA1	USART2_RTS / USART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIMM2_CH2/**ADC123_IN1**
16	25	36	P2	42	PA2[5]	FT	PA2	USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/**ADC123_IN2**
-	-	-	F4	43	PH2	FT	PH2	ETH_MII_CRS
-	-	-	G4	44	PH3	FT	PH3	ETH_MII_COL
-	-	-	H4	45	PH4	FT	PH4	I2C2_SCL / OTG_HS_ULPI_NXT
-	-	-	J4	46	PH5	FT	PH5	I2C2_SDA
17	26	37	R2	47	PA3[5]	FT	PA3	USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/**ADC123_IN3**
18	27	38	-	48	V_{SS_4}		V_{SS_4}	
			L4	-	BYPASS_REG		BYPASS_ REG	
19	28	39	K4	49	V_{DD}		V_{DD}	
20	29	40	N4	50	PA4[5]	FT	PA4	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/**ADC12_IN4 /DAC1_OUT**
21	30	41	P4	51	PA5[5]	FT	PA5	SPI1_SCK/ OTG_HS_ULPI_CK / / TIM2_CH1_ETR/ TIM8_CHIN/**ADC12_IN5/DAC2_OUT**
22	31	42	P3	52	PA6[5]	FT	PA6	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/**ADC12_IN6**
23	32	43	R3	53	PA7[5]	FT	PA7	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1 TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / RMII_CRS_DV/**ADC12_IN7**
24	33	44	N5	54	PC4[5]	FT	PC4	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ **ADC12_IN14**
25	34	45	P5	55	PC5[5]	FT	PC5	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ **ADC12_IN15**
26	35	46	R5	56	PB0[5]	FT	PB0	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/**ADC12_IN8**
27	36	47	R4	57	PB1[5]	FT	PB1	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / OTG_HS_INTN / TIM1_CH3N/**ADC12_IN9**
28	37	48	M6	58	PB2	FT	PB2-BOOT1	
-	-	49	R6	59	PF11	FT	PF11	DCMI_12
-	-	50	P6	60	PF12	FT	PF12	FSMC_A6
-	-	51	M8	61	V_{SS}		V_{SS}	

Table 5. STM32F40x pin and ball definitions (continued)

Pins					Pin name	I / O Level	Function[1] after reset	Alternate functions[2]
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176				
-	-	52	N8	62	V_{DD}		V_{DD}	
-	-	53	N6	63	PF13	FT	PF13	FSMC_A7
-	-	54	R7	64	PF14	FT	PF14	FSMC_A8
-	-	55	P7	65	PF15	FT	PF15	FSMC_A9
-	-	56	N7	66	PG0	FT	PG0	FSMC_A10
-	-	57	M7	67	PG1	FT	PG1	FSMC_A11
-	38	58	R8	68	PE7	FT	PE7	FSMC_D4/TIM1_ETR
-	39	59	P8	69	PE8	FT	PE8	FSMC_D5/ TIM1_CH1N
-	40	60	P9	70	PE9	FT	PE9	FSMC_D6/TIM1_CH1
-	-	61	M9	71	V_{SS}		V_{SS}	
-	-	62	N9	72	V_{DD}		V_{DD}	
-	41	63	R9	73	PE10	FT	PE10	FSMC_D7/TIM1_CH2N
-	42	64	P10	74	PE11	FT	PE11	FSMC_D8/TIM1_CH2
-	43	65	R10	75	PE12	FT	PE12	FSMC_D9/TIM1_CH3N
-	44	66	N11	76	PE13	FT	PE13	FSMC_D10/TIM1_CH3
-	45	67	P11	77	PE14	FT	PE14	FSMC_D11/TIM1_CH4
-	46	68	R11	78	PE15	FT	PE15	FSMC_D12/TIM1_BKIN
29	47	69	R12	79	PB10	FT	PB10	SPI2_SCK / I2S2_CK / I2C2_SCL/ USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / OTG_HS_SCL / TIM2_CH3
30	48	70	R13	80	PB11	FT	PB11	I2C2_SDA/USART3_RX/ OTG_HS_ULPI_D4 / ETH_RMII_TX_EN/ ETH_MII_TX_EN / OTG_HS_SDA / TIM2_CH4
31	49	71	M10	81	V_{CAP_1}		V_{CAP_1}	
32	50	72	N10	82	V_{DD}		V_{DD}	
-	-	-	M11	83	PH6	FT	PH6	I2C2_SMBA / TIM12_CH1 / ETH_MII_RXD2
-	-	-	N12	84	PH7	FT	PH7	I2C3_SCL / ETH_MII_RXD3
-	-	-	M12	85	PH8	FT	PH8	I2C3_SDA / DCMI_HSYNC
-	-	-	M13	86	PH9	FT	PH9	I2C3_SMBA / TIM12_CH2/ DCMI_D0
-	-	-	L13	87	PH10	FT	PH10	TIM5_CH1_ETR / DCMI_D1
-	-	-	L12	88	PH11	FT	PH11	TIM5_CH2 / DCMI_D2
-	-	-	K12	89	PH12	FT	PH12	TIM5_CH3 / DCMI_D3
-	-	-	H12	90	V_{SS}		V_{SS}	
-	-	-	J12	91	V_{DD}		V_{DD}	
33	51	73	P12	92	PB12	FT	PB12	SPI2_NSS / I2S2_WS / I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID
34	52	74	P13	93	PB13	FT	PB13	SPI2_SCK / I2S2_CK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1/ **OTG_HS_VBUS**

Table 5. STM32F40x pin and ball definitions (continued)

Pins					Pin name	I / O Level	Function[1] after reset	Alternate functions[2]
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176				
35	53	75	R14	94	PB14	FT	PB14	SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DMUSART3_RTS / TIM8_CH2N/I2S2ext_SD
36	54	76	R15	95	PB15	FT	PB15	SPI2_MOSI / I2S2_SD/ TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP
-	55	77	P15	96	PD8	FT	PD8	FSMC_D13 / USART3_TX
-	56	78	P14	97	PD9	FT	PD9	FSMC_D14 / USART3_RX
-	57	79	N15	98	PD10	FT	PD10	FSMC_D15 / USART3_CK
-	58	80	N14	99	PD11	FT	PD11	FSMC_A16/USART3_CTS
-	59	81	N13	100	PD12	FT	PD12	FSMC_A17/TIM4_CH1 / USART3_RTS
-	60	82	M15	101	PD13	FT	PD13	FSMC_A18/TIM4_CH2
-	-	83	-	102	V_{SS_8}		V_{SS_8}	
-	-	84	J13	103	V_{DD}		V_{DD}	
-	61	85	M14	104	PD14	FT	PD14	FSMC_D0/TIM4_CH3
-	62	86	L14	105	PD15	FT	PD15	FSMC_D1/TIM4_CH4
-	-	87	L15	106	PG2	FT	PG2	FSMC_A12
-	-	88	K15	107	PG3	FT	PG3	FSMC_A13
-	-	89	K14	108	PG4	FT	PG4	FSMC_A14
-	-	90	K13	109	PG5	FT	PG5	FSMC_A15
-	-	91	J15	110	PG6	FT	PG6	FSMC_INT2
-	-	92	J14	111	PG7	FT	PG7	FSMC_INT3 /USART6_CK
-	-	93	H14	112	PG8	FT	PG8	USART6_RTS / ETH_PPS_OUT
-	-	94	G12	113	V_{SS}		V_{SS}	
-	-	95	H13	114	V_{DD}		V_{DD}	
37	63	96	H15	115	PC6	FT	PC6	I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1
38	64	97	G15	116	PC7	FT	PC7	I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2
39	65	98	G14	117	PC8	FT	PC8	TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2
40	66	99	F14	118	PC9	FT	PC9	I2S_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / /I2C3_SDA / DCMI_D3 / TIM3_CH4
41	67	100	F15	119	PA8	FT	PA8	MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF
42	68	101	E15	120	PA9	FT	PA9	USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/**OTG_FS_VBUS**
43	69	102	D15	121	PA10	FT	PA10	USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1
44	70	103	C15	122	PA11	FT	PA11	USART1_CTS / CAN1_RX / TIM1_CH4 / OTG_FS_DM
45	71	104	B15	123	PA12	FT	PA12	USART1_RTS / CAN1_TX/ TIM1_ETR/ OTG_FS_DP
46	72	105	A15	124	PA13	FT	JTMS-SWDIO	JTMS-SWDIO
47	73	106	F13	125	V_{CAP_2}		V_{CAP_2}	
-	74	107	F12	126	V_{SS}		V_{SS}	

Table 5. STM32F40x pin and ball definitions (continued)

Pins					Pin name	I / O Level	Function[1] after reset	Alternate functions[2]
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176				
48	75	108	G13	127	V_{DD}		V_{DD}	
-	-	-	E12	128	PH13	FT	PH13	TIM8_CH1N / CAN1_TX
-	-	-	E13	129	PH14	FT	PH14	TIM8_CH2N / DCMI_D4
-	-	-	D13	130	PH15	FT	PH15	TIM8_CH3N / DCMI_D11
-	-	-	E14	131	PI0	FT	PI0	TIM5_CH4 / SPI2_NSS / I2S2_WS / DCMI_D13
-	-	-	D14	132	PI1	FT	PI1	SPI2_SCK / I2S2_CK / DCMI_D8
-	-	-	C14	133	PI2	FT	PI2	TIM8_CH4 /SPI2_MISO / DCMI_D9 / I2S2ext_SD
-	-	-	C13	134	PI3	FT	PI3	TIM8_ETR / SPI2_MOSI / I2S2_SD / DCMI_D10
-	-	-	D9	135	V_{SS}		V_{SS}	
-	-	-	C9	136	V_{DD}		V_{DD}	
49	76	109	A14	137	PA14	FT	JTCK-SWCLK	JTCK-SWCLK
50	77	110	A13	138	PA15	FT	JTDI	JTDI/ SPI3_NSS/ I2S3_WS/TIM2_CH1_ETR / SPI1_NSS
51	78	111	B14	139	PC10	FT	PC10	SPI3_SCK / I2S3_CK/ UART4_TX/SDIO_D2 / DCMI_D8 / USART3_TX
52	79	112	B13	140	PC11	FT	PC11	UART4_RX/ SPI3_MISO / SDIO_D3 / DCMI_D4/USART3_RX / I2S3ext_SD
53	80	113	A12	141	PC12	FT	PC12	UART5_TX/SDIO_CK / DCMI_D9 / SPI3_MOSI / I2S3_SD / USART3_CK
-	81	114	B12	142	PD0	FT	PD0	FSMC_D2/CAN1_RX
-	82	115	C12	143	PD1	FT	PD1	FSMC_D3 / CAN1_TX
54	83	116	D12	144	PD2	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD / DCMI_D11
-	84	117	D11	145	PD3	FT	PD3	FSMC_CLK/USART2_CTS
-	85	118	D10	146	PD4	FT	PD4	FSMC_NOE/USART2_RTS
-	86	119	C11	147	PD5	FT	PD5	FSMC_NWE/USART2_TX
-	-	120	D8	148	V_{SS}		V_{SS}	
-	-	121	C8	149	V_{DD}		V_{DD}	
-	87	122	B11	150	PD6	FT	PD6	FSMC_NWAIT/USART2_RX
-	88	123	A11	151	PD7	FT	PD7	USART2_CK/FSMC_NE1/FSMC_NCE2
-	-	124	C10	152	PG9	FT	PG9	USART6_RX / FSMC_NE2/ FSMC_NCE3
-	-	125	B10	153	PG10	FT	PG10	FSMC_NCE4_1/ FSMC_NE3
-	-	126	B9	154	PG11	FT	PG11	FSMC_NCE4_2 / ETH_MII_TX_EN/ ETH _RMII_TX_EN
-	-	127	B8	155	PG12	FT	PG12	FSMC_NE4 / USART6_RTS
-	-	128	A8	156	PG13	FT	PG13	FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ETH_RMII_TXD0
-	-	129	A7	157	PG14	FT	PG14	FSMC_A25 / USART6_TX /ETH_MII_TXD1/ETH_RMII_TXD1
-	-	130	D7	158	V_{SS}		V_{SS}	
-	-	131	C7	159	V_{DD}		V_{DD}	

Table 5. STM32F40x pin and ball definitions (continued)

Pins					Pin name	I / O Level	Function[1] after reset	Alternate functions[2]
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176				
-	-	132	B7	160	PG15	FT	PG15	USART6_CTS / DCMI_D13
55	89	133	A10	161	PB3	FT	JTDO/ TRACESWO	JTDO/ TRACESWO/ SPI3_SCK / I2S3_CK / TIM2_CH2 / SPI1_SCK
56	90	134	A9	162	PB4	FT	NJTRST	NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO / I2S3ext_SD
57	91	135	A6	163	PB5	FT	PB5	I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD
58	92	136	B6	164	PB6	FT	PB6	I2C1_SCL/ TIM4_CH1 / CAN2_TX /OTG_FS_INTN / DCMI_D5/USART1_TX
59	93	137	B5	165	PB7	FT	PB7	I2C1_SDA / FSMC_NL / DCMI_VSYNC / USART1_RX/ TIM4_CH2
60	94	138	D6	166	BOOT0		BOOT0	V_{PP}
61	95	139	A5	167	PB8	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / OTG_FS_SCL/ ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX
62	96	140	B4	168	PB9	FT	PB9	SPI2_NSS/ I2S2_WS / TIM4_CH4/ TIM11_CH1/ OTG_FS_SDA/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX
-	97	141	A4	169	PE0	FT	PE0	TIM4_ETR / FSMC_NBL0 / DCMI_D2
-	98	142	A3	170	PE1	FT	PE1	FSMC_NBL1 / DCMI_D3
63	-	-	D5	-	V_{SS_3}		V_{SS_3}	
-	99	143	C6	171	PDR_ON		PDR_ON	
64	100	144	C5	172	V_{DD}		V_{DD}	
-	-	-	D4	173	PI4	FT	PI4	TIM8_BKIN / DCMI_D5
-	-	-	C4	174	PI5	FT	PI5	TIM8_CH1 / DCMI_VSYNC
-	-	-	C3	175	PI6	FT	PI6	TIM8_CH2 / DCMI_D6
-	-	-	C2	176	PI7	FT	PI7	TIM8_CH3 / DCMI_D7

1. Function availability depends on the chosen device.
2. The functions in bold are remapped through peripheral registers.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F46x reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
6. If the device is delivered in an UFBGA176 and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low).

Table 6. Alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
PA0		TIM2_CH1 TIM2_ETR	TIM 5_CH1	TIM8_ETR				USART2_CTS	UART4_TX			ETH_MII_CRS				EVENTOUT
PA1		TIM2_CH2	TIM5_CH2					USART2_RTS	UART4_RX			ETH_MII _RX_CLK ETH_RMII _REF_CLK				EVENTOUT
PA2		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX				ETH_MDIO				EVENTOUT
PA3		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX			OTG_HS_ULPI_D0	ETH _MII_COL				EVENTOUT
PA4						SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK					OTG_HS_SOF	DCMI_HSYNC		EVENTOUT
PA5		TIM2_CH1 TIM2_ETR		TIM8_CH1N		SPI1_SCK					OTG_HS_ULPI_CK					EVENTOUT
PA6		TIM1_BKIN	TIM3_CH1	TIM8_BKIN		SPI1_MISO				TIM13_CH1				DCMI_PIXCK		EVENTOUT
PA7		TIM1_CH1N	TIM3_CH2	TIM8_CH1N		SPI1_MOSI				TIM14_CH1		ETH_MII _RX_DV ETH_RMII _CRS_DV				EVENTOUT
PA8	MCO1	TIM1_CH1			I2C3_SCL			USART1_CK			OTG_FS_SOF					EVENTOUT
PA9		TIM1_CH2			I2C3_SMBA			USART1_TX						DCMI_D0		EVENTOUT
PA10		TIM1_CH3						USART1_RX			OTG_FS_ID			DCMI_D1		EVENTOUT
PA11		TIM1_CH4						USART1_CTS		CAN1_RX	OTG_FS_DM					EVENTOUT
PA12		TIM1_ETR						USART1_RTS		CAN1_TX	OTG_FS_DP					EVENTOUT
PA13	JTMS-SWDIO															EVENTOUT
PA14	JTCK-SWCLK															EVENTOUT
PA15	JTDI	TIM 2_CH1 TIM 2_ETR				SPI1_NSS	SPI3_NSS/ I2S3S_WS									EVENTOUT
PB0		TIM1_CH2N	TIM3_CH3	TIM8_CH2N							OTG_HS_ULPI_D1	ETH _MII_RXD2				EVENTOUT
PB1		TIM1_CH3N	TIM3_CH4	TIM8_CH3N							OTG_HS_ULPI_D2	ETH _MII_RXD3	OTG_HS_INTN			EVENTOUT
PB2																EVENTOUT
PB3	JTDO/ TRACESWO	TIM2_CH2				SPI1_SCK	SPI3_SCK I2S3_CK									EVENTOUT
PB4	JTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO	I2S3ext_SD								EVENTOUT
PB5			TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD			CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT		DCMI_D10		EVENTOUT
PB6			TIM4_CH1		I2C1_SCL	I2S2_WS		USART1_TX		CAN2_TX	OTG_FS_INTN			DCMI_D5		EVENTOUT
PB7			TIM4_CH2		I2C1_SDA			USART1_RX					FSMC_NL	DCMI_VSYNC		EVENTOUT
PB8			TIM4_CH3	TIM10_CH1	I2C1_SCL					CAN1_RX	OTG_FS_SCL	ETH _MII_TXD3	SDIO_D4	DCMI_D6		EVENTOUT
PB9			TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS				CAN1_TX	OTG_FS_SDA		SDIO_D5	DCMI_D7		EVENTOUT
PB10		TIM2_CH3			I2C2_SCL	SPI2_SCK I2S2_CK		USART3_TX			OTG_HS_ULPI_D3	ETH_ MII_RX_ER	OTG_HS_SCL			EVENTOUT
PB11		TIM2_CH4			I2C2_SDA			USART3_RX			OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN	OTG_HS_SDA			EVENTOUT
PB12		TIM1_BKIN			I2C2_SMBA	SPI2_NSS I2S2_WS		USART3_CK		CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID			EVENTOUT
PB13		TIM1_CH1N				SPI2_SCK I2S2_CK		USART3_CTS		CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1				EVENTOUT
PB14		TIM1_CH2N		TIM8_CH2N		SPI2_MISO	I2S2ext_SD	USART3_RTS		TIM12_CH1			OTG_HS_DM			EVENTOUT

Table 6. Alternate function mapping (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
PB15	RTC_50Hz	TIM1_CH3N		TIM8_CH3N		SPI2_MOSI I2S2_SD				TIM12_CH2			OTG_HS_DP			EVENTOUT
PC0											OTG_HS_ULPI_STP					EVENTOUT
PC1												ETH_MDC				EVENTOUT
PC2						SPI2_MISO	I2S2ext_SD				OTG_HS_ULPI_DIR	ETH _MII_TXD2				EVENTOUT
PC3						SPI2_MOSI I2S2_SD					OTG_HS_ULPI_NXT	ETH _MII_TX_CLK ETH _RMII_TX_CLK				EVENTOUT
PC4												ETH_MII_RXD0 ETH_RMII_RXD0				EVENTOUT
PC5												ETH _MII_RXD1 ETH _RMII_RXD1				EVENTOUT
PC6			TIM3_CH1	TIM8_CH1		I2S2_MCK			USART6_TX				SDIO_D6	DCMI_D0		EVENTOUT
PC7			TIM3_CH2	TIM8_CH2			I2S3_MCK		USART6_RX				SDIO_D7	DCMI_D1		EVENTOUT
PC8			TIM3_CH3	TIM8_CH3					USART6_CK				SDIO_D0	DCMI_D2		EVENTOUT
PC9	MCO2		TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN							SDIO_D1	DCMI_D3		EVENTOUT
PC10							SPI3_SCK/ I2S3S_CK	USART3_TX/	UART4_TX				SDIO_D2	DCMI_D8		EVENTOUT
PC11							SPI3_MISO I2S3ext_SD/	USART3_RX	UART4_RX				SDIO_D3	DCMI_D4		EVENTOUT
PC12							SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX				SDIO_CK	DCMI_D9		EVENTOUT
PC13																
PC14																
PC15																
PD0										CAN1_RX			FSMC_D2			EVENTOUT
PD1										CAN1_TX			FSMC_D3			EVENTOUT
PD2			TIM3_ETR						UART5_RX				SDIO_CMD	DCMI_D11		EVENTOUT
PD3								USART2_CTS					FSMC_CLK			EVENTOUT
PD4								USART2_RTS					FSMC_NOE			EVENTOUT
PD5								USART2_TX					FSMC_NWE			EVENTOUT
PD6								USART2_RX					FSMC_NWAIT			EVENTOUT
PD7								USART2_CK					FSMC_NE1/ FSMC_NCE2			EVENTOUT
PD8								USART3_TX					FSMC_D13			EVENTOUT
PD9								USART3_RX					FSMC_D14			EVENTOUT
PD10								USART3_CK					FSMC_D15			EVENTOUT
PD11								USART3_CTS					FSMC_A16			EVENTOUT
PD12			TIM4_CH1					USART3_RTS					FSMC_A17			EVENTOUT
PD13			TIM4_CH2										FSMC_A18			EVENTOUT
PD14			TIM4_CH3										FSMC_D0			EVENTOUT

Table 6. Alternate function mapping (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
PD15			TIM4_CH4										FSMC_D1			EVENTOUT
PE0			TIM4_ETR										FSMC_NBL0	DCMI_D2		EVENTOUT
PE1													FSMC_BLN1	DCMI_D3		EVENTOUT
PE2	TRACECLK											ETH _MII_TXD3	FSMC_A23			EVENTOUT
PE3	TRACED0												FSMC_A19			EVENTOUT
PE4	TRACED1												FSMC_A20	DCMI_D4		EVENTOUT
PE5	TRACED2			TIM9_CH1									FSMC_A21	DCMI_D6		EVENTOUT
PE6	TRACED3			TIM9_CH2									FSMC_A22	DCMI_D7		EVENTOUT
PE7		TIM1_ETR											FSMC_D4			EVENTOUT
PE8		TIM1_CH1N											FSMC_D5			EVENTOUT
PE9		TIM1_CH1											FSMC_D6			EVENTOUT
PE10		TIM1_CH2N											FSMC_D7			EVENTOUT
PE11		TIM1_CH2											FSMC_D8			EVENTOUT
PE12		TIM1_CH3N											FSMC_D9			EVENTOUT
PE13		TIM1_CH3											FSMC_D10			EVENTOUT
PE14		TIM1_CH4											FSMC_D11			EVENTOUT
PE15		TIM1_BKIN											FSMC_D12			EVENTOUT
PF0					I2C2_SDA								FSMC_A0			EVENTOUT
PF1					I2C2_SCL								FSMC_A1			EVENTOUT
PF2					I2C2_SMBA								FSMC_A2			EVENTOUT
PF3													FSMC_A3			EVENTOUT
PF4													FSMC_A4			EVENTOUT
PF5													FSMC_A5			EVENTOUT
PF6				TIM10_CH1									FSMC_NIORD			EVENTOUT
PF7				TIM11_CH1									FSMC_NREG			EVENTOUT
PF8										TIM13_CH1			FSMC_NIOWR			EVENTOUT
PF9										TIM14_CH1			FSMC_CD			EVENTOUT
PF10													FSMC_INTR			EVENTOUT
PF11														DCMI_D12		EVENTOUT
PF12													FSMC_A6			EVENTOUT
PF13													FSMC_A7			EVENTOUT
PF14													FSMC_A8			EVENTOUT
PF15													FSMC_A9			EVENTOUT

Table 6. Alternate function mapping (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
PG0													FSMC_A10			EVENTOUT
PG1													FSMC_A11			EVENTOUT
PG2													FSMC_A12			EVENTOUT
PG3													FSMC_A13			EVENTOUT
PG4													FSMC_A14			EVENTOUT
PG5													FSMC_A15			EVENTOUT
PG6													FSMC_INT2			EVENTOUT
PG7									USART6_CK				FSMC_INT3			EVENTOUT
PG8									USART6_RTS			ETH _PPS_OUT				EVENTOUT
PG9									USART6_RX				FSMC_NE2/ FSMC_NCE3			EVENTOUT
PG10													FSMC_NCE4_1/ FSMC_NE3			EVENTOUT
PG11												ETH _MII_TX_EN ETH _RMII_TX_EN	FSMC_NCE4_2			EVENTOUT
PG12									USART6_RTS				FSMC_NE4			EVENTOUT
PG13									UART6_CTS			ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24			EVENTOUT
PG14									USART6_TX			ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25			EVENTOUT
PG15									USART6_CTS					DCMI_D13		EVENTOUT
PH0																
PH1																
PH2												ETH _MII_CRS				EVENTOUT
PH3												ETH _MII_COL				EVENTOUT
PH4					I2C2_SCL						OTG_HS_ULPI_NXT					EVENTOUT
PH5					I2C2_SDA											EVENTOUT
PH6					I2C2_SMBA					TIM12_CH1		ETH _MII_RXD2				EVENTOUT
PH7					I2C3_SCL							ETH _MII_RXD3				EVENTOUT
PH8					I2C3_SDA									DCMI_HSYNC		EVENTOUT
PH9					I2C3_SMBA					TIM12_CH2				DCMI_D0		EVENTOUT
PH10			TIM5_CH1TIM5_ETR											DCMI_D1		EVENTOUT
PH11			TIM5_CH2											DCMI_D2		EVENTOUT
PH12			TIM5_CH3											DCMI_D3		EVENTOUT
PH13				TIM8_CH1N						CAN1_TX						EVENTOUT
PH14				TIM8_CH2N										DCMI_D4		EVENTOUT

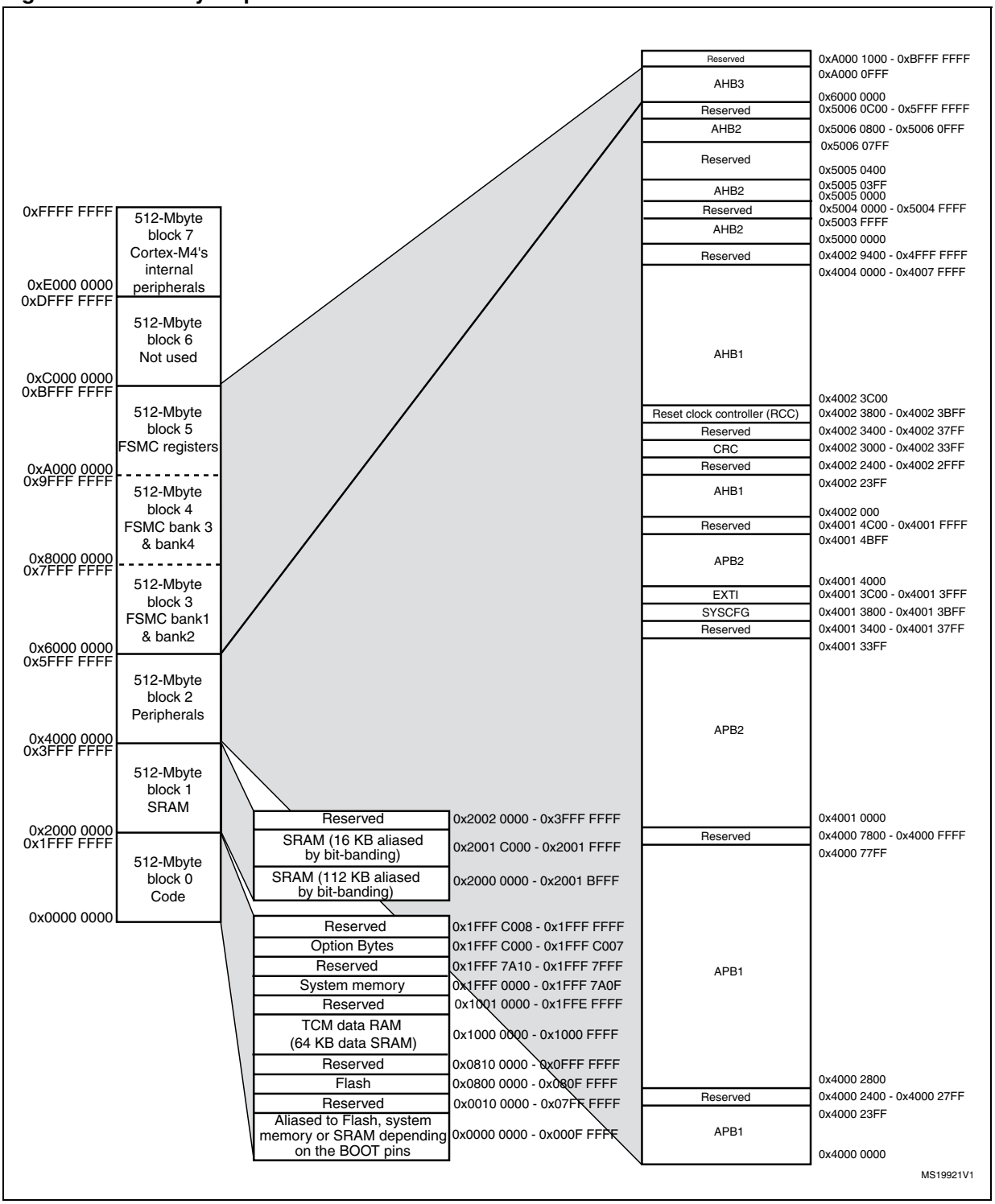
Table 6. Alternate function mapping (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
PH15				TIM8_CH3N										DCMI_D11		EVENTOUT
PI0			TIM5_CH4			SPI2_NSS I2S2_WS								DCMI_D13		EVENTOUT
PI1						SPI2_SCK I2S2_CK								DCMI_D8		EVENTOUT
PI2				TIM8_CH4		SPI2_MISO	I2S2ext_SD							DCMI_D9		EVENTOUT
PI3				TIM8_ETR		SPI2_MOSI I2S2_SD								DCMI_D10		EVENTOUT
PI4				TIM8_BKIN										DCMI_D5		EVENTOUT
PI5				TIM8_CH1										DCMI_VSYNC		EVENTOUT
PI6				TIM8_CH2										DCMI_D6		EVENTOUT
PI7				TIM8_CH3										DCMI_D7		EVENTOUT
PI8																
PI9										CAN1_RX						EVENTOUT
PI10												ETH _MII_RX_ER				EVENTOUT
PI11											OTG_HS_ULPI_DIR					EVENTOUT

4 Memory map

The memory map is shown in *Figure 15*.

Figure 15. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 16*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 16. Pin loading conditions

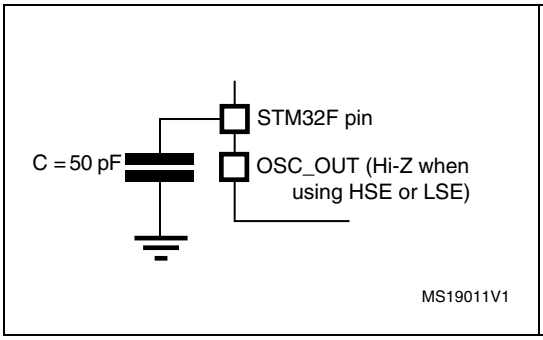
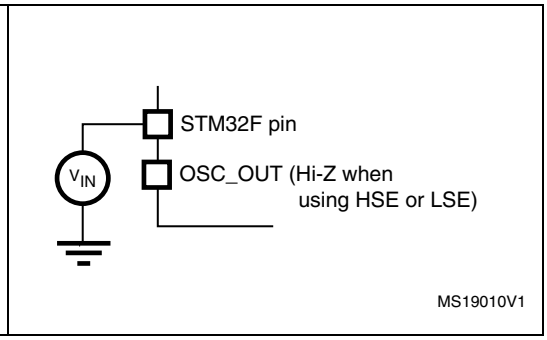
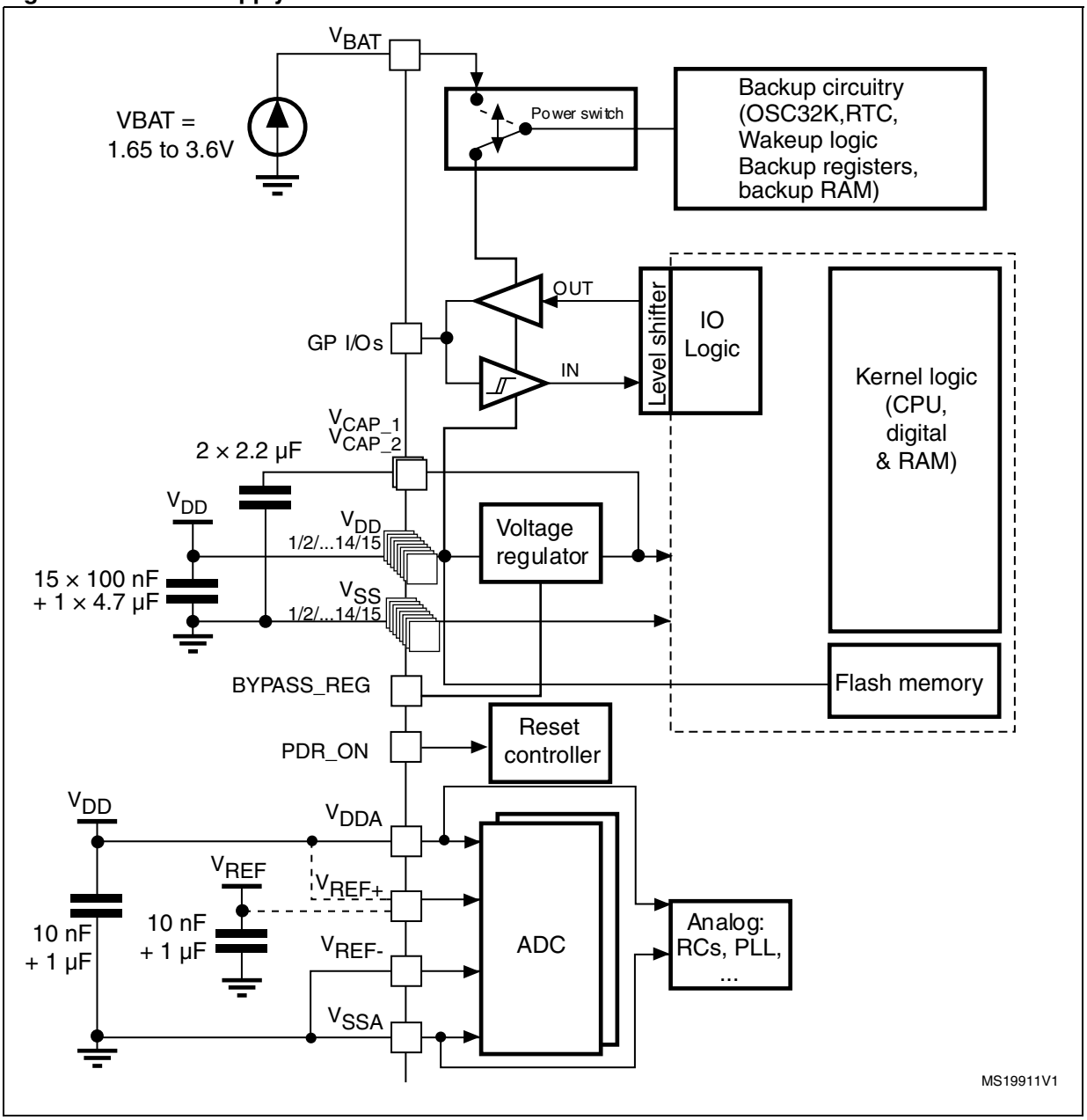


Figure 17. Pin input voltage



5.1.6 Power supply scheme

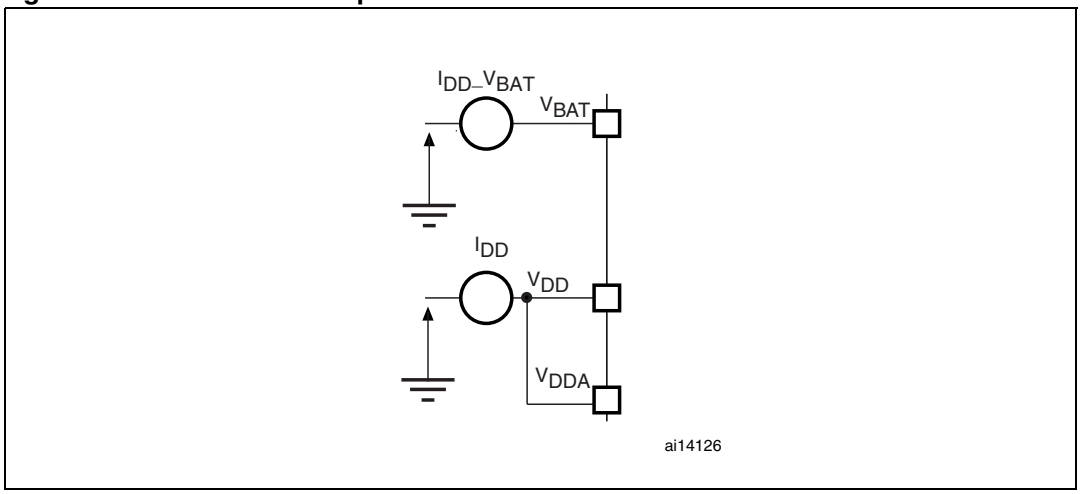
Figure 18. Power supply scheme



1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect BYPASS_REG and PDR_ON pins, refer to *Section 2.2.17: Real-time clock (RTC), backup SRAM and backup registers*.
3. The two 2.2 µF ceramic capacitors should not be connected when the voltage regulator is OFF.
4. The 4.7 µF ceramic capacitor must be connected to one of the VDDx pin.
5. $V_{DDA}=V_{DD}$ and $V_{SSA}=V_{SS}$.

5.1.7 Current consumption measurement

Figure 19. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 8* for the values of the maximum allowed injected current.

Table 8. Current characteristics(1)

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	TBD	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	TBD	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4)	–5/+0	
	Injected current on any other pin(5)	±5	
$\Sigma I_{INJ(PIN)}$(5)	Total injected current (sum of all I/O and control pins)(6)	±25	

1. TBD stands for “to be defined”.
2. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7* for the values of the maximum allowed input voltage.
5. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7* for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	VOS bit in PWR_CR = 0	0	144	MHz
		VOS bit in PWR_CR = 1	0	168	
f_{PCLK1}	Internal APB1 clock frequency		0	42	
f_{PCLK2}	Internal APB2 clock frequency		0	84	
V_{DD}	Standard operating voltage		1.8(2)	3.6	V
V_{DDA}(3)(4)	Analog operating voltage (ADC limited to 1 M samples)	Must be the same potential as V_{DD}(5)	1.8(2)	3.6	V
	Analog operating voltage (ADC limited to 2 M samples)		2.4	3.6	

Table 10. General operating conditions(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	Backup operating voltage		1.65	3.6	V
V_{CAP1}	When the internal regulator is ON, V_{CAP_1} and V_{CAP_2} pins are used to connect a stabilization capacitor. When the internal regulator is OFF (BYPASS_REG connected to V_{DD}), V_{CAP_1} and V_{CAP_2} must be supplied from 1.2 V.		1.1	1.3	V
V_{CAP2}					
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(6)	LQFP64	-	TBD	mW
		LQFP100	-	TBD	
		LQFP144	-	TBD	
		LQFP176	-	TBD	
		UFBGA176	-	TBD	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(7)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(7)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. TBD stands for “to be defined”.
2. If PDR_ON is set to V_{SS}, this value can be lowered to 1.7 V when the device operates in a reduced temperature range (0 to 70 °C).
3. When the ADC is used, refer to *Table 64: ADC characteristics*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
7. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 11. Limitations depending on the operating power supply range

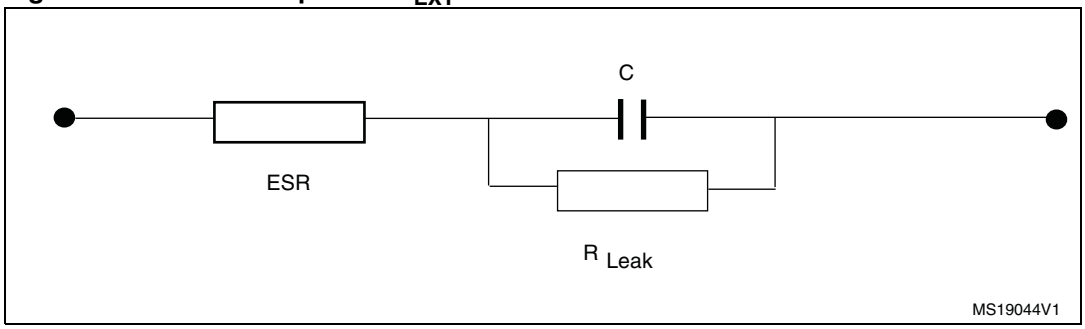
Operating power supply range	ADC operation	Maximum Flash memory access frequency ($f_{Flashmax}$)	Number of wait states at maximum CPU frequency(1)	I/O operation	FSMC controller operation	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(2)	Conversion time up to 1.2 Msps	16 MHz with no Flash memory wait state	TBD	– Degraded speed performance – No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	18 MHz with no Flash memory wait state	7(3)	– Degraded speed performance – No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz with no Flash memory wait state	6(3)	– Degraded speed performance – I/O compensation works	up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2.4 Msps	30 MHz with no Flash memory wait state	5(3)	– Full-speed operation – I/O compensation works	– up to 60 MHz when V_{DD} = 3.0 to 3.6 V – up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. The number of wait states can be reduced by reducing the CPU frequency.
2. If PDR_ON is set to V_{SS}, this value can be lowered to 1.7 V when the device operates in a reduced temperature range (0 to 70 °C).
3. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
4. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 10* and *Table 12*.

Figure 20. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 12. VCAP1/VCAP2 operating conditions

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	Must be 2.2 µF
ESR	ESR of external capacitor	Must be lower than 2 Ω

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 13. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 14. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 15. Embedded reset and power control block characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(3)	PVD hysteresis		-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	TBD(2)	1.70	TBD	V
		Rising edge	TBD	1.74	TBD	V
$V_{PDRhyst}$(3)	PDR hysteresis		-	40	-	mV

Table 15. Embedded reset and power control block characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}$(3)	BOR hysteresis		-	100	-	mV
$T_{RSTTEMPO}$(3)(4)	Reset temporization		0.5	1.5	3.0	ms
I_{RUSH}(3)	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
E_{RUSH}(3)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. TBD stands for “to be defined”.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.
4. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 19: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using a CoreMark-compliant code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz, 3 wait states

from 90 to 120 MHz, 4 wait states from 120 to 150 MHz, and 5 wait states from 150 to 168 MHz,).

- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 16. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)(1)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(2)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(3), all peripherals enabled(4)	168 MHz	93.1	TBD	TBD	mA
			144 MHz	76.2	TBD	TBD	
			120 MHz	66.5	TBD	TBD	
			90 MHz	53	TBD	TBD	
			60 MHz	36.7	TBD	TBD	
			30 MHz	20.1	TBD	TBD	
			25 MHz	15.5	TBD	TBD	
			16 MHz(5)	11	TBD	TBD	
			8 MHz	6.4	TBD	TBD	
			4 MHz	4	TBD	TBD	
			2 MHz	2.8	TBD	TBD	
		External clock(4), all peripherals disabled	168 MHz	46.4	TBD	TBD	
			144 MHz	40.3	TBD	TBD	
			120 MHz	36.6	TBD	TBD	
			90 MHz	30	TBD	TBD	
			60 MHz	21.5	TBD	TBD	
			30 MHz	12.2	TBD	TBD	
			25 MHz	9.7	TBD	TBD	
			16 MHz(5)	7.1	TBD	TBD	
			8 MHz	4.4	TBD	TBD	
			4 MHz	3	TBD	TBD	
			2 MHz	2.3	TBD	TBD	

1. TBD stands for “to be defined”.
2. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
3. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
4. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. In this case HCLK = system clock/2.

Table 17. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM (1)(2)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(3)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(4), all peripherals enabled(5)	168 MHz	86.8	TBD	TBD	mA
			144 MHz	67	TBD	TBD	
			120 MHz	56.2	TBD	TBD	
			90 MHz	43.5	TBD	TBD	
			60 MHz	29.7	TBD	TBD	
			30 MHz	16.3	TBD	TBD	
			25 MHz	12.4	TBD	TBD	
			16 MHz(6)	8.7	TBD	TBD	
			8 MHz	5.1	TBD	TBD	
			4 MHz	3.3	TBD	TBD	
			2 MHz	2.4	TBD	TBD	
		External clock(4), all peripherals disabled	168 MHz	39.8	TBD	TBD	
			144 MHz	30.8	TBD	TBD	
			120 MHz	26	TBD	TBD	
			90 MHz	20.4	TBD	TBD	
			60 MHz	14.3	TBD	TBD	
			30 MHz	8.2	TBD	TBD	
			25 MHz	6.4	TBD	TBD	
			16 MHz(6)	4.75	TBD	TBD	
			8 MHz	3	TBD	TBD	
			4 MHz	2.3	TBD	TBD	
			2 MHz	2	TBD	TBD	

1. Code and data processing running from SRAM1 using boot pins.
2. TBD stands for “to be defined”.
3. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
4. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
5. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
6. In this case HCLK = system clock/2.

Table 18. Typical and maximum current consumption in Sleep mode(1)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(2)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(3), all peripherals enabled(4)	168 MHz	TBD	TBD	TBD	mA
			144 MHz	TBD	TBD	TBD	
			120 MHz	38	TBD	TBD	
			90 MHz	30	TBD	TBD	
			60 MHz	20	TBD	TBD	
			30 MHz	11	TBD	TBD	
			25 MHz	8	TBD	TBD	
			16 MHz	6	TBD	TBD	
			8 MHz	3.6	TBD	TBD	
			4 MHz	2.4	TBD	TBD	
			2 MHz	1.9	TBD	TBD	
		External clock(3), all peripherals disabled	168 MHz	TBD	TBD	TBD	
			144 MHz	TBD	TBD	TBD	
			120 MHz	8	TBD	TBD	
			90 MHz	7	TBD	TBD	
			60 MHz	5	TBD	TBD	
			30 MHz	3.5	TBD	TBD	
			25 MHz	2.5	TBD	TBD	
			16 MHz	2.1	TBD	TBD	
			8 MHz	1.7	TBD	TBD	
			4 MHz	1.5	TBD	TBD	
			2 MHz	1.4	TBD	TBD	

1. TBD stands for “to be defined”.
2. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
3. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
4. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

Table 19. Typical and maximum current consumptions in Stop mode(1)(2)

Symbol	Parameter	Conditions	Typ	Max		Unit
			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	1.00	TBD	TBD	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.98	TBD	TBD	
	Supply current in Stop mode with main regulator in Low Power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.66	TBD	TBD	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.63	TBD	TBD	

1. All typical and maximum values will be further reduced by up to 50% as part of ST continuous improvement of test procedures. New versions of the datasheet will be released to reflect these changes.
2. TBD stands for “to be defined”.

Table 20. Typical and maximum current consumptions in Standby mode(1)

Symbol	Parameter	Conditions	Typ			Max		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, RTC ON	TBD	TBD	TBD	TBD(2)	TBDS(2)	µA
		Backup SRAM OFF, RTC ON	TBD	TBD	TBD	TBDS(2)	TBDS(2)	
		Backup SRAM ON, RTC OFF	TBD	TBD	TBD	TBDS(2)	TBDS(2)	
		Backup SRAM OFF, RTC OFF	TBD	TBD	TBD	TBDS(2)	TBDS(2)	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production.

Table 21. Typical and maximum current consumptions in V_{BAT} mode(1)

Symbol	Parameter	Conditions	Typ			Max		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, RTC ON	TBD	TBD	TBD	TBD(2)	TBD(2)	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	TBD	TBD	TBD	TBD(2)	TBD(2)	
		Backup SRAM ON, RTC OFF	TBD	TBD	TBD	TBD(2)	TBD(2)	
		Backup SRAM OFF, RTC OFF	TBD	TBD	TBD	TBD(2)	TBD(2)	

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 43: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog pins.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 23: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the /O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 22. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	Supply current	V_{DD} = 3.3 V C_{ext} = 20 pF	TBD	TBD	mA
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
		V_{DD} = 3.3 V C_{ext} = 50 pF	TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
		V_{DD} = 2.4V C_{ext} = 20pF	TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
		V_{DD} = 2.4V C_{ext} = 50pF	TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	

1. TBD stands for “to be defined”.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 23*. The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog pins by firmware.
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- The code is running from Flash memory and the Flash memory access time is equal to 3 wait states at 120 MHz, 4 wait states at 144 MHz, and 5 wait states at 168 MHz.
- Prefetch and Cache ON
- When the peripherals are enabled, HCLK = 120/144/168 MHz, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$
- The typical values are obtained for V_{DD} = 3.3 V and T_A= 25 °C, unless otherwise specified.

Table 23. Peripheral current consumption(1)

Peripheral(2)		Typical consumption at 25 °C	Unit
AHB1	GPIO A	TBD	mA
	GPIO B	TBD	
	GPIO C	TBD	
	GPIO D	TBD	
	GPIO E	TBD	
	GPIO F	TBD	
	GPIO G	TBD	
	GPIO H	TBD	
	GPIO I	TBD	
	OTG_HS + ULPI	TBD	
	CRC	TBD	
	BKPSRAM	TBD	
	DMA1	TBD	
	DMA2	TBD	
	ETH_MAC + ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	TBD	
AHB2	OTG_FS	TBD	
	DCMI	TBD	
AHB3	FSMC	TBD	

Table 23. Peripheral current consumption(1) (continued)

Peripheral(2)		Typical consumption at 25 °C	Unit
APB1	TIM2	TBD	mA
	TIM3	TBD	
	TIM4	TBD	
	TIM5	TBD	
	TIM6	TBD	
	TIM7	TBD	
	TIM12	TBD	
	TIM13	TBD	
	TIM14	TBD	
	USART2	TBD	
	USART3	TBD	
	UART4	TBD	
	UART5	TBD	
	I2C1	TBD	
	I2C2	TBD	
	I2C3	TBD	
	SPI2	TBD	
	SPI3	TBD	
	CAN1	TBD	
	CAN2	TBD	
	DAC channel 1(3)	TBD	
	DAC channel 1(4)	TBD	
	PWR	TBD	
	WWDG	TBD	

Table 23. Peripheral current consumption(1) (continued)

Peripheral(2)		Typical consumption at 25 °C	Unit
APB2	SDIO	TBD	mA
	TIM1	TBD	
	TIM8	TBD	
	TIM9	TBD	
	TIM10	TBD	
	TIM11	TBD	
	ADC1(5)	TBD	
	ADC2(5)	TBD	
	ADC3(5)	TBD	
	SPI1	TBD	
	USART1	TBD	
	USART6	TBD	

1. TBD stands for “to be defined”.
2. External clock is 25 MHz (HSE oscillator with 25 MHz crystal) and PLL is on.
3. EN1 bit is set in DAC_CR register.
4. EN2 bit is set in DAC_CR register.
5. $f_{ADC} = f_{PCLK2}/2$, ADON bit set in ADC_CR2 register.

5.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 24* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 24. Low-power mode wakeup timings

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	1	-	µs
t_{WUSTOP}(2)	Wakeup from Stop mode (regulator in Run mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low power mode)	-	17	40	
	Wakeup from Stop mode (regulator in low power mode and Flash memory in Deep power down mode)	-	110	-	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	260	375	480	µs

1. Based on characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 25* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 25. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	8	26	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 26* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 26. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	TBD(2)	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.
2. TBD stands for “to be defined”.

Figure 21. High-speed external clock source AC timing diagram

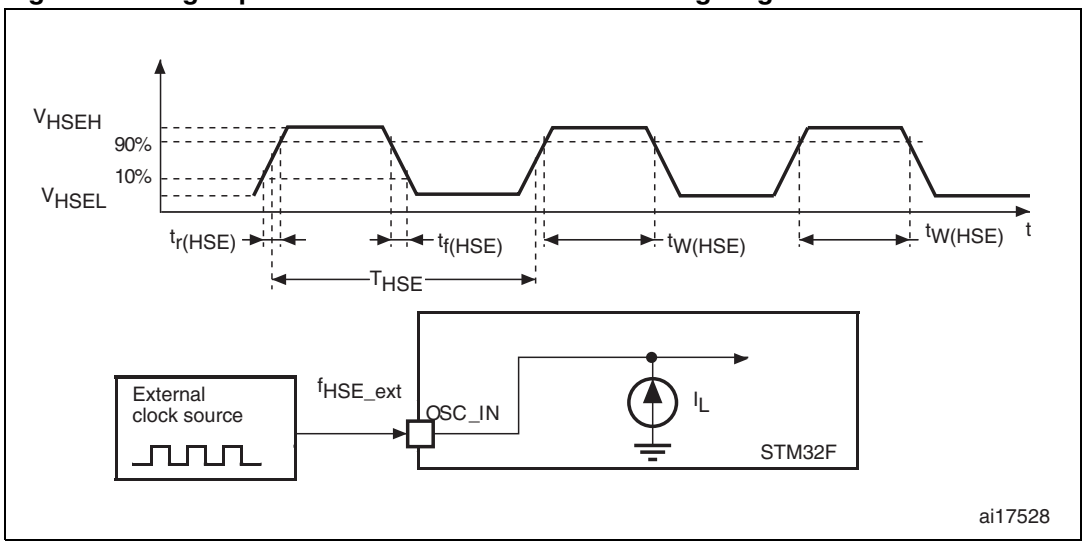
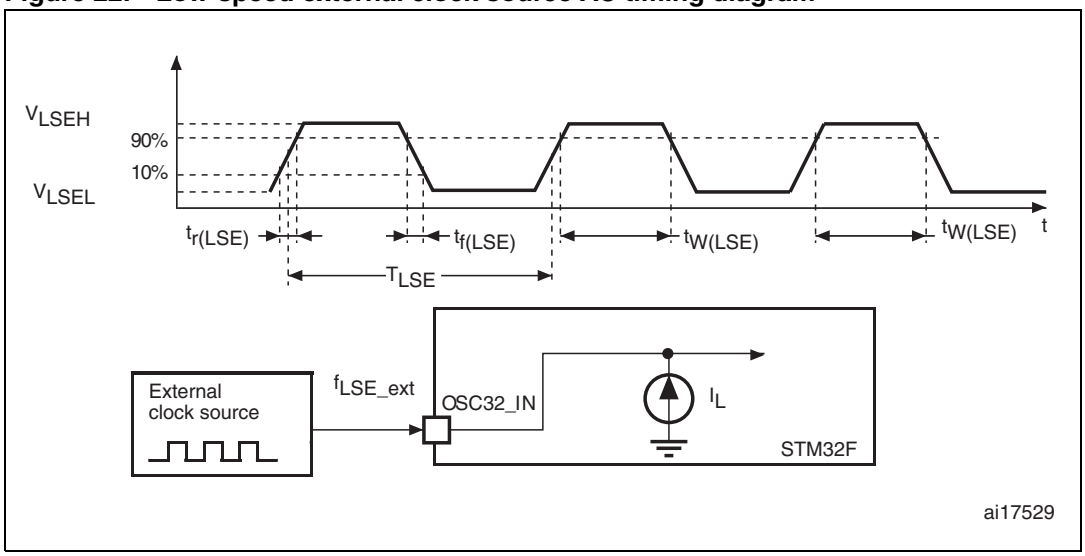


Figure 22. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 27*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

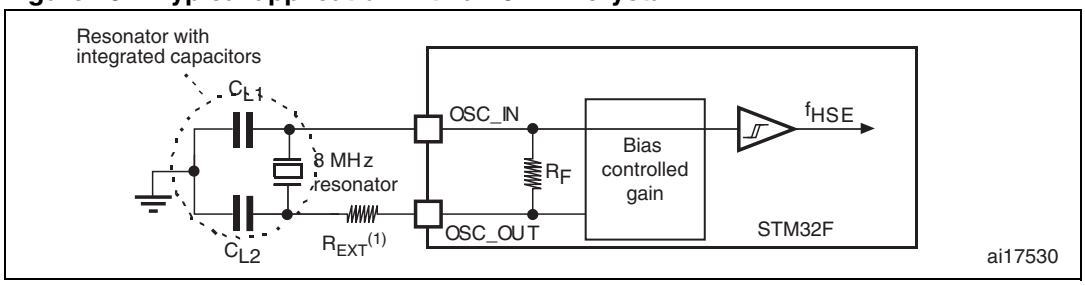
Table 27. HSE 4-26 MHz oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	15	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	5	-	-	mA/V
$t_{SU(HSE}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 23*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 23. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 28*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 28. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)(2)

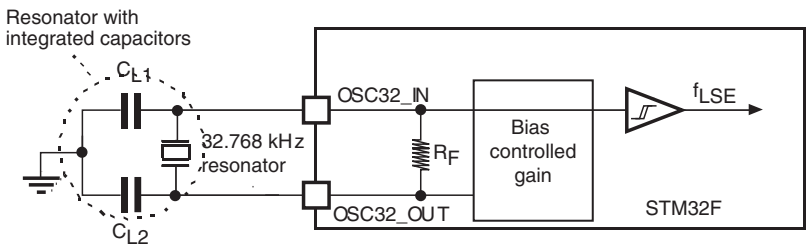
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor		-	TBD	-	MΩ
$C^{(3)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 kΩ	-	-	TBD	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	TBD	µA
g_m	Oscillator Transconductance		TBD	-	-	µA/V
$t_{SU(LSE)}^{(5)}$	startup time	V_{DD} is stabilized	-	TBD	-	s

1. Based on characterization, not tested in production.
2. TBD stands for “to be defined”.
3. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
4. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
5. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For C_{L1} and C_{L2} it is recommended to use high-quality external ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 24). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

Figure 24. Typical application with a 32.768 kHz crystal



5.3.9 Internal clock source characteristics

The parameters given in *Table 29* and *Table 30* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

High-speed internal (HSI) RC oscillator

Low-speed internal (LSI) RC oscillator

Table 29. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency			-	16	-	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1	%
		Factory-calibrated	T_A = –40 to 105 °C	–8	-	4.5	%
			T_A = –10 to 85 °C	–4	-	4	%
			T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time			-	2.2	4	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			-	60	80	µA

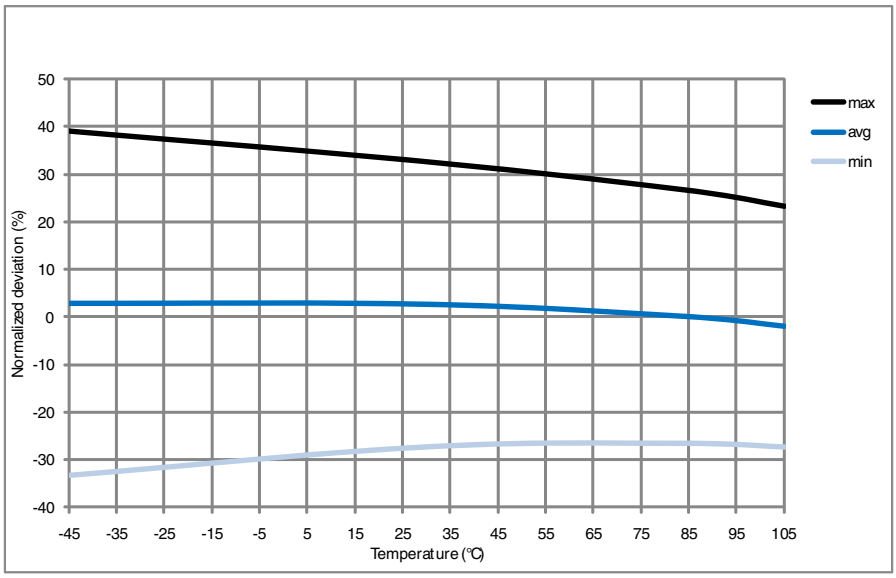
1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.

Table 30. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Figure 25. ACC_{LSI} versus temperature



MS19013V1

5.3.10 PLL characteristics

The parameters given in *Table 31* and *Table 32* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 31. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)		0.95(2)	1	2.0(3)	MHz
f_{PLL_OUT}	PLL multiplier output clock		24	-	168	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock		-	48	-	MHz
f_{VCO_OUT}	PLL VCO output		192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 31. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(4)	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
	Main clock output (MCO) for RMMI Ethernet	Long term Jitter, PLL input=6.25MHz		-	1.6	-	ns
$I_{DD(PLL)}$(5)	PLL power consumption on VDD	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(5)	PLL power consumption on VDDA	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. Maximum input PLL frequency is recommended for applications sensitive of long term jitter.
4. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
5. Based on characterization, not tested in production.

Table 32. PLLI2S (audio PLL) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(2)		0.95(3)	1	2.0(4)	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock		-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output		192	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 32. PLLI2S (audio PLL) characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(5)	Master I2S clock jitter	Cycle to cycle at 12,343 MHz on 48KHz period, N=432, P=4, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12,343 MHz N=432, P=4, R=5 on 256 samples		TBD	-	TBD	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(6)	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(6)	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. TBD stands for “to be defined”.
2. Take care of using the appropriate division factor M to have the specified PLL input clock values.
3. Guaranteed by design, not tested in production.
4. Maximum input PLL frequency is recommended for applications sensitive of long term jitter.
5. Value given with main PLL running.
6. Based on characterization, not tested in production.

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 39: EMI characteristics*). It is available only on the main PLL.

Table 33. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN}/(4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6/(4 \times 10^3)] = 25$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15}-1) \times md \times f_{VCO\_OUT})/(100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and f_{VCO_OUT} = 240 (in MHz):

$$INCSTEP = round[((2^{15}-1) \times 2 \times 240)/(100 \times 5 \times 25)] = 1258 md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5)/((2^{15}-1) \times f_{VCO\_OUT})$$

As a result:

$$md_{quantized}\% = (25 \times 1258 \times 100 \times 5)/((2^{15}-1) \times 240) = 1.99954\%(peak)$$

The error in modulation depth is consequently: 2.0 - 1.99954 = 0.00046%.

Figure 26 and *Figure 27* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 26. PLL output clock waveforms in center spread mode

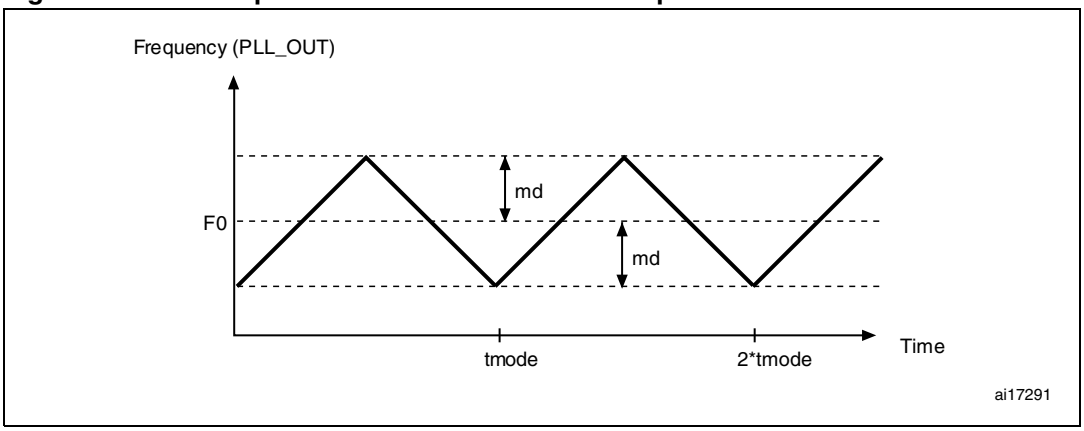
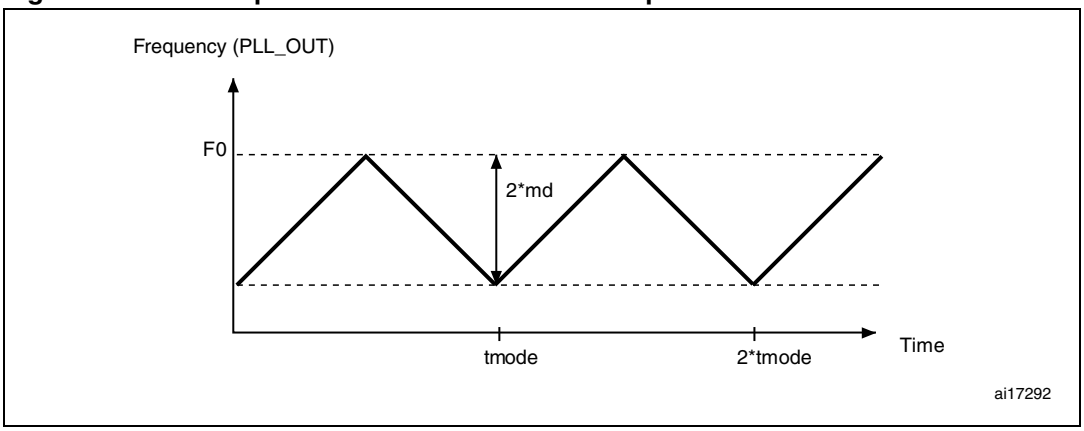


Figure 27. PLL output clock waveforms in down spread mode



5.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 34. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
I_{DD}	Supply current	Read mode f_{HCLK} = 168 MHz with 4 wait states, V_{DD} = 3.3 V	-	TBD	mA
		Write / Erase modes f_{HCLK} = 168 MHz, V_{DD} = 3.3 V	-	TBD	mA

1. TBD stands for “to be defined”.

Table 35. Flash memory programming(1)

Symbol	Parameter	Conditions	Min(2)	Typ	Max(2)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(3)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	TBD	s
		Program/erase parallelism (PSIZE) = x 16	-	11	TBD	
		Program/erase parallelism (PSIZE) = x 32	-	8	TBD	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. TBD stands for “to be defined”.
2. Based on characterization, not tested in production.
3. The maximum programming time is measured after 100K erase operations.

Table 36. Flash memory programming with V_{PP}(1)

Symbol	Parameter	Conditions	Min(2)	Typ	Max(2)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C	-	16	100(3)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	TBD	-	
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	TBD	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	TBD	-	
t_{ME}	Mass erase time		-	6.8	-	
V_{prog}	Programming voltage		2.7	-	3.6	V
V_{PP}	V_{PP} voltage range		7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin		10	-	-	mA
t_{VPP}(4)	Cumulative time during which V_{PP} is applied		-	-	1	hour

1. TBD stands for “to be defined”.
2. Guaranteed by design, not tested in production.
3. The maximum programming time is measured after 100K erase operations.
4. V_{PP} should only be connected during programming/erasing.

Table 37. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 84 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 84 MHz, conforms to IEC 61000-4-2	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC® code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics(1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/120 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled	0.1 to 30 MHz	TBD	dBµV
			30 to 130 MHz	TBD	
			130 MHz to 1GHz	TBD	
			SAE EMI Level	TBD	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running with ART enabled, PLL spread spectrum enabled	0.1 to 30 MHz	TBD	dBµV
			30 to 130 MHz	TBD	
			130 MHz to 1GHz	TBD	
			SAE EMI level	TBD	-

1. TBD stands for “to be defined”.

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 42*.

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all FT pins	–5	+0	mA
	Injected current on any other pin	–5	+5	

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage		TTL ports 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{SS}–0.3	-	0.8	V
V_{IH}(1)	TT(2) I/O input high level voltage			2.0	-	V_{DD}+0.3	
	FT(3) I/O input high level voltage			2.0	-	5.5	
V_{IL}	Input low level voltage		CMOS ports 1.8 V ≤ V_{DD} ≤ 3.6 V	V_{SS}–0.3	-	0.3V_{DD}	
V_{IH}(1)	TT I/O input high level voltage			0.7V_{DD}	-	3.6(4)	
	FT I/O input high level voltage				-	5.2(4)	
			CMOS ports 2.0 V ≤ V_{DD} ≤ 3.6 V		-	5.5(4)	
V_{hys}	I/O Schmitt trigger voltage hysteresis(5)			-	200	-	mV
	IO FT Schmitt trigger voltage hysteresis(5)			5% V_{DD}(4)	-	-	
I_{lkg}	I/O input leakage current (6)		V_{SS} ≤ V_{IN} ≤ V_{DD}	-	-	±1	µA
	I/O FT input leakage current (6)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	All pins except for PA10 and PB12	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 and PB12		8	11	15	
R_{PD}	Weak pull-down equivalent resistor	All pins except for PA10 and PB12	V_{IN} = V_{DD}	30	40	50	
		PA10 and PB12		8	11	15	
C_{IO}(8)	I/O pin capacitance				5		pF

1. If V_{IH} maximum value cannot be respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum value.
2. TT = 3.6 V tolerant.
3. FT = 5 V tolerant.
4. With a minimum of 100 mV.
5. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
6. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).
8. Guaranteed by design, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 8*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 8*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 28* and *Table 45*, respectively.

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 45. I/O AC characteristics(1)(2)

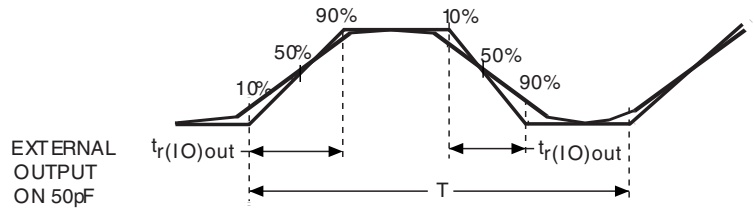
OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	2	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	TBD	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	TBD	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	TBD	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	-	TBD	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5(4)	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	TBD	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} < 2.7 V	-	-	TBD	ns
			C_L = 10 pF, V_{DD} > 2.7 V	-	-	TBD	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} < 2.7 V	-	-	TBD	
			C_L = 10 pF, V_{DD} > 2.7 V	-	-	TBD	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	25	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	TBD	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, 2.4 < V_{DD} < 2.7 V	-	-	TBD	ns
			C_L = 10 pF, V_{DD} > 2.7 V	-	-	TBD	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, 2.4 < V_{DD} < 2.7 V	-	-	TBD	
			C_L = 10 pF, V_{DD} > 2.7 V	-	-	TBD	

Table 45. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50(4)	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	200(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	TBD	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 20 pF, 2.4 < V_{DD} < 2.7 V	-	-	TBD	ns
			C_L = 10 pF, V_{DD} > 2.7 V	-	-	TBD	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 20 pF, 2.4 < V_{DD} < 2.7 V	-	-	TBD	
			C_L = 10 pF, V_{DD} > 2.7 V	-	-	TBD	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	-	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F20/21xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
2. TBD stands for “to be defined”.
3. The maximum frequency is defined in *Figure 28*.
4. For maximum frequencies above 50 MHz, the compensation cell should be used.

Figure 28. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 43*).

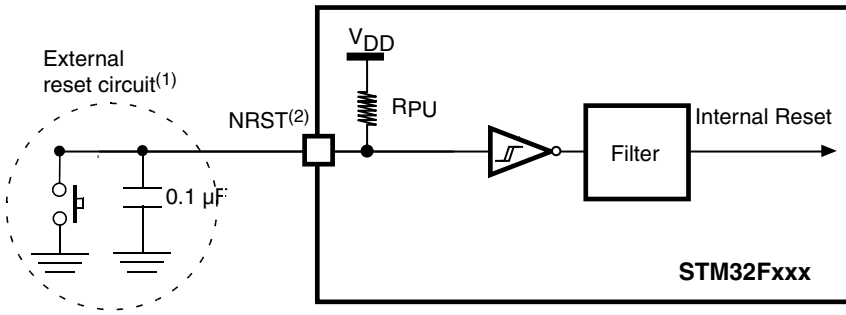
Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 46. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 29. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset is not taken into account by the device.

5.3.18 TIM timer characteristics

The parameters given in *Table 47* and *Table 48* are guaranteed by design.

Refer to *Section 5.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. Characteristics of TIMx connected to the APB1 domain(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK}$ = 42 MHz	1	-	$t_{TIMxCLK}$
			23.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 84 MHz APB1= 42 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	42	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0119	TBD	µs
	32-bit counter clock period when internal clock is selected		1	-	$t_{TIMxCLK}$
			0.0119	TBD	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	TBD	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.
2. TBD stands for “to be defined”.

Table 48. Characteristics of TIMx connected to the APB2 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB2 prescaler distinct from 1, $f_{TIMxCLK}$ = 168 MHz	1	-	$t_{TIMxCLK}$
			5.95	-	ns
		AHB/APB2 prescaler = 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 168 MHz APB2 = 84 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	84	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.00595	TBD	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	TBD(2)	s

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.
2. TBD stands for “to be defined”.

5.3.19 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

The STM32F405xx and STM32F407xx I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

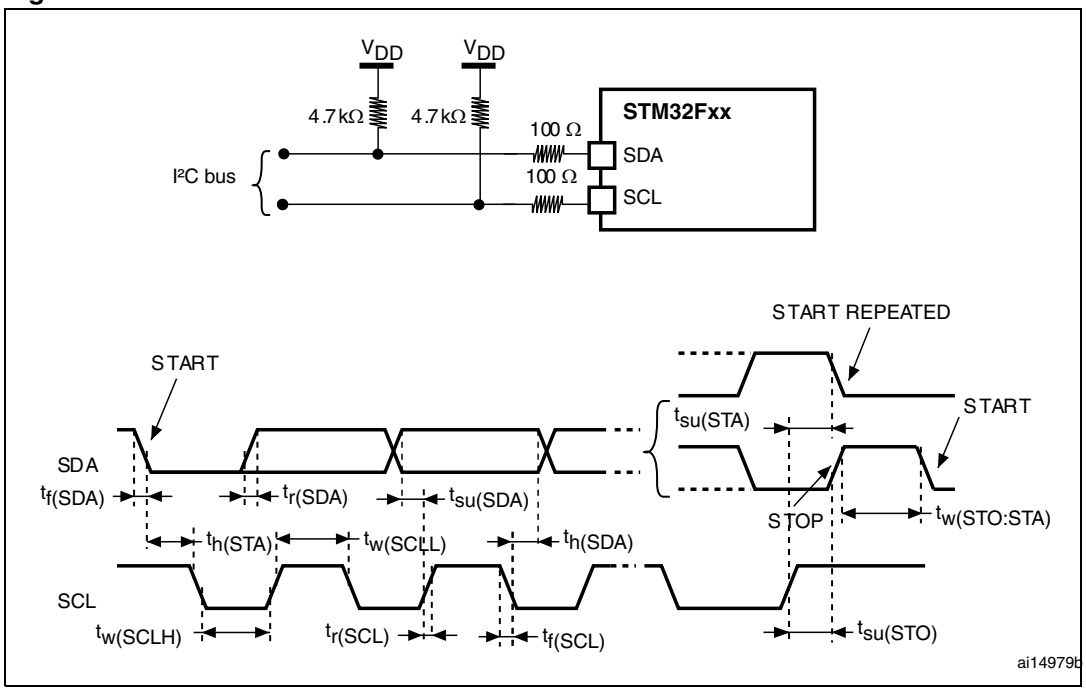
The I²C characteristics are described in *Table 49*. Refer also to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 49. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I^2C fast mode clock.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 30. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 50. SCL frequency (f_{PCLK1}= 42 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I^2S - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 51* for SPI or in *Table 52* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 51. SPI characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	37.5	MHz
		Slave mode	-	37.5	
$t_{r(SCL)}$ $t_{f(SCL)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(3)	NSS setup time	Slave mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$(3)	NSS hold time	Slave mode	2 t_{PCLK}	-	
$t_{w(SCLH)}$(3) $t_{w(SCLL)}$(3)	SCK high and low time	Master mode, f_{PCLK} = 42 MHz, presc = 4	TBD	TBD	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode	5	-	
		Slave mode	4	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3 t_{PCLK}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$(3)(1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$(3)(1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)	2	-	

1. Remapped SPI1 characteristics to be determined.
2. TBD stands for “to be defined”.
3. Based on characterization, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 31. SPI timing diagram - slave mode and CPHA = 0

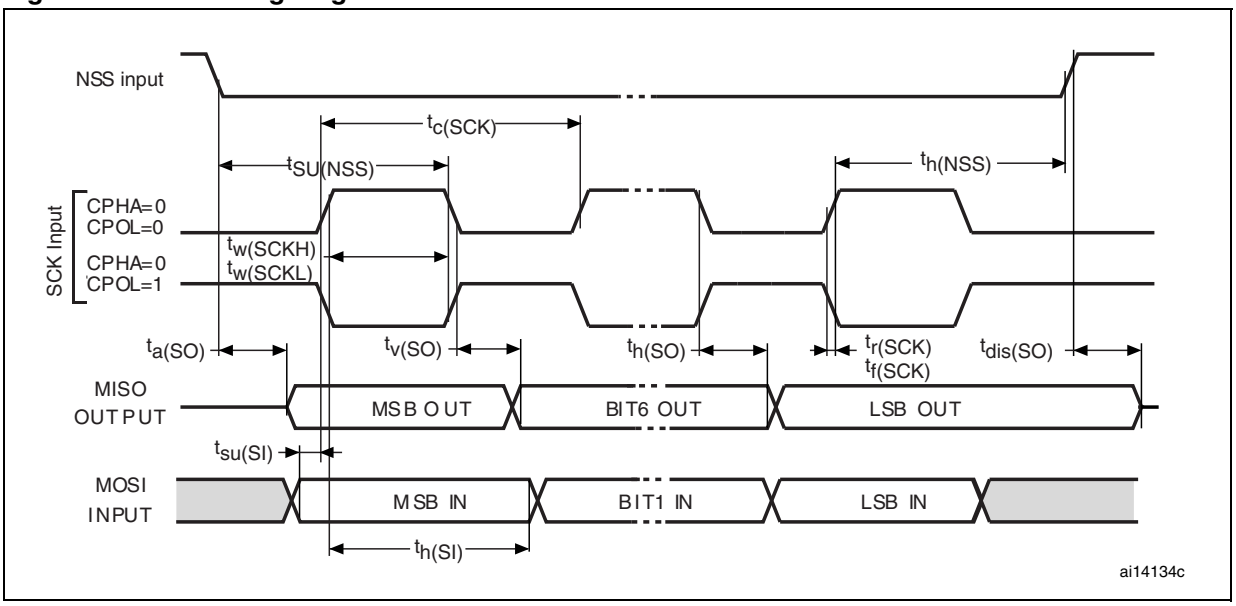
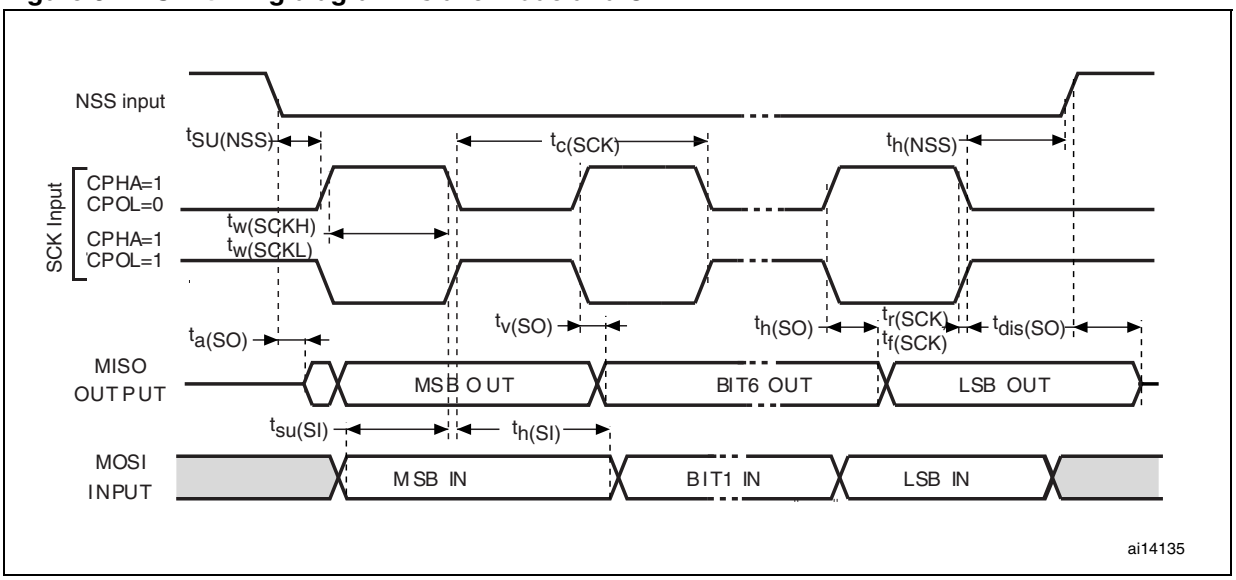
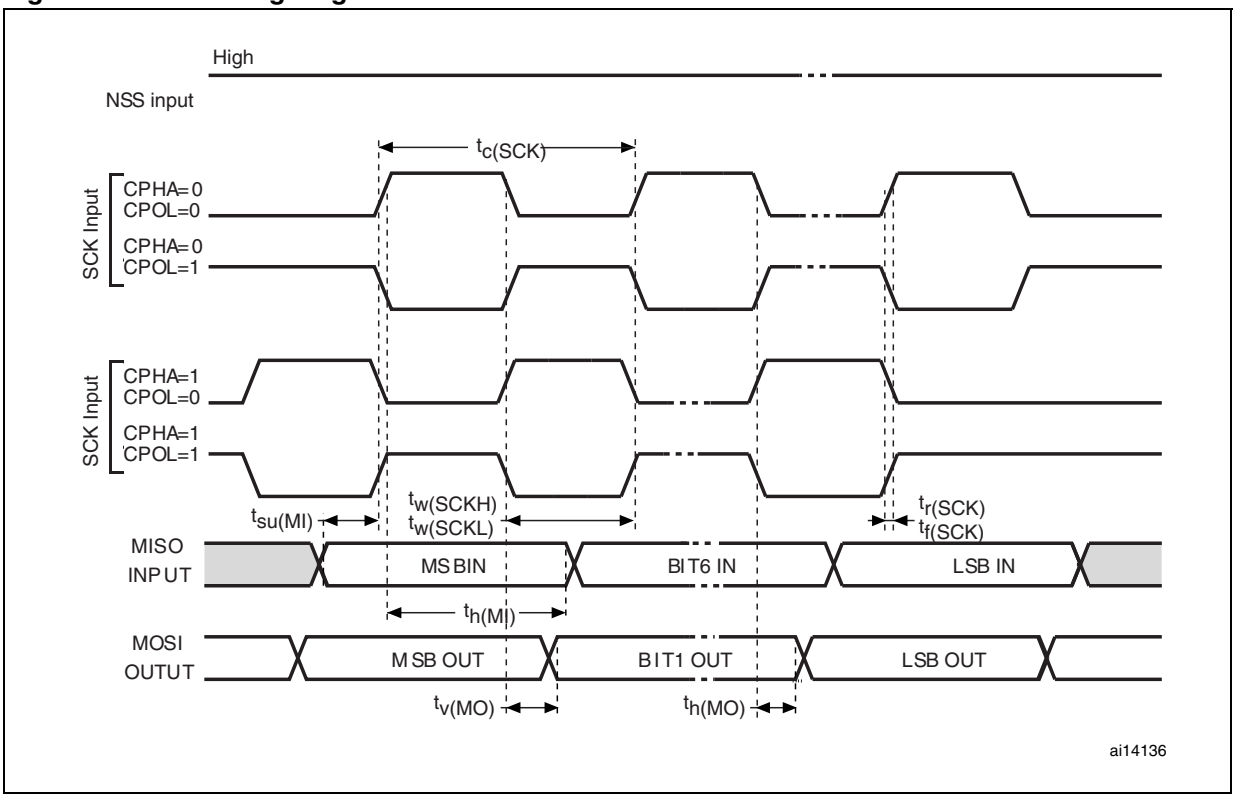


Figure 32. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 33. SPI timing diagram - master mode(1)



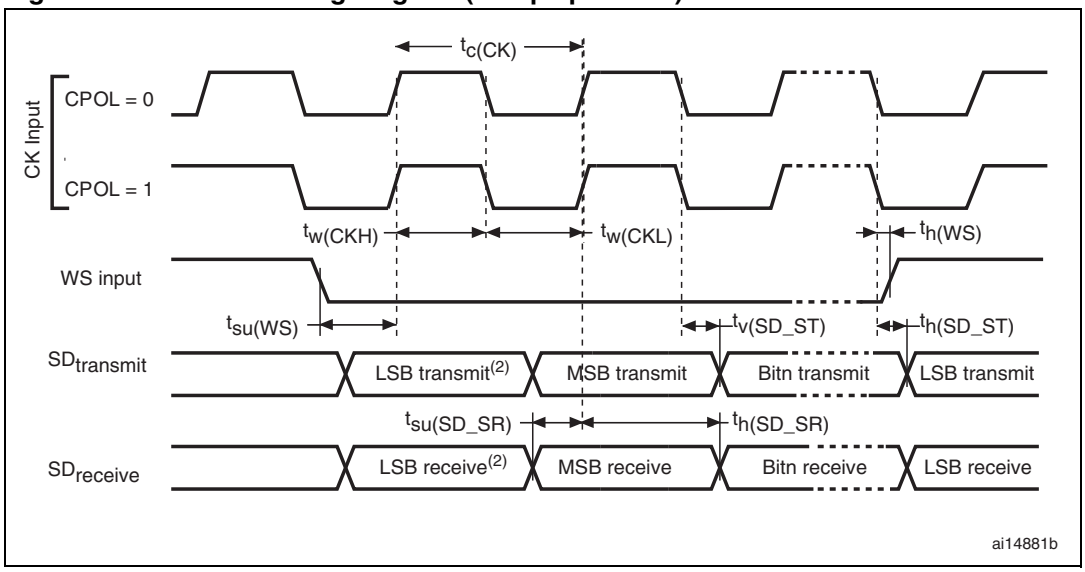
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 52. I^2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master	TBD	37.5	MHz
		Slave	0	37.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	capacitive load C_L = 50 pF	-	TBD	ns
$t_{v(WS)}$ (2)	WS valid time	Master	TBD	-	
$t_{h(WS)}$ (2)	WS hold time	Master	TBD	-	
$t_{su(WS)}$ (2)	WS setup time	Slave	TBD	-	
$t_{h(WS)}$ (2)	WS hold time	Slave	TBD	-	
$t_{w(CKH)}$ (2) $t_{w(CKL)}$ (2)	CK high and low time	Master f_{PCLK}= TBD, presc = TBD	TBD	-	
$t_{su(SD\_MR)}$ (2) $t_{su(SD\_SR)}$ (2)	Data input setup time	Master receiver Slave receiver	TBD TBD	-	
$t_{h(SD\_MR)}$ (2)(3) $t_{h(SD\_SR)}$ (2)(3)	Data input hold time	Master receiver Slave receiver	TBD TBD	-	
$t_{h(SD\_MR)}$ (2) $t_{h(SD\_SR)}$ (2)	Data input hold time	Master f_{PCLK} = TBD Slave f_{PCLK} = TBD	TBD TBD	-	
$t_{v(SD\_ST)}$ (2)(3)	Data output valid time	Slave transmitter (after enable edge)	-	TBD	
		f_{PCLK} = TBD	-	TBD	
$t_{h(SD\_ST)}$ (2)	Data output hold time	Slave transmitter (after enable edge)	TBD	-	
$t_{v(SD\_MT)}$ (2)(3)	Data output valid time	Master transmitter (after enable edge)	-	TBD	
		f_{PCLK} = TBD	TBD	TBD	
$t_{h(SD\_MT)}$ (2)	Data output hold time	Master transmitter (after enable edge)	TBD	-	

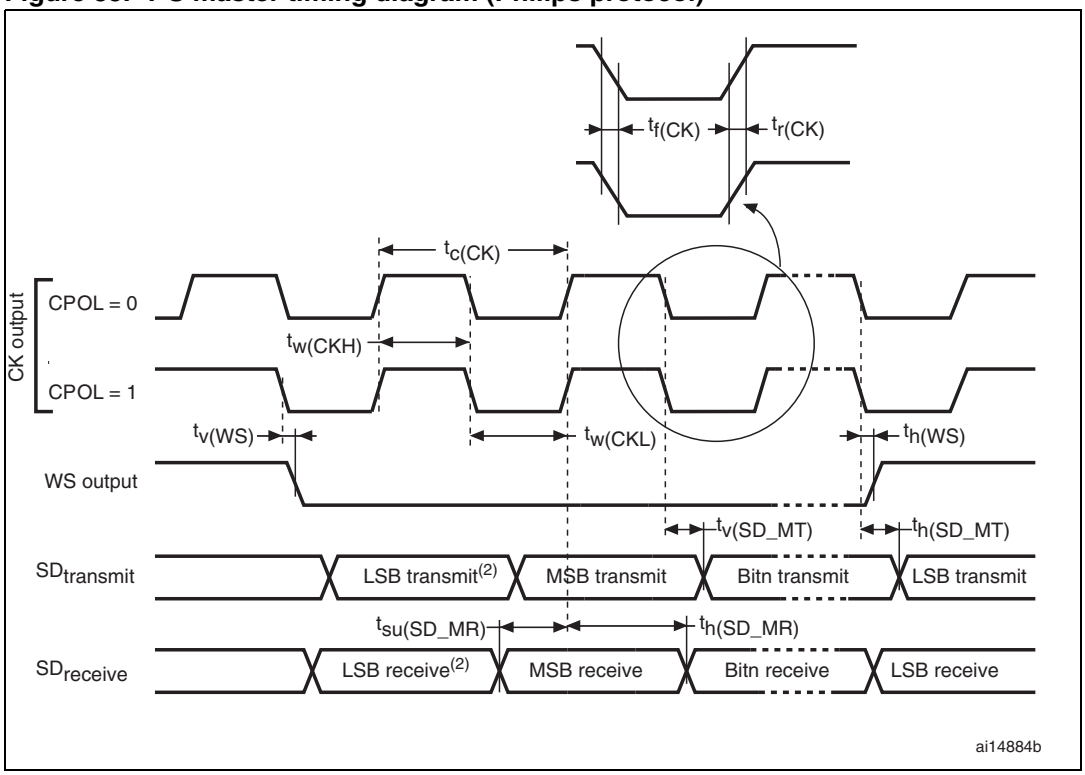
1. TBD stands for “to be defined”.
2. Based on design simulation and/or characterization results, not tested in production.
3. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.

Figure 34. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 35. I²S master timing diagram (Philips protocol)(1)



1. Based on characterization, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed). This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 53. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 54. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F405xx and STM32F407xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Figure 36. USB OTG FS timings: definition of data signal rise and fall time

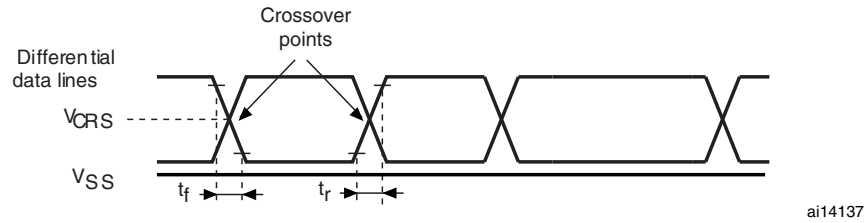


Table 55. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

Table 56. USB FS clock timing parameters(1)(2)

Parameter		Symbol	Min	Nominal	Max	Unit
f_{HCLK} value to guarantee proper operation of USB FS interface		-	TBD			MHz
AHB frequency for correct USB FS operation		-	14.2			MHz
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	TBD	TBD	TBD	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	TBD	TBD	TBD	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	TBD	TBD	TBD	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	TBD	TBD	TBD	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	TBD	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	TBD	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design, not tested in production.
2. TBD stands for “to be defined”.

USB HS characteristics

Table 57 shows the USB HS operating voltage.

Table 57. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 58. USB HS clock timing parameters(1)

Parameter		Symbol	Min	Nominal	Max	Unit
f_{HCLK} value to guarantee proper operation of USB HS interface			TBD			MHz
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design, not tested in production.

Figure 37. ULPI timing diagram

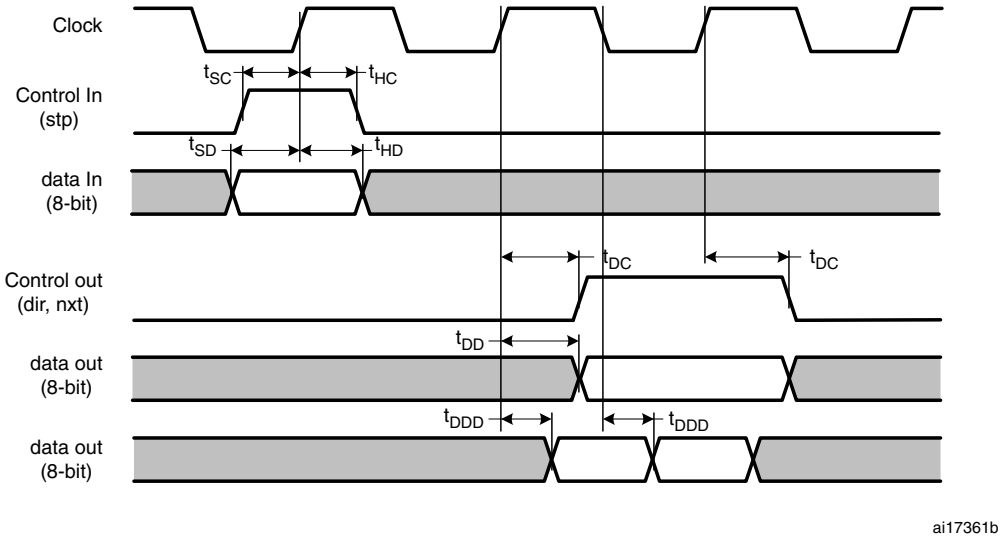


Table 59. ULPI timing

Parameter		Symbol	Value(1)		Unit
			Min.	Max.	
Output clock	Setup time (control in)	t_{SC}, t_{SD}	-	6.0	ns
	Hold time (control in)	t_{HC}, t_{HD}	0.0	-	ns
	Output delay (control out)	t_{DC}, t_{DD}	-	9.0	ns
Input clock (optional)	Setup time (control in)	t_{SC}, t_{SD}	-	3.0	ns
	Hold time (control in)	t_{HC}, t_{HD}	1.5	-	ns
	Output delay (control out)	t_{DC}, t_{DD}	-	6.0	ns

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Ethernet characteristics

Table 60 shows the Ethernet operating voltage.

Table 60. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 61 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 38* shows the corresponding timing diagram.

Figure 38. Ethernet SMI timing diagram

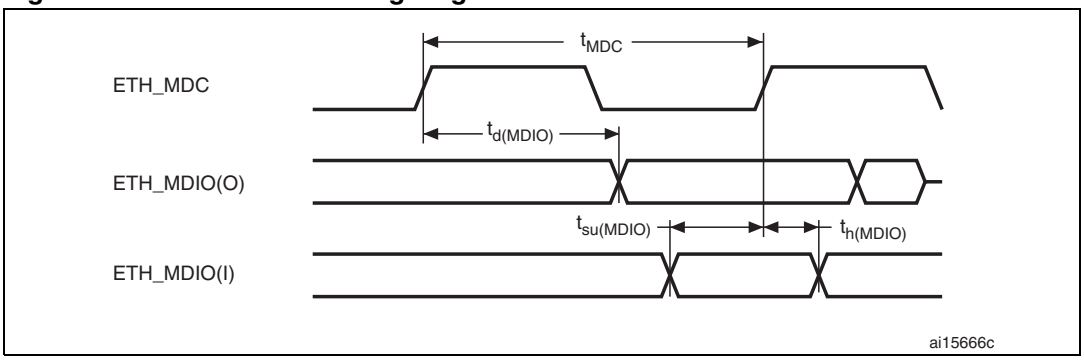


Table 61. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (1.71 MHz, AHB = 72 MHz)	TBD	TBD	TBD	ns
$t_{d(MDIO)}$	MDIO write data valid time	TBD	TBD	TBD	ns
$t_{su(MDIO)}$	Read data setup time	TBD	TBD	TBD	ns
$t_{h(MDIO)}$	Read data hold time	TBD	TBD	TBD	ns

1. TBD stands for “to be defined”.

Table 62 gives the list of Ethernet MAC signals for the RMII and *Figure 39* shows the corresponding timing diagram.

Figure 39. Ethernet RMII timing diagram

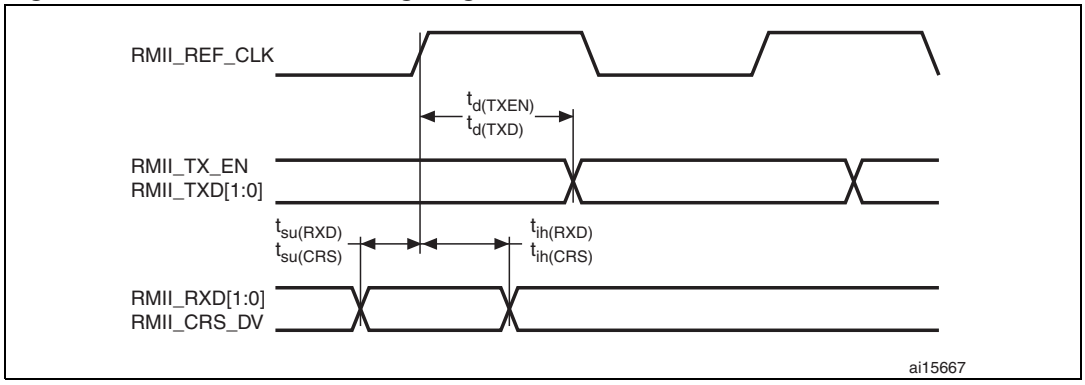


Table 62. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	TBD	TBD	TBD	ns
$t_{ih(RXD)}$	Receive data hold time	TBD	TBD	TBD	ns
$t_{su(CRS)}$	Carrier sense set-up time	TBD	TBD	TBD	ns
$t_{ih(CRS)}$	Carrier sense hold time	TBD	TBD	TBD	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	0	9.6	21.9	ns
$t_{d(TXD)}$	Transmit data valid delay time	0	9.9	21	ns

1. TBD stands for “to be defined”.

Table 63 gives the list of Ethernet MAC signals for MII and *Figure 39* shows the corresponding timing diagram.

Figure 40. Ethernet MII timing diagram

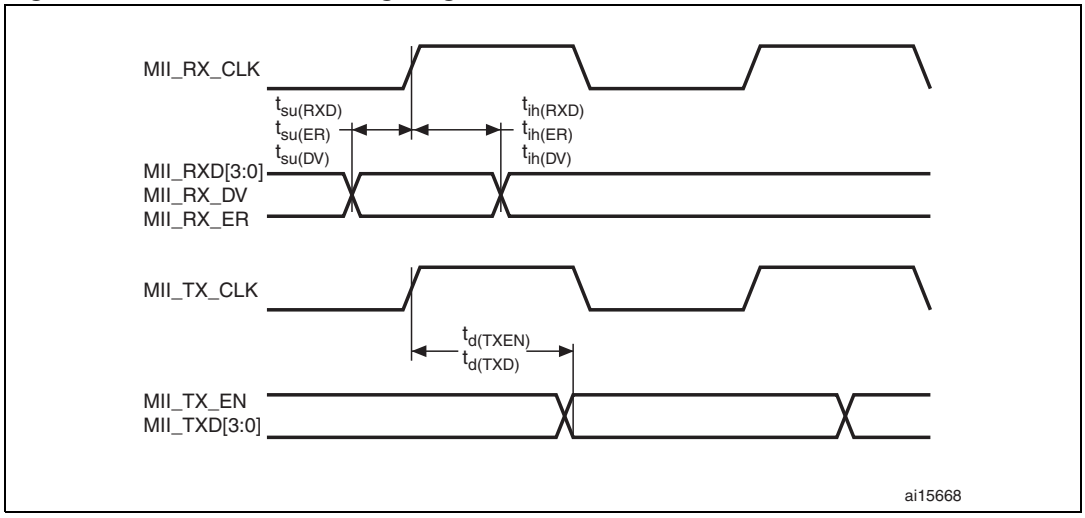


Table 63. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	TBD	TBD	TBD	ns
$t_{ih(RXD)}$	Receive data hold time	TBD	TBD	TBD	ns
$t_{su(DV)}$	Data valid setup time	TBD	TBD	TBD	ns
$t_{ih(DV)}$	Data valid hold time	TBD	TBD	TBD	ns
$t_{su(ER)}$	Error setup time	TBD	TBD	TBD	ns
$t_{ih(ER)}$	Error hold time	TBD	TBD	TBD	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	13.4	15.5	17.7	ns
$t_{d(TXD)}$	Transmit data valid delay time	12.9	16.1	19.4	ns

1. TBD stands for “to be defined”.

CAN (controller area network) interface

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 64* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Table 64. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		1.8(2)	-	3.6	V
V_{REF+}(3)	Positive reference voltage		1.8(2)(4)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(2) to 2.4 V	0.6	-	TBD	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	-	TBD	MHz
f_{TRIG}(5)	External trigger frequency	f_{ADC} = 36 MHz	-	-	TBD	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(6)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(5)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(5)(7)	Sampling switch resistance		1.5	-	6	kΩ
C_{ADC}(5)	Internal sample and hold capacitor		4	-	TBD	pF
t_{lat}(5)	Injection trigger conversion latency	f_{ADC} = 36 MHz	-	-	0.100	µs
			-	-	3(8)	$1/f_{ADC}$
t_{latr}(5)	Regular trigger conversion latency	f_{ADC} = 36 MHz	-	-	0.067	µs
			-	-	2(8)	$1/f_{ADC}$

Table 64. ADC characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S(5)	Sampling time	f_{ADC} = 36 MHz	0.100	-	16	µs
			3	-	416	$1/f_{ADC}$
t_{STAB}(5)	Power-up time		-	2	3	µs
t_{CONV}(5)	Total conversion time (including sampling time)	f_{ADC} = 36 MHz 12-bit resolution	0.416	-	12.95	µs
		f_{ADC} = 36 MHz 10-bit resolution	0.360	-	12.89	µs
		f_{ADC} = 36 MHz 8-bit resolution	0.305	-	12.84	µs
		f_{ADC} = 36 MHz 6-bit resolution	0.250	-	12.79	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(5)	Sampling rate (f_{ADC} = 36 MHz)	12-bit resolution Single ADC	-	-	2.4	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	4.8	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	Msps
I_{VREF+}(5)	ADC V_{REF} DC current consumption in conversion mode	f_{ADC} = 36 MHz 3 sampling time 12-bit resolution	-	300	500	µA
		f_{ADC} = 36 MHz 480 sampling time 12-bit resolution	-	-	TBD	µA
I_{DDA}(5)	ADC VDDA DC current consumption in conversion mode	f_{ADC} = 36 MHz 3 sampling time 12-bit resolution	-	1.6	1.8	mA
		f_{ADC} = 36 MHz 480 sampling time 12-bit resolution	-	-	TBD	

1. TBD stands for “to be defined”.
2. If PDR_ON is set to V_{SS}, this value can be lowered to 1.7 V when the device operates in a reduced temperature range (0 to 70 °C).
3. V_{DDA} -V_{REF+} < 1.2 V.
4. It is recommended to maintain the voltage difference between V_{REF+} and V_{DDA} below 1.8 V.
5. Based on characterization, not tested in production.
6. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
7. R_{ADC} maximum value is given for V_{DD}=1.8 V, and minimum value for V_{DD}=3.3 V.
8. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 64*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

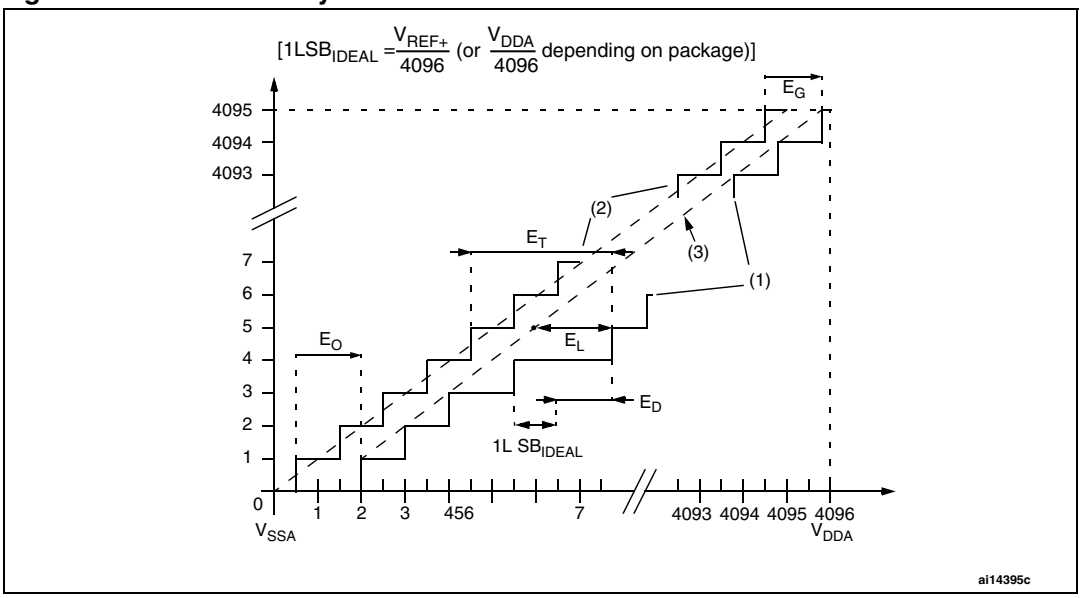
Table 65. ADC accuracy (1)(2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 84 MHz, f_{ADC} = 36 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.8(4) to 3.6 V	TBD	TBD	LSB
EO	Offset error		TBD	TBD	
EG	Gain error		TBD	TBD	
ED	Differential linearity error		TBD	TBD	
EL	Integral linearity error		TBD	TBD	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. TBD stands for “to be defined”.
3. Based on characterization, not tested in production.
4. If PDR_ON is set to V_{SS}, this value can be lowered to 1.7 V when the device operates in a reduced temperature range (0 to 70 °C).

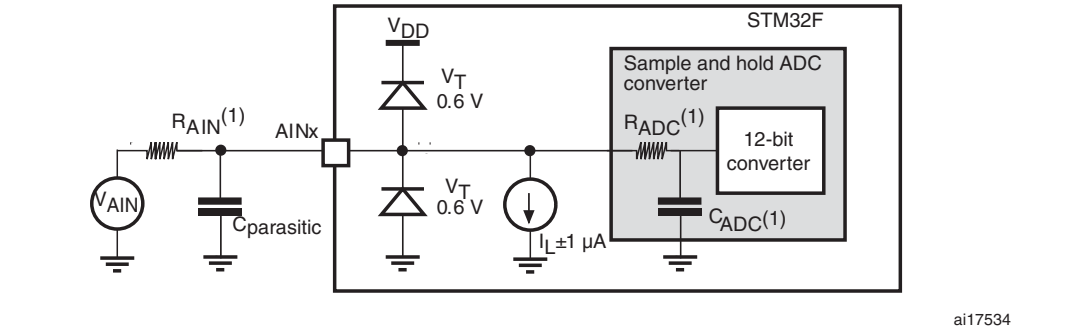
Note: ADC accuracy vs. negative injection current: Injecting a negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.16* does not affect the ADC accuracy.

Figure 41. ADC accuracy characteristics



1. See also *Table 65*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical connection diagram using the ADC

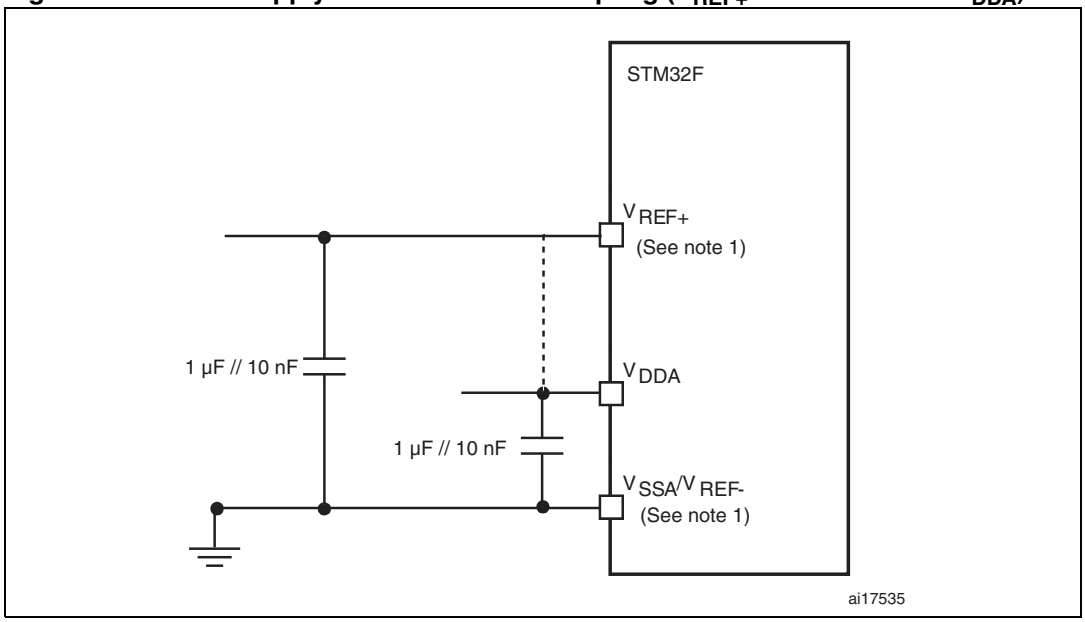


1. Refer to *Table 64* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

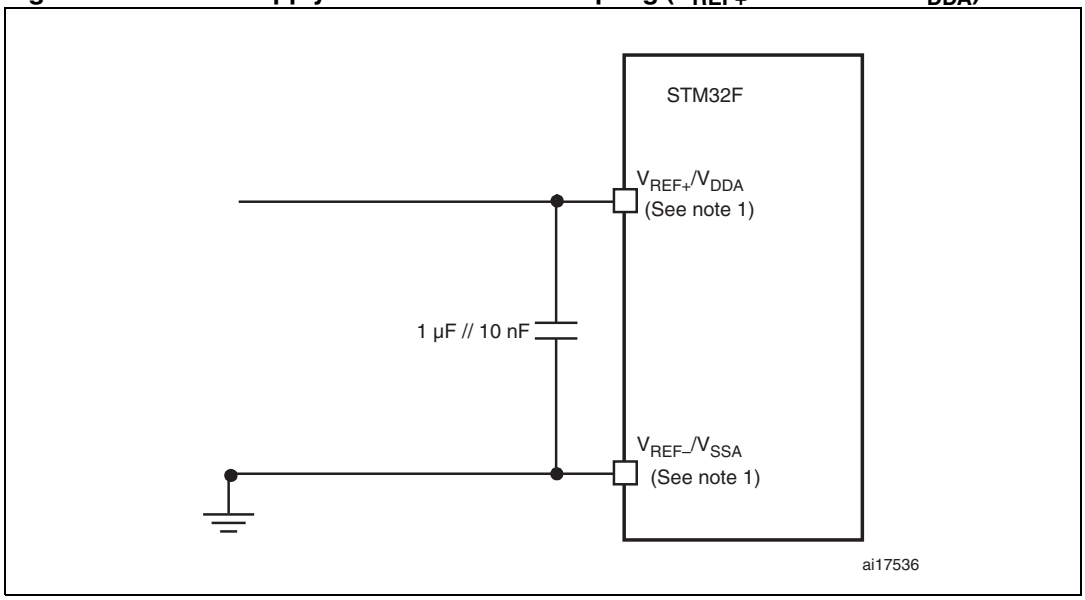
Power supply decoupling should be performed as shown in *Figure 43* or *Figure 44*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 43. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 44. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

5.3.21 Temperature sensor characteristics

Table 66. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5		mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76		V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

5.3.22 V_{BAT} monitoring characteristics

Table 67. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.23 Embedded reference voltage

The parameters given in *Table 68* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 68. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage		10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient		-	30	50	ppm/°C
t_{START}(2)	Startup time		-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.24 DAC electrical characteristics

Table 69. DAC characteristics

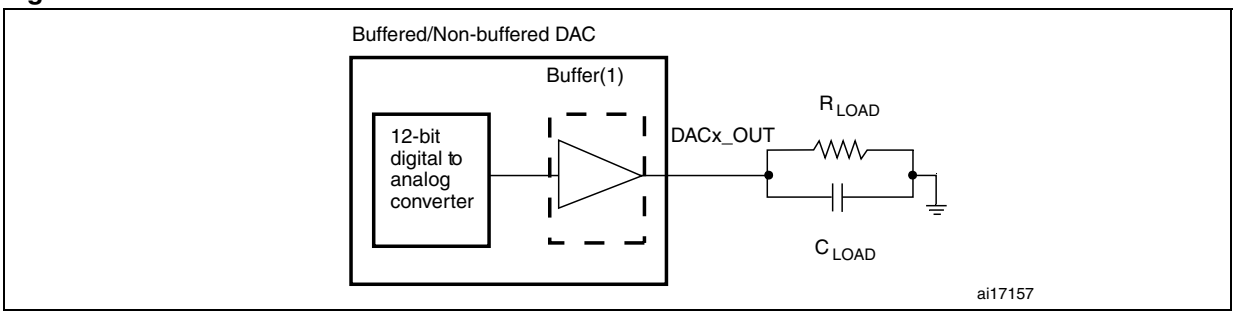
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8(1)	-	3.6	V	
V_{REF+}	Reference supply voltage	1.8(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(3)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}(3)	DAC DC VDDA current consumption in quiescent mode (Standby mode)	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.

Table 69. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(3)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	3	6	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
THD(3)	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. If PDR_ON is set to V_{SS}, this value can be lowered to 1.7 V when the device operates in a reduced temperature range (0 to 70 °C).
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization, not tested in production.

Figure 45. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

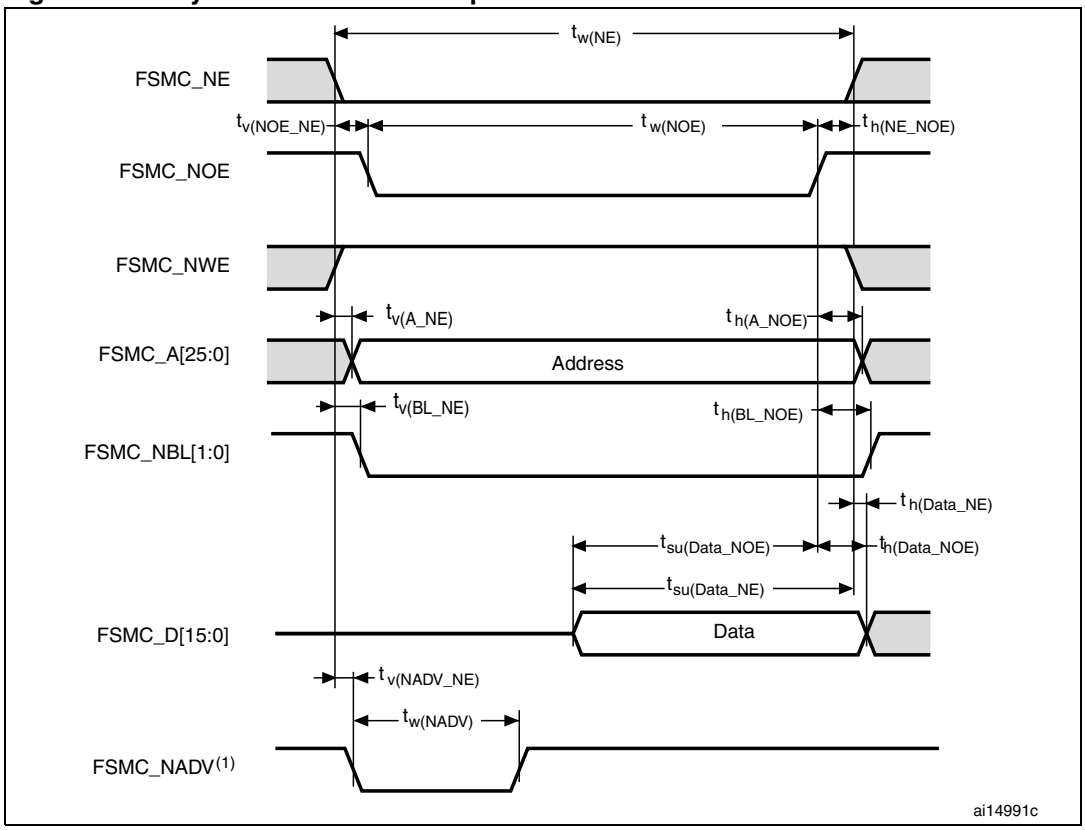
5.3.25 FSMC characteristics

Asynchronous waveforms and timings

Figure 46 through *Figure 49* represent asynchronous waveforms and *Table 70* through *Table 73* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 46. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)

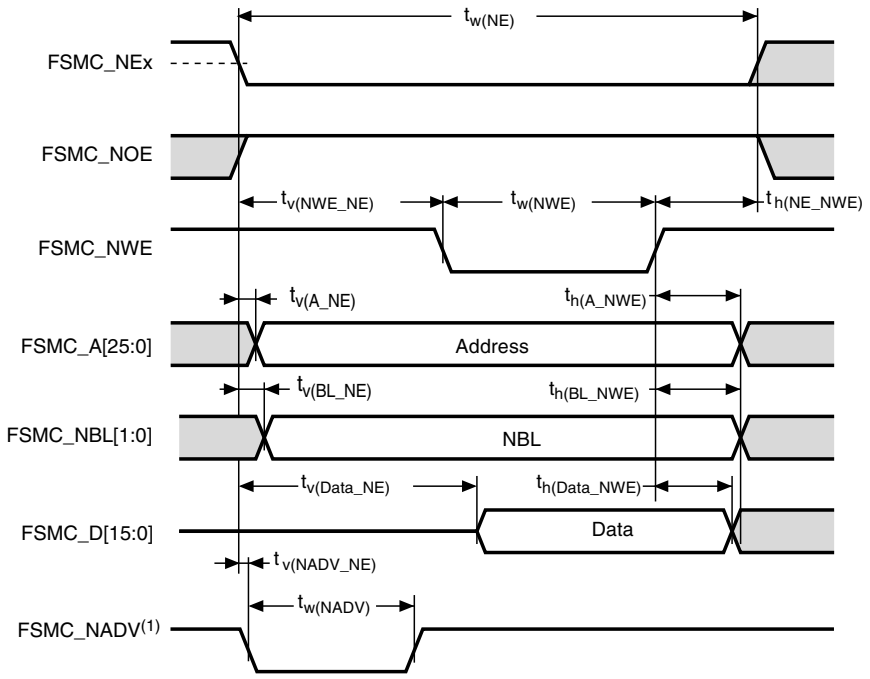
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	TBD	TBD	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	TBD	TBD	ns
$t_{w(NOE)}$	FSMC_NOE low time	TBD	TBD	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	TBD	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	TBD	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	TBD	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns

Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	TBD	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	TBD	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	TBD	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	TBD	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	TBD	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	TBD	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	TBD	ns

1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

Figure 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	TBD	TBD	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	TBD	TBD	ns
$t_{w(NWE)}$	FSMC_NWE low time	TBD	TBD	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	TBD	-	ns

Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	TBD	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	TBD	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	TBD	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	TBD	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	TBD	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	TBD	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	TBD	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	TBD	ns

1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

Figure 48. Asynchronous multiplexed PSRAM/NOR read waveforms

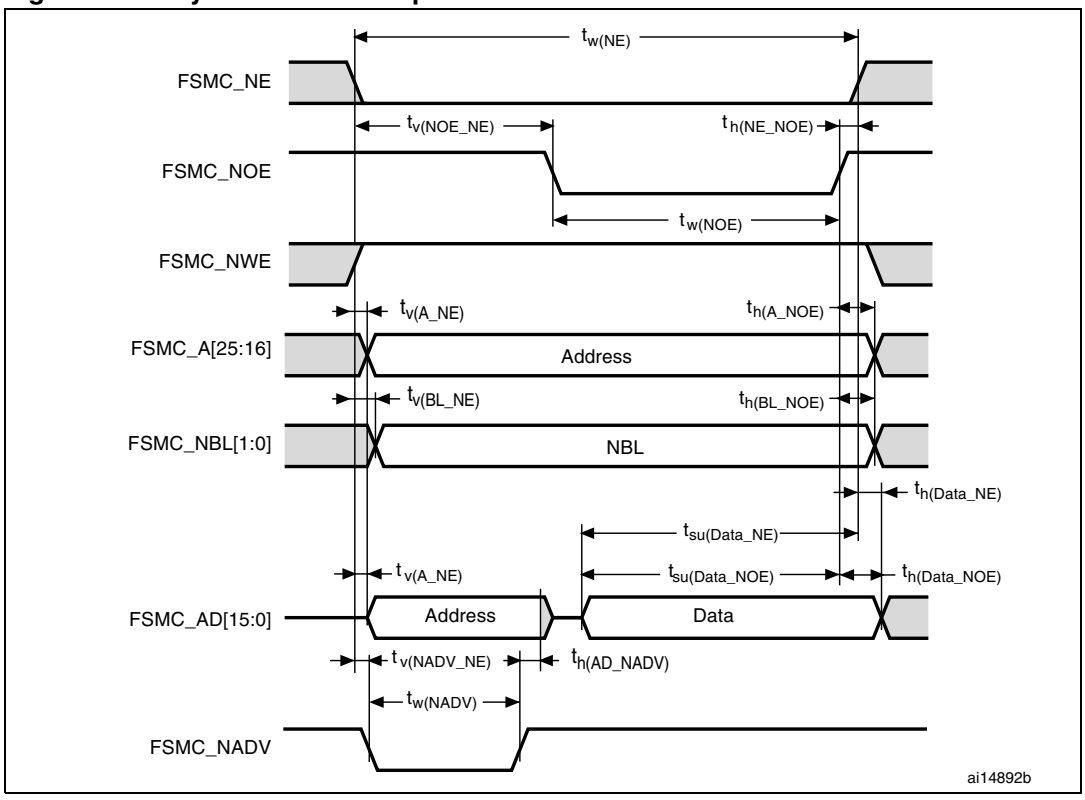


Table 72. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	TBD	TBD	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	TBD	TBD	ns
$t_{w(NOE)}$	FSMC_NOE low time	TBD	TBD	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	TBD	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	TBD	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	TBD	TBD	ns
$t_{w(NADV)}$	FSMC_NADV low time	TBD	TBD	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	TBD	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	TBD	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	TBD	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	TBD	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	TBD	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	TBD	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	TBD	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	TBD	-	ns

1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

Figure 49. Asynchronous multiplexed PSRAM/NOR write waveforms

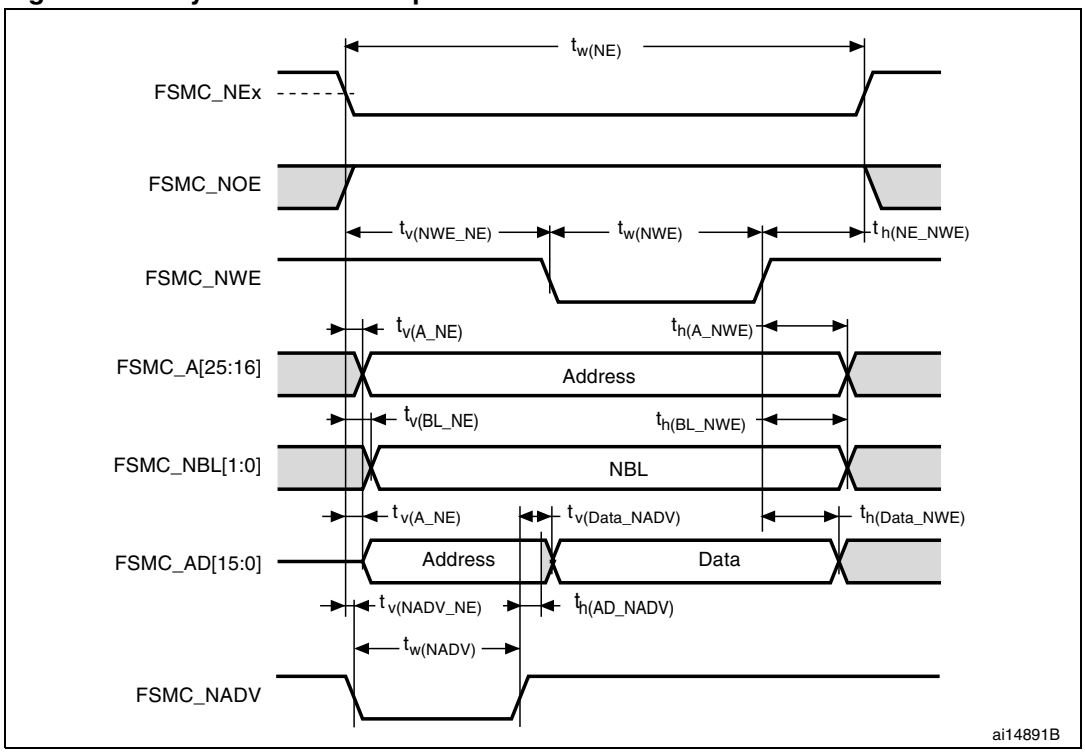


Table 73. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	TBD	TBD	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	TBD	TBD	ns
$t_{w(NWE)}$	FSMC_NWE low time	TBD	TBD	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	TBD	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	TBD	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	TBD	TBD	ns
$t_{w(NADV)}$	FSMC_NADV low time	TBD	TBD	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	TBD	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	TBD	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	TBD	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	TBD	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	TBD	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	TBD	-	ns

1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

Synchronous waveforms and timings

Figure 50 through *Figure 53* represent synchronous waveforms and *Table 75* through *Table 77* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F20xxx/21xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 50. Synchronous multiplexed NOR/PSRAM read timings

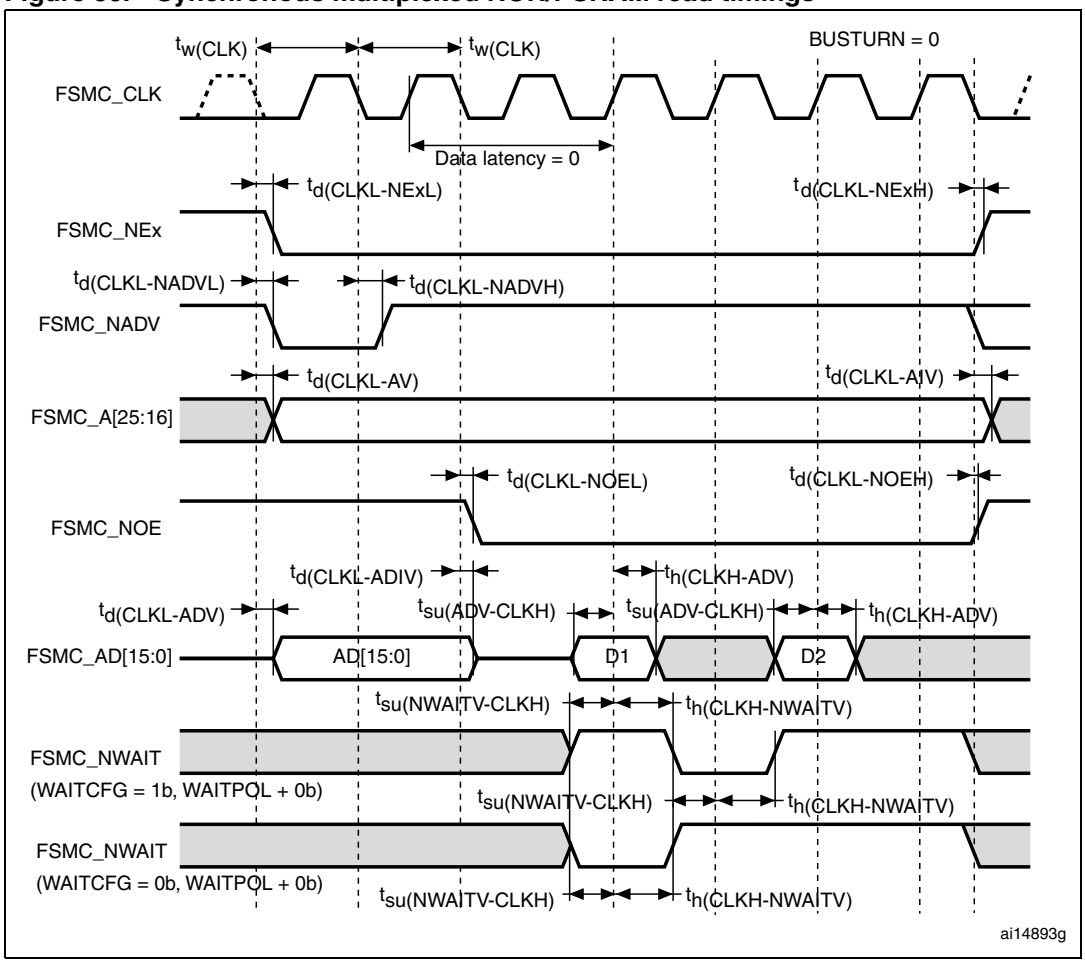


Table 74. Synchronous multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	16.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	TBD	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	TBD	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	TBD	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	TBD	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	TBD	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	TBD	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	TBD	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	TBD	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	TBD	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	TBD	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	TBD	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	TBD	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	TBD	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns

1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

Figure 51. Synchronous multiplexed PSRAM write timings

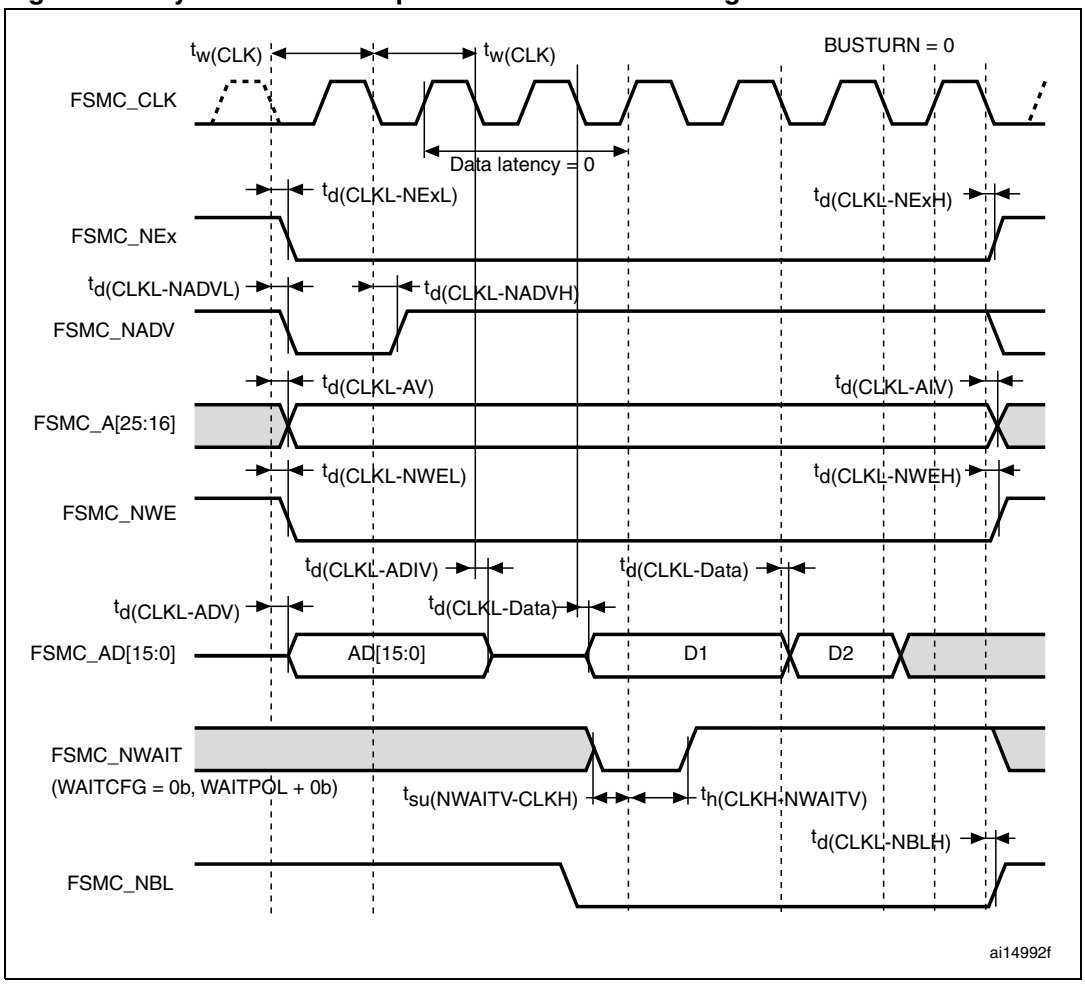


Table 75. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	TBD	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	TBD	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	TBD	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	TBD	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	TBD	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	TBD	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	TBD	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	TBD	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	TBD	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	TBD	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	TBD	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	TBD	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	TBD	-	ns

1. C_L = 15 pF.
2. Preliminary values.

Figure 52. Synchronous non-multiplexed NOR/PSRAM read timings

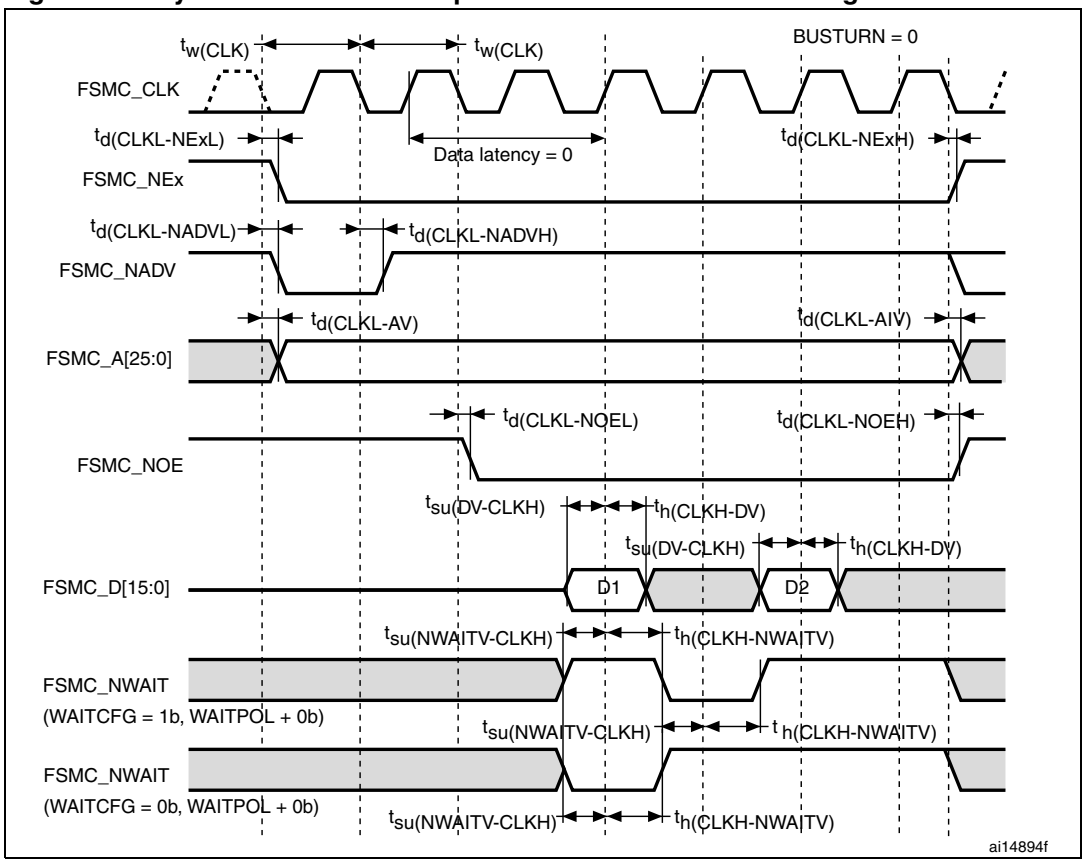


Table 76. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	TBD	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	TBD	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	TBD	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	TBD	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	TBD	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	TBD	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	TBD	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	TBD	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	TBD	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	TBD	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	TBD	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns

1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

Figure 53. Synchronous non-multiplexed PSRAM write timings

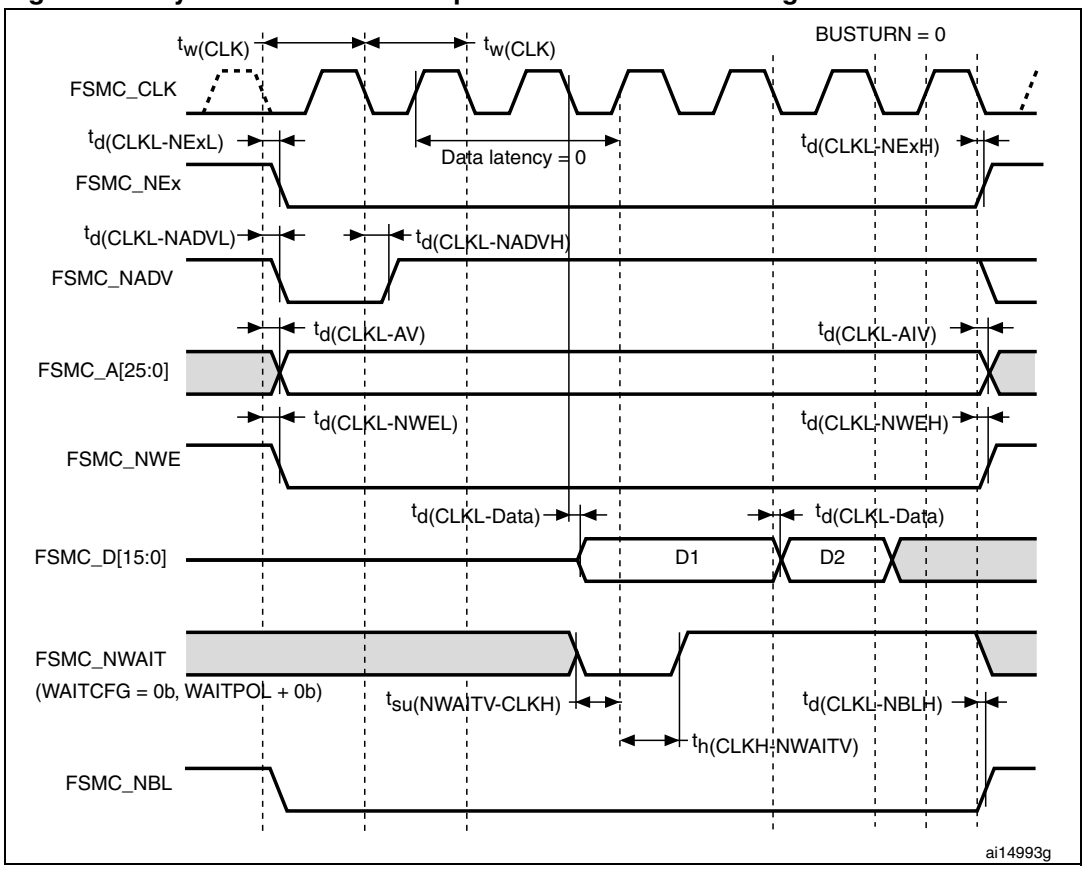


Table 77. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	TBD	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	TBD	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	TBD	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	TBD	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	TBD	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	TBD		ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	TBD	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	TBD	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	TBD	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	TBD	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	TBD	-	ns

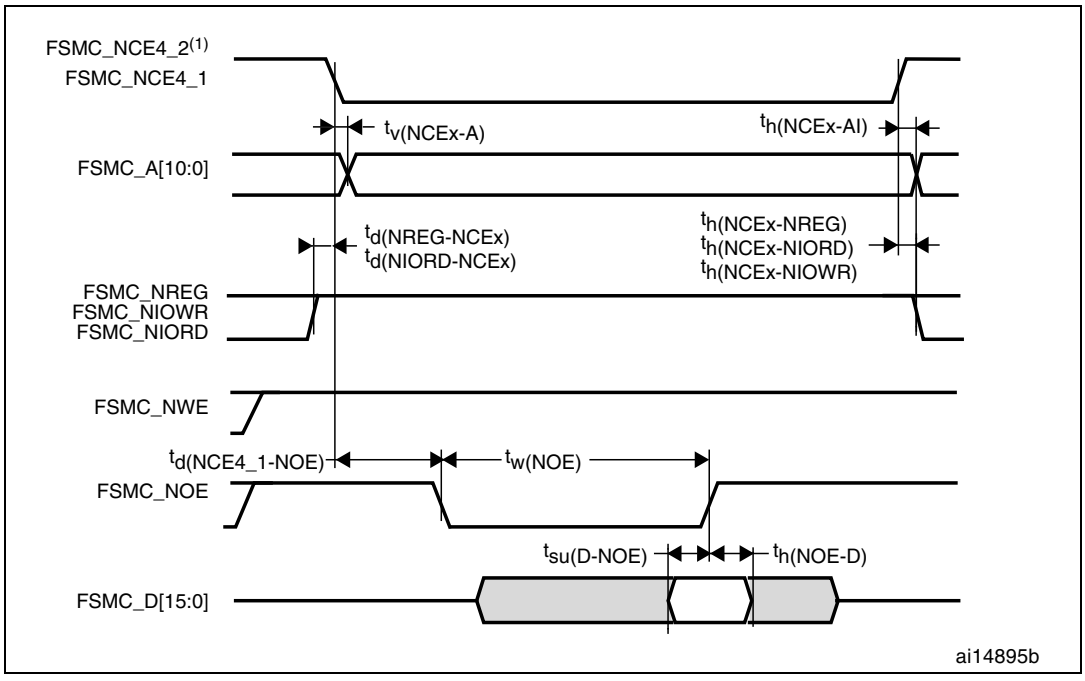
1. C_L = 15 pF.
2. Preliminary values.
3. TBD stands for “to be defined”.

PC Card/CompactFlash controller waveforms and timings

Figure 54 through *Figure 59* represent synchronous waveforms and *Table 78* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 54. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 55. PC Card/CompactFlash controller waveforms for common memory write access

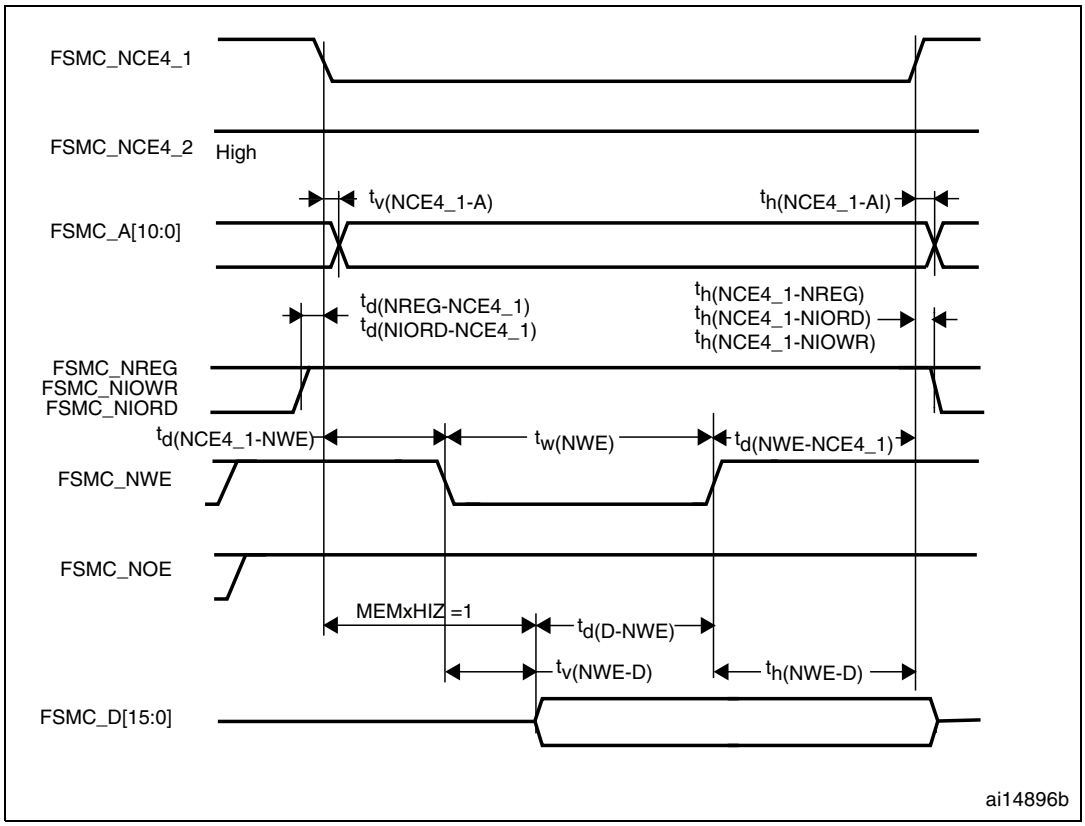
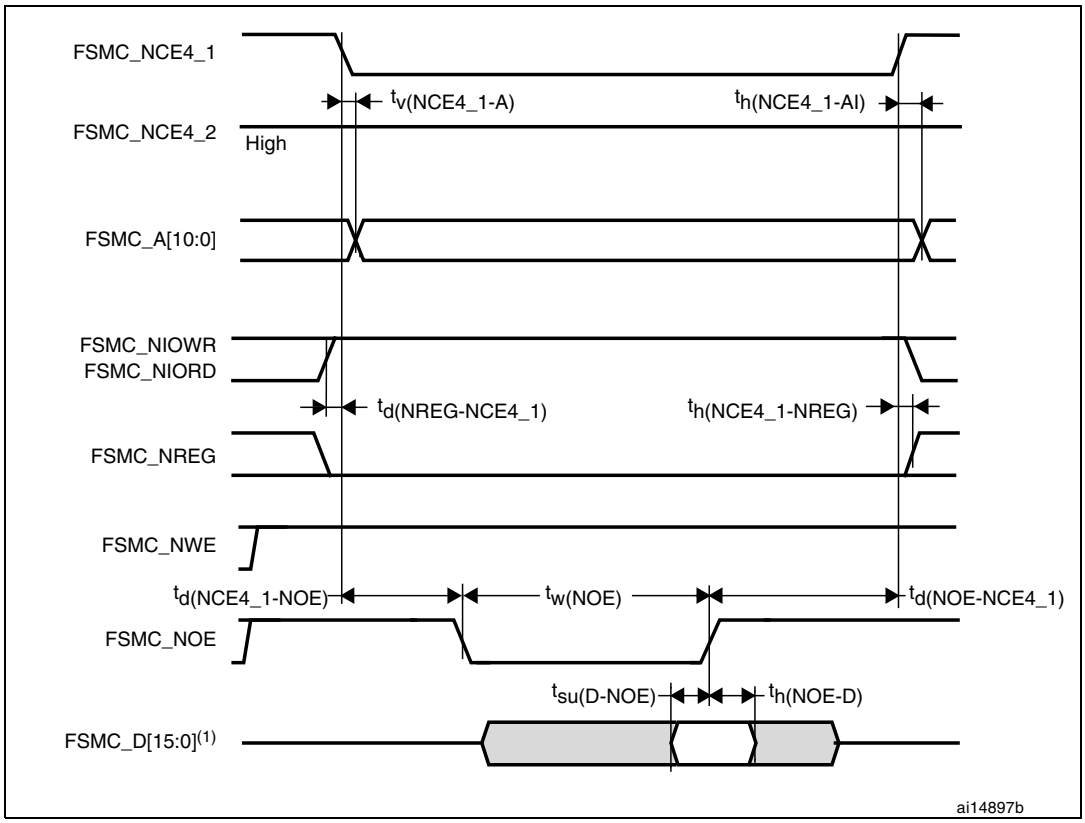
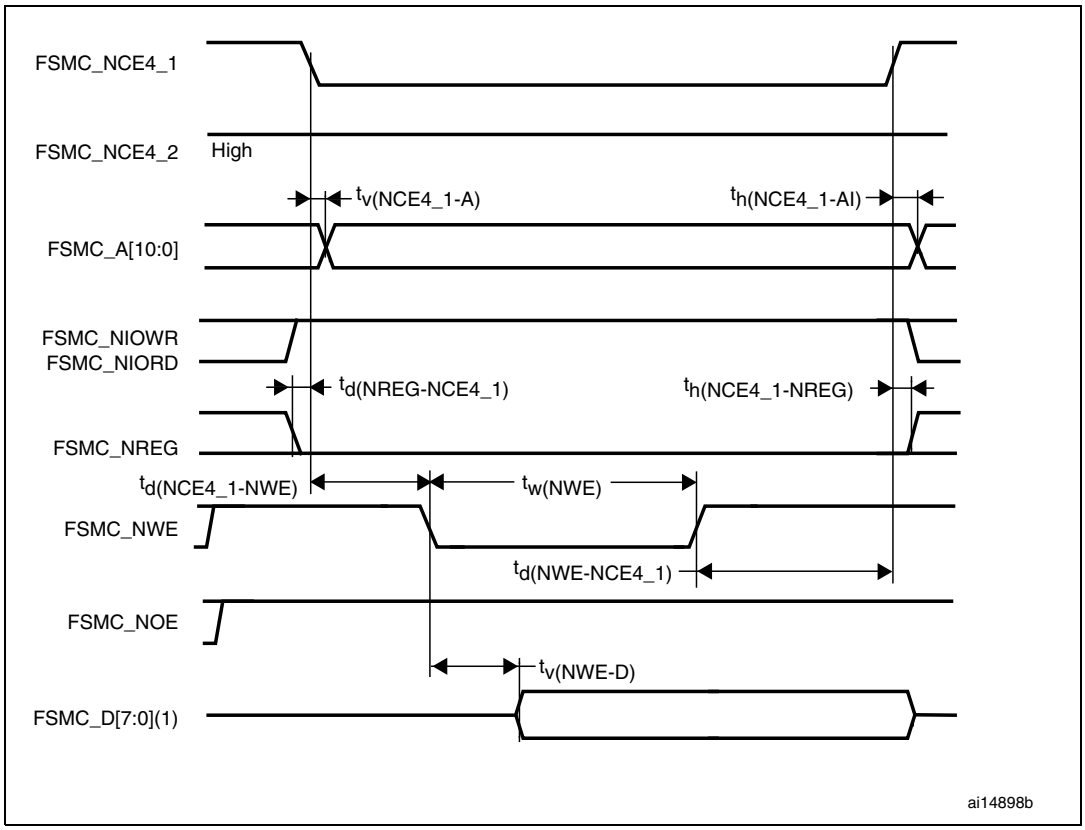


Figure 56. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 57. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Figure 58. PC Card/CompactFlash controller waveforms for I/O space read access

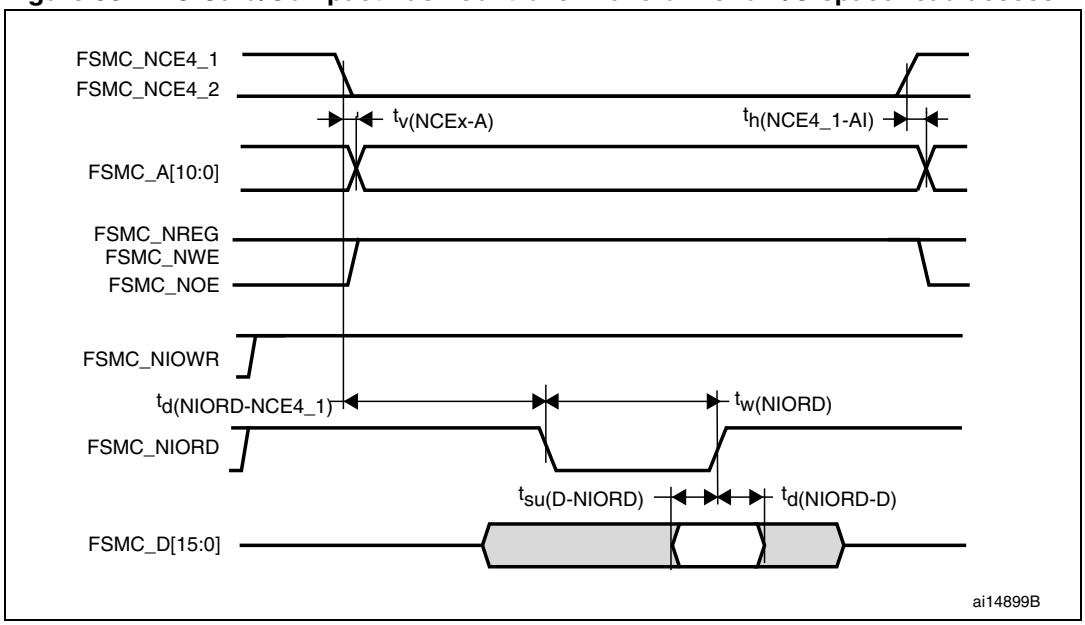


Figure 59. PC Card/CompactFlash controller waveforms for I/O space write access

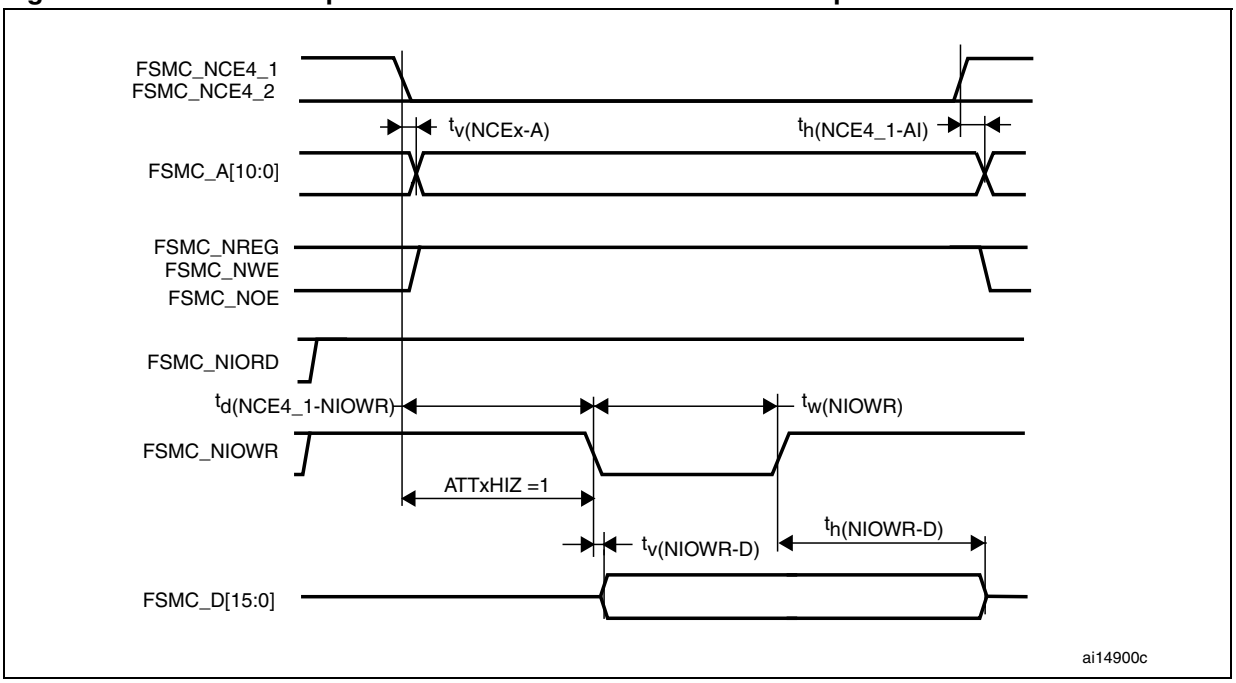


Table 78. Switching characteristics for PC Card/CF read and write cycles(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$ $t_{v(NCE4\_1-A)}$	FSMC_NCEx low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) FSMC_NCE4_1 low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10)	-	TBD	ns
$t_{h(NCEx-AI)}$ $t_{h(NCE4\_1-AI)}$	FSMC_NCEx high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) FSMC_NCE4_1 high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10)	TBD		ns
$t_{d(NREG-NCEx)}$ $t_{d(NREG-NCE4\_1)}$	FSMC_NCEx low to FSMC_NREG valid FSMC_NCE4_1 low to FSMC_NREG valid	-	TBD	ns
$t_{h(NCEx-NREG)}$ $t_{h(NCE4\_1-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid FSMC_NCE4_1 high to FSMC_NREG invalid	TBD	-	ns
$t_{d(NCE4\_1-NOE)}$	FSMC_NCE4_1 low to FSMC_NOE low	-	TBD	ns
$t_{w(NOE)}$	FSMC_NOE low width	TBD	TBD	ns
$t_{d(NOE-NCE4\_1}$	FSMC_NOE high to FSMC_NCE4_1 high	TBD	-	ns
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	TBD	-	ns
$t_{h(NOE-D)}$	FSMC_D[15:0] valid data after FSMC_NOE high	TBD	-	ns
$t_{w(NWE)}$	FSMC_NWE low width	TBD	TBD	ns
$t_{d(NWE-NCE4\_1)}$	FSMC_NWE high to FSMC_NCE4_1 high	TBD	-	ns
$t_{d(NCE4\_1-NWE)}$	FSMC_NCE4_1 low to FSMC_NWE low	-	TBD	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	TBD	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	TBD	-	ns
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	TBD	-	ns

Table 78. Switching characteristics for PC Card/CF read and write cycles(1)(2)(3) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	TBD	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	TBD	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	TBD	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	TBD	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	TBD	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	TBD	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	TBD	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	TBD	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	TBD	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	TBD	-	ns

1. C_L = 15 pF.
2. Based on characterization, not tested in production.
3. TBD stands for “to be defined”.

NAND controller waveforms and timings

Figure 60 through *Figure 63* represent synchronous waveforms and *Table 79* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 60. NAND controller waveforms for read access

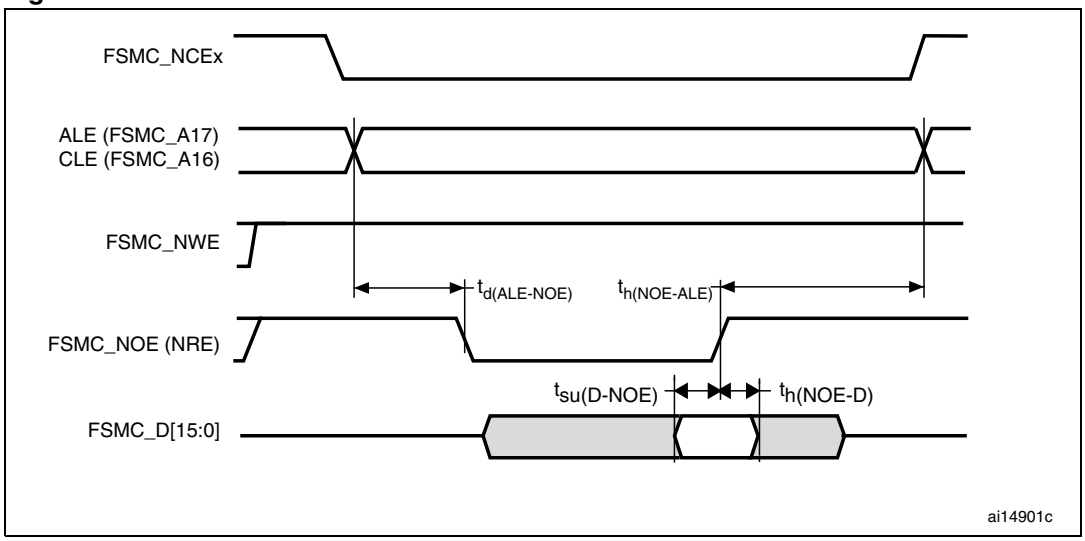


Figure 61. NAND controller waveforms for write access

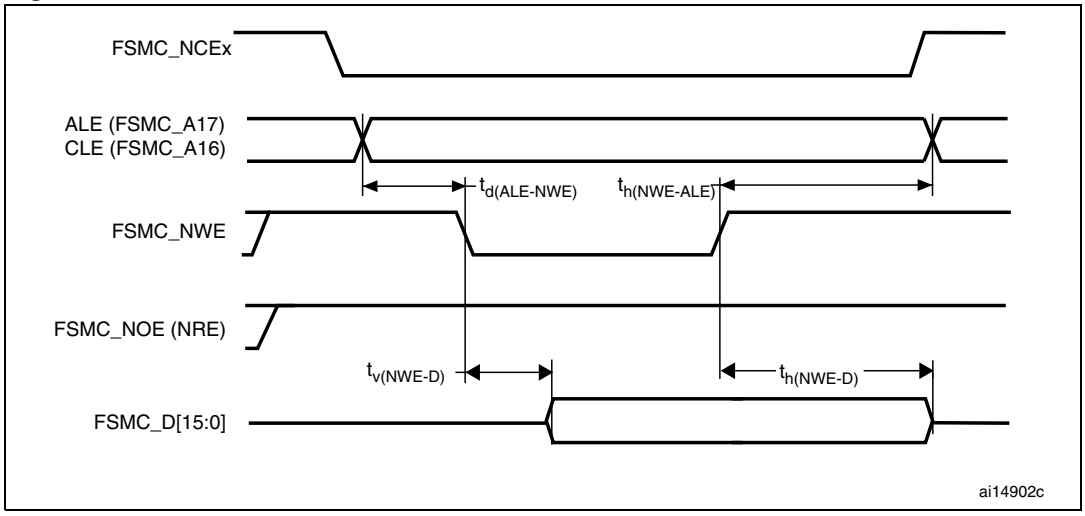


Figure 62. NAND controller waveforms for common memory read access

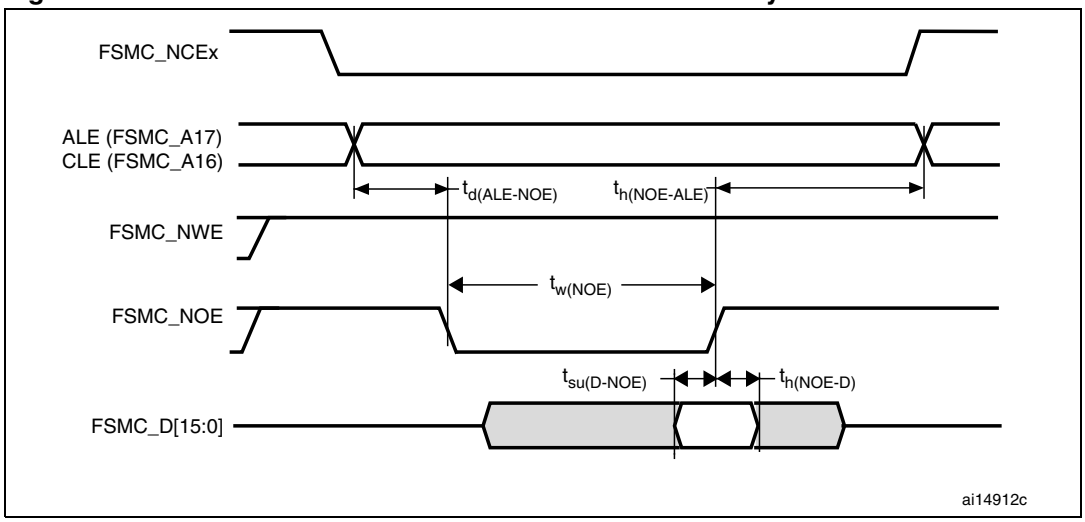


Figure 63. NAND controller waveforms for common memory write access

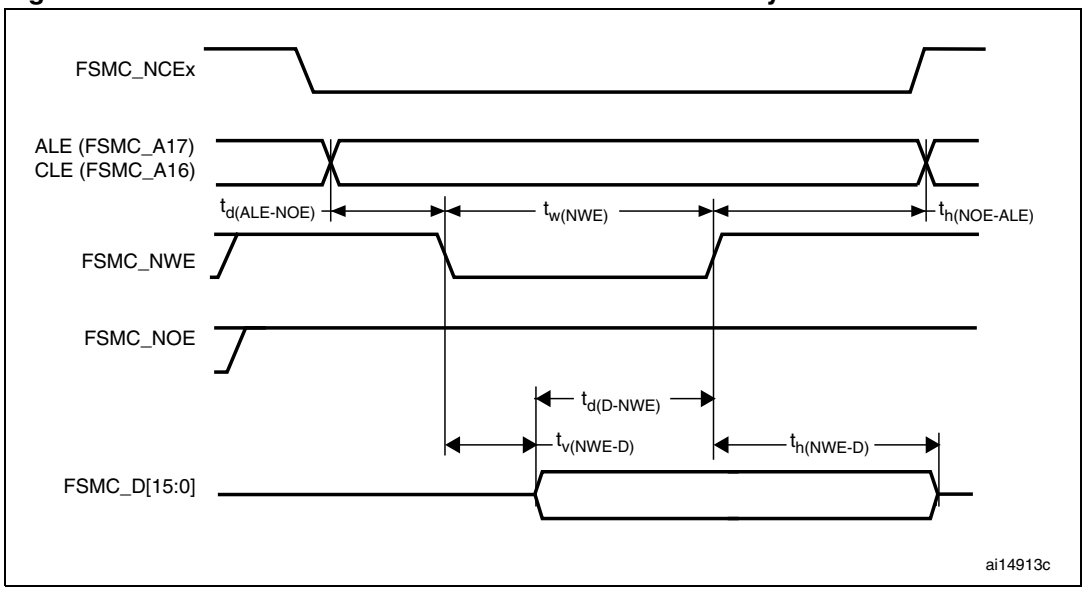


Table 79. Switching characteristics for NAND Flash read and write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$(3)	FSMC_D[15:0] valid before FSMC_NWE high	TBD	-	ns
$t_{w(NOE)}$(3)	FSMC_NOE low width	TBD	TBD	ns
$t_{su(D-NOE)}$(3)	FSMC_D[15:0] valid data before FSMC_NOE high	TBD	-	ns
$t_{h(NOE-D)}$(3)	FSMC_D[15:0] valid data after FSMC_NOE high	TBD	-	ns
$t_{w(NWE)}$(3)	FSMC_NWE low width	TBD	TBD	ns
$t_{v(NWE-D)}$(3)	FSMC_NWE low to FSMC_D[15:0] valid	-	TBD	ns
$t_{h(NWE-D)}$(3)	FSMC_NWE high to FSMC_D[15:0] invalid	TBD	-	ns

Table 79. Switching characteristics for NAND Flash read and write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{d(ALE-NWE)}$(4)	FSMC_ALE valid before FSMC_NWE low	-	TBD	ns
$t_{h(NWE-ALE)}$(4)	FSMC_NWE high to FSMC_ALE invalid	TBD	-	ns
$t_{d(ALE-NOE)}$(4)	FSMC_ALE valid before FSMC_NOE low	-	TBD	ns
$t_{h(NOE-ALE)}$(4)	FSMC_NWE high to FSMC_ALE invalid	TBD	-	ns

1. C_L = 15 pF.
2. TBD stands for “to be defined”.
3. Based on characterization, not tested in production.
4. Guaranteed by design, not tested in production.

5.3.26 Camera interface (DCMI) timing specifications

Table 80. DCMI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}(1)			0.4	

1. Maximum value of DCMI_PIXCLK = 54 MHz.

5.3.27 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 81* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 64. SDIO high-speed mode

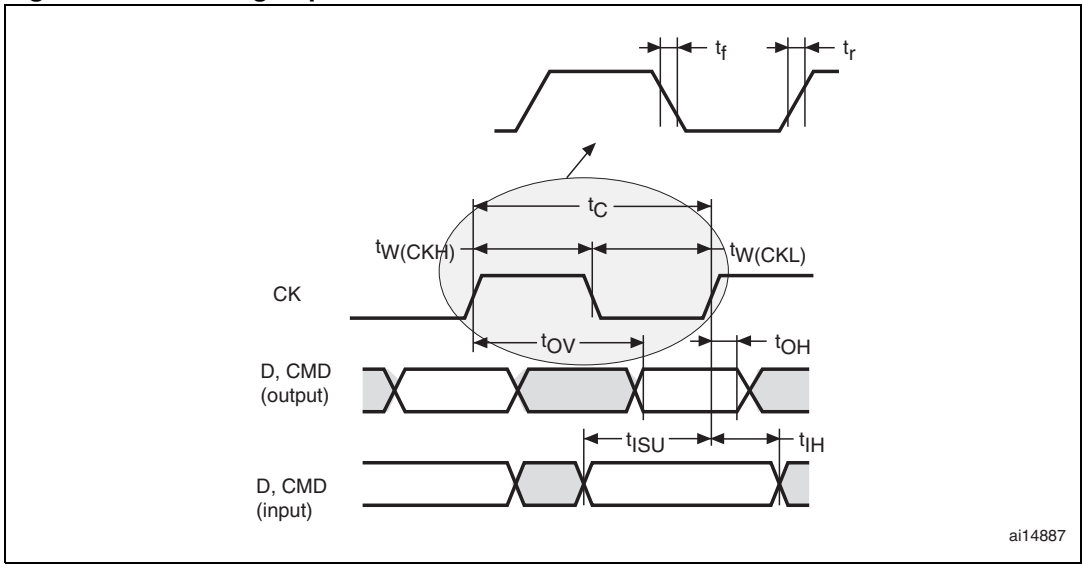


Figure 65. SD default mode

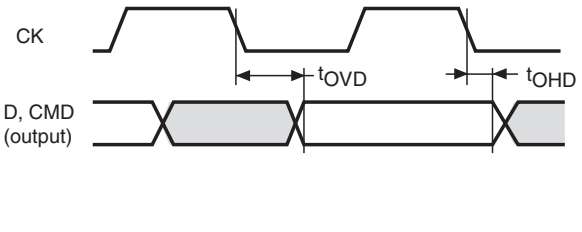


Table 81. SD / MMC characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	TBD	TBD	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	TBD	-
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	TBD	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	TBD	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	TBD	
t_f	Clock fall time	$C_L \leq 30$ pF	-	TBD	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	TBD	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	TBD	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	TBD	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	TBD	-	
CMD, D outputs (referenced to CK) in SD default mode(2)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	TBD	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	TBD	-	

1. TBD stands for “to be defined”.
2. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

5.3.28 RTC characteristics

Table 82. RTC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-	-

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 66. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline(1)

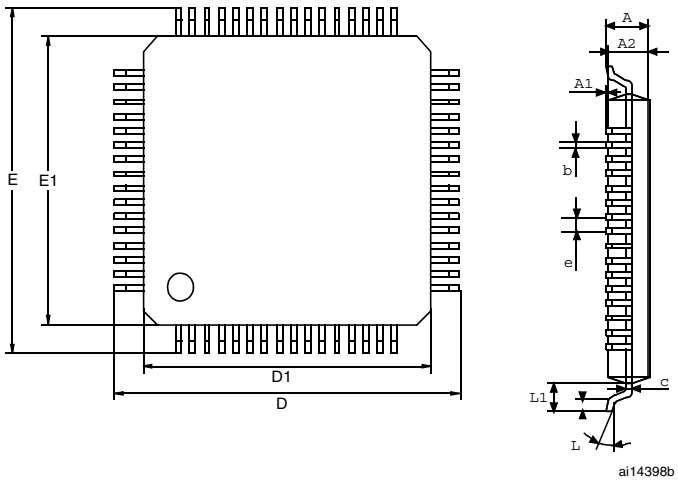
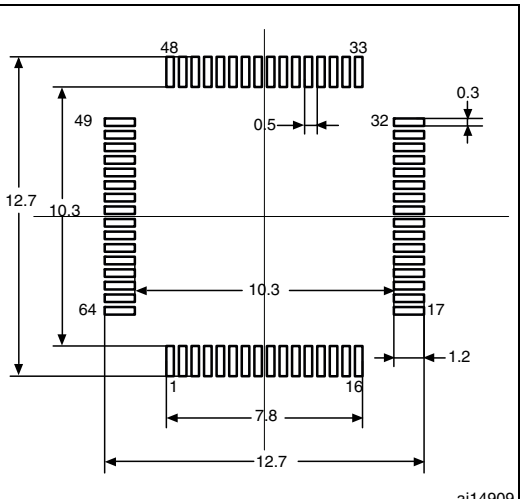


Figure 67. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 83. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D		12.000			0.4724	
D1		10.000			0.3937	
E		12.000			0.4724	
E1		10.000			0.3937	
e		0.500			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 68. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline(1)

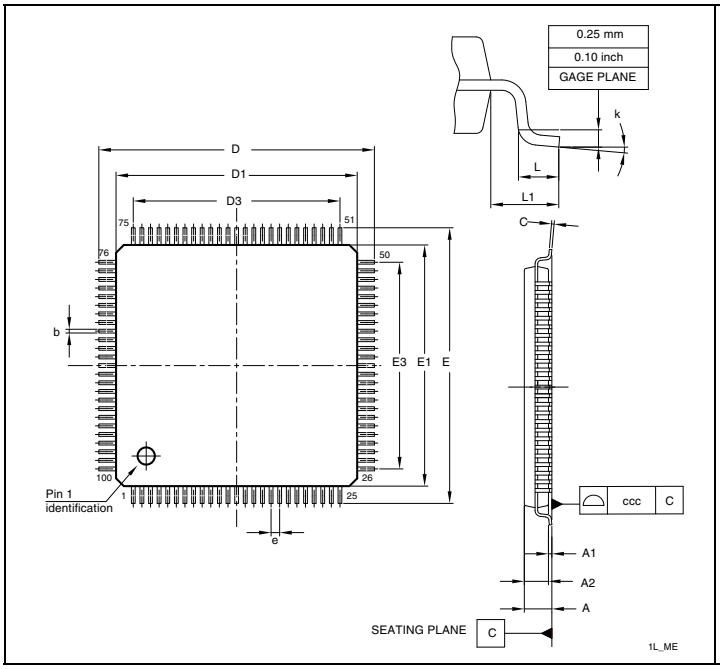
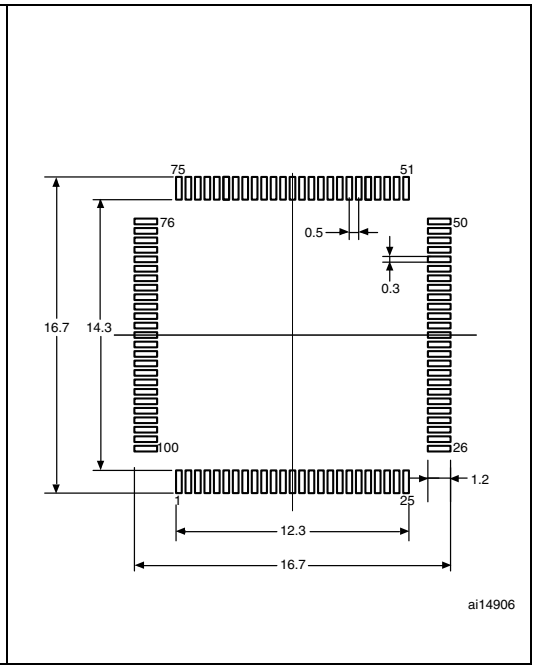


Figure 69. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 84. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	
E	15.80v	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline(1)

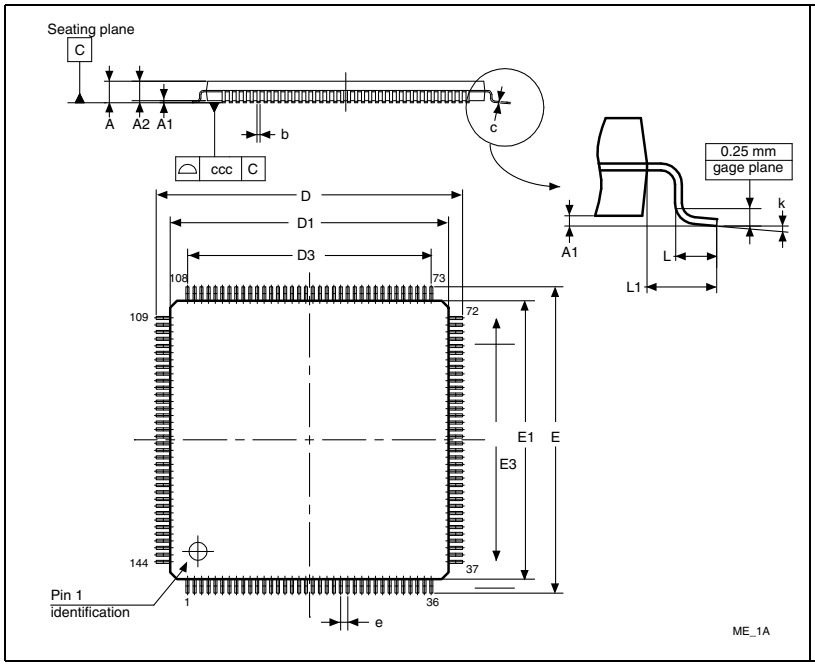
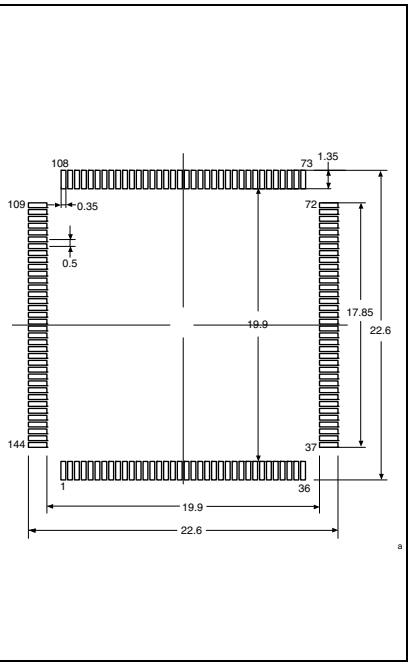


Figure 71. Recommended footprint(1)(2)



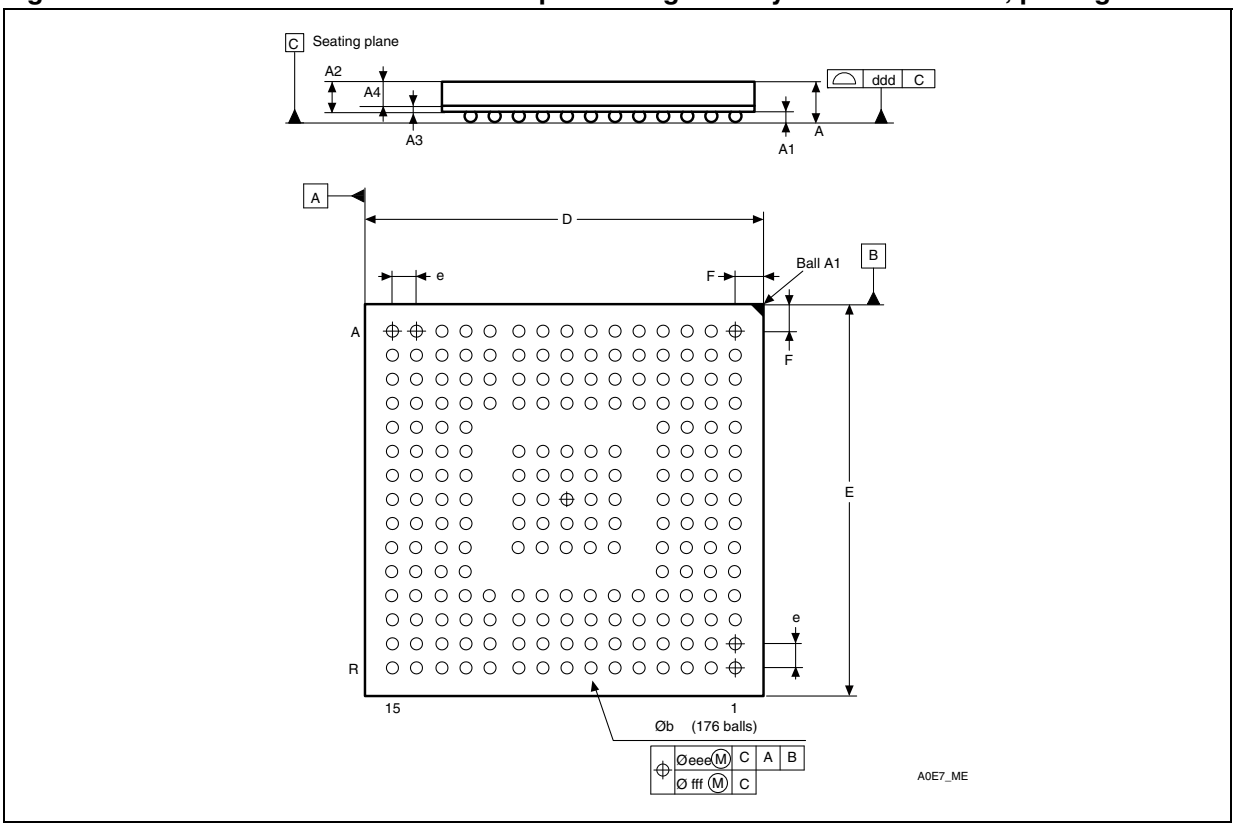
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 85. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3		17.500			0.689	
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3		17.500			0.6890	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 72. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline



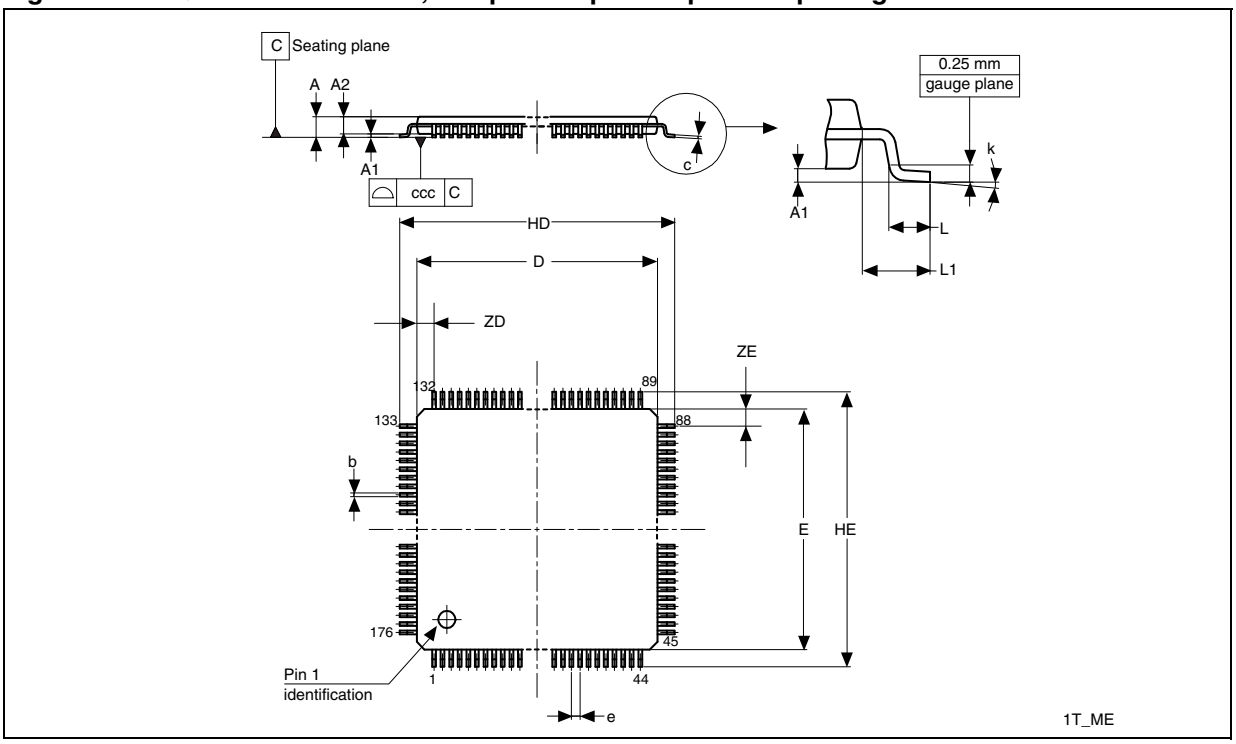
1. Drawing is not to scale.

Table 86. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3		0.130			0.0051	
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3740	0.3937	0.3957
E	9.950	10.000	10.050	0.3740	0.3937	0.3957
e	0.600	0.650	0.700	0.0236	0.0256	0.0276
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd		0.080			0.0031	
eee		0.150			0.0059	
fff		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 73. LQFP176 24 x 24 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 87. LQFP176, 24 x 24 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		
A2	1.350		1.450	0.0531		0.0060
b	0.170		0.270	0.0067		0.0106
C	0.090		0.200	0.0035		0.0079
D	23.900		24.100	0.9409		0.9488
E	23.900		24.100	0.9409		0.9488
e		0.500			0.0197	
HD	25.900		26.100	1.0200		1.0276
HE	25.900		26.100	1.0200		1.0276
L	0.450		0.750	0.0177		0.0295
L1		1.000			0.0394	
ZD		1.250			0.0492	
ZE		1.250			0.0492	
ccc			0.080			0.0031
k	0 °		7 °	0 °		7 °

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 88. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP 144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Part numbering

Table 89. Ordering information scheme

Example: STM32 F 405 R E T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

405 = STM32F40x, connectivity, USB OTG FS/HS,

407= STM32F40x, connectivity, USB OTG FS/HS, camera interface, Ethernet

Pin count

R = 64 pins or 66 pins
V = 100 pins
Z = 144 pins
I = 176 pins

Flash memory size

C = 256 Kbytes of Flash memory
E = 512 Kbytes of Flash memory
F = 768 Kbytes of Flash memory
G = 1024 Kbytes of Flash memory

Package

T = LQFP
H = UFBGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Application block diagrams

A.1 Main applications versus package

Table 90 gives examples of configurations for each package.

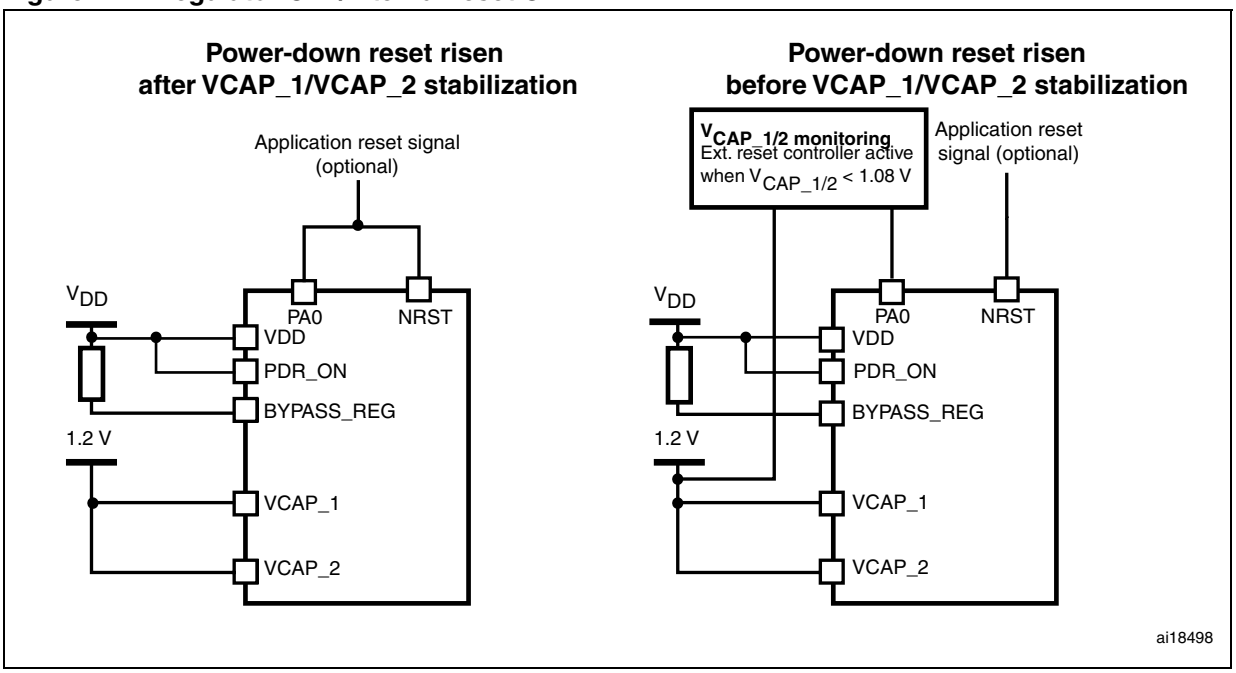
Table 90. Main applications versus package for STM32F407xx microcontrollers(1)

		64 pins			100 pins				144 pins				176 pins	
		Config 1	Config 2	Config 3	Config 1	Config 2	Config 3	Config 4	Config 1	Config 2	Config 3	Config 4	Config 1	Config 2
USB 1	OTG FS	X	X	X	X	X	X	-	X		X		X	
	FS	X	X	X	X	X	X	X	X	X	X	X	X	
USB 2	HS ULPI	-	-	-	X	-	-	-	X	X			X	X
	OTGFS	-	-	-	X				X	X			X	X
	FS	-	-	-	X	X	X	X	X	X	X	X	X	X
Ethernet	MII	-	-	-	-	-	X	X			X	X	X	X
	RMII	-	-	-	-	X	X	X	X	X	X	X	X	X
SPI/I2S2 SPI/I2S3		-	X	-	-	X	X	X	X	X	X	X	X	X
SDIO	SDIO	SDIO or DCMI	SDIO or DCMI	-	SDIO or DCMI	SDIO or DCMI	SDIO or DCMI	X	SDIO or DCMI	X	SDIO or DCMI	X	X	X
DCMI	8bits Data			-				X		X		X	X	X
	10bits Data			-				X		X		X	X	X
	12bits Data			-				X		X		X	X	X
	14bits Data	-	-	-	-	-	-	-		X		X	X	X
FSMC	NOR/ RAM Muxed	-	-	-	X	X	X	X	X	X	X	X	X	X
	NOR/ RAM	-	-	-					X	X	X	X	X	X
	NAND	-	-	-	X	X	X*22	X*19	X	X*19	X*22	X*19	X*22	X*22
	CF	-	-	-	-	-	-	-	X	X	X	X	X	X
CAN		-	X	X	-	X	X	X	-	-	X	X	-	X

1. X*y: FSMC address limited to “y”.

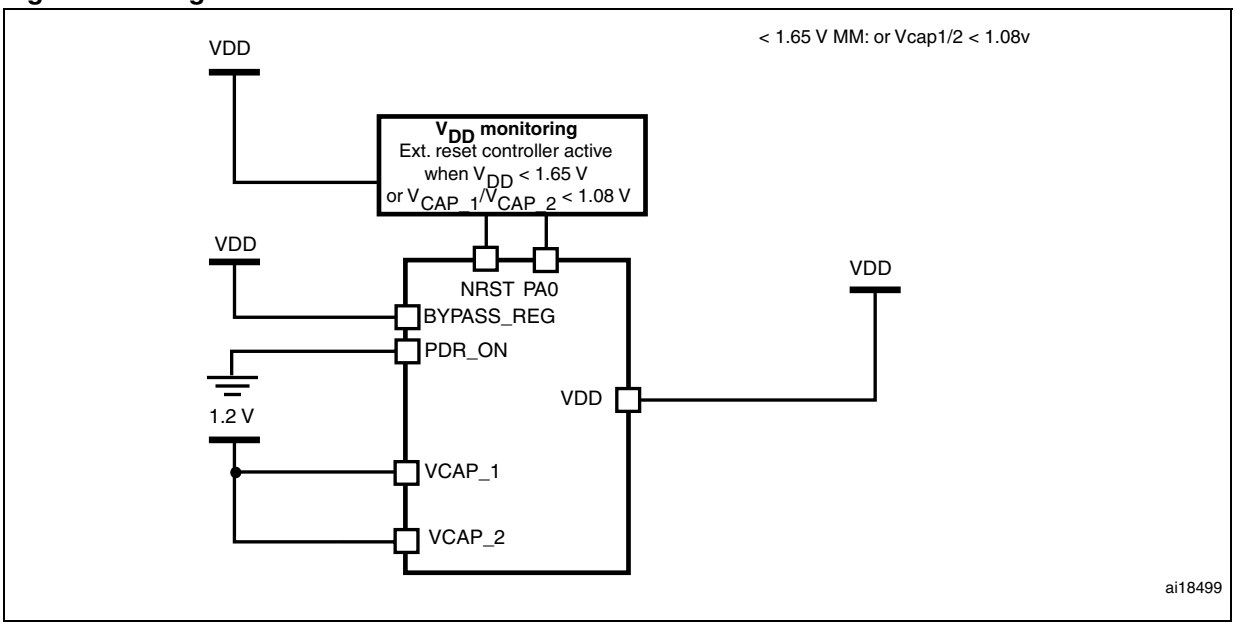
A.2 Application example with regulator OFF

Figure 74. Regulator OFF/internal reset ON



1. This mode is available only on UFBGA176 package.

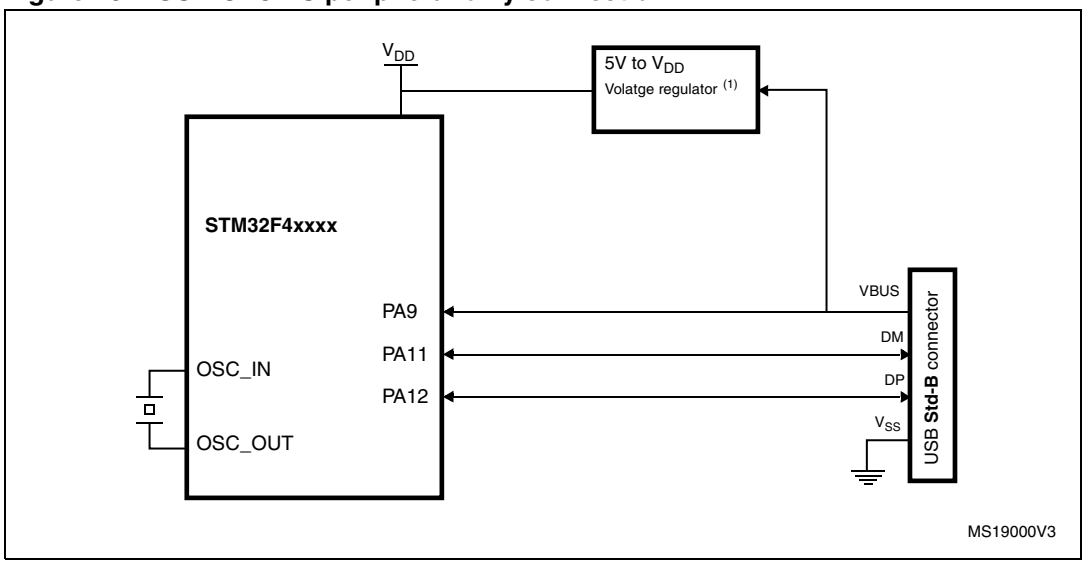
Figure 75. Regulator OFF/internal reset OFF



1. This mode is available only on UFBGA176 package.

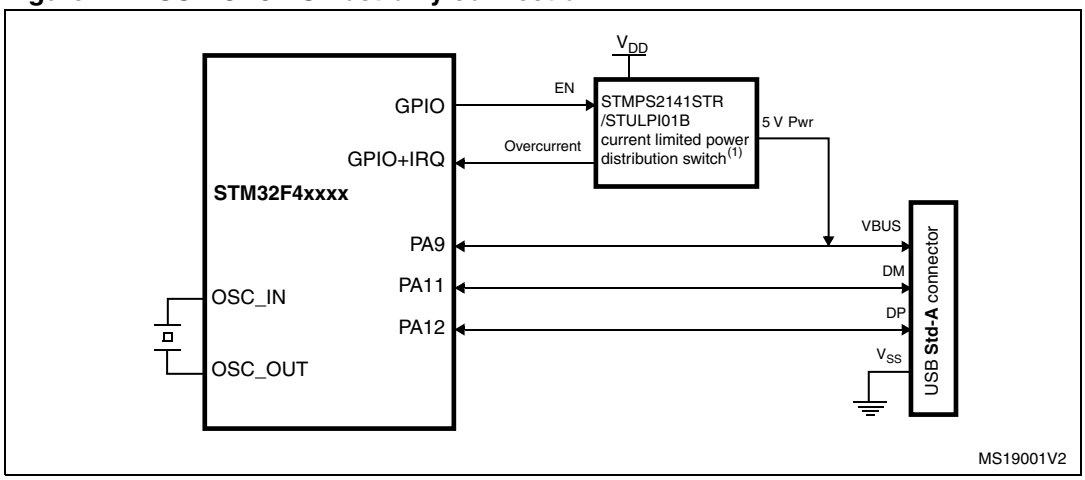
A.3 USB OTG full speed (FS) interface solutions

Figure 76. USB OTG FS peripheral-only connection



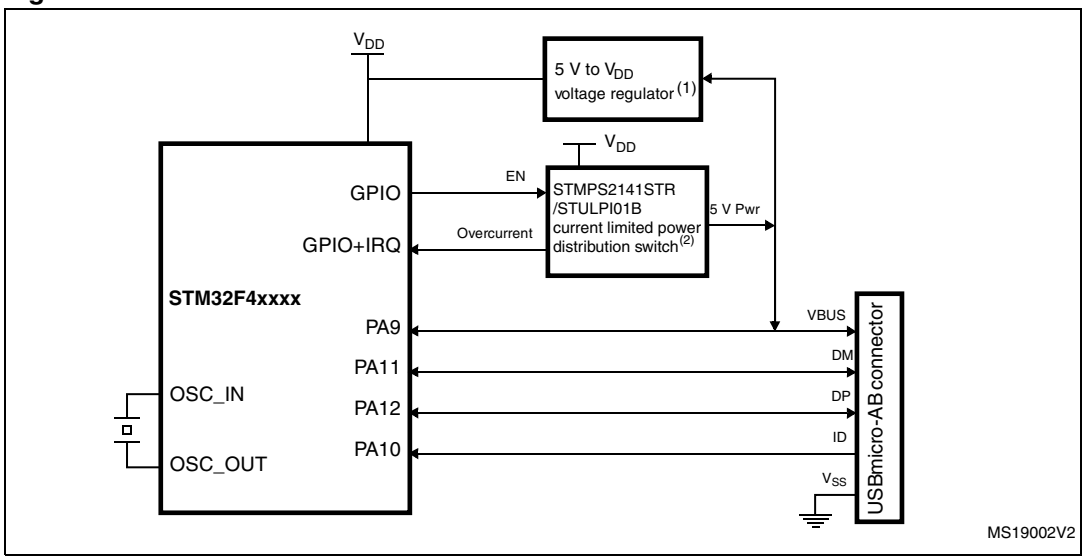
1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 77. USB OTG FS host-only connection



1. STMPS2141STR/STULPI01B needed only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

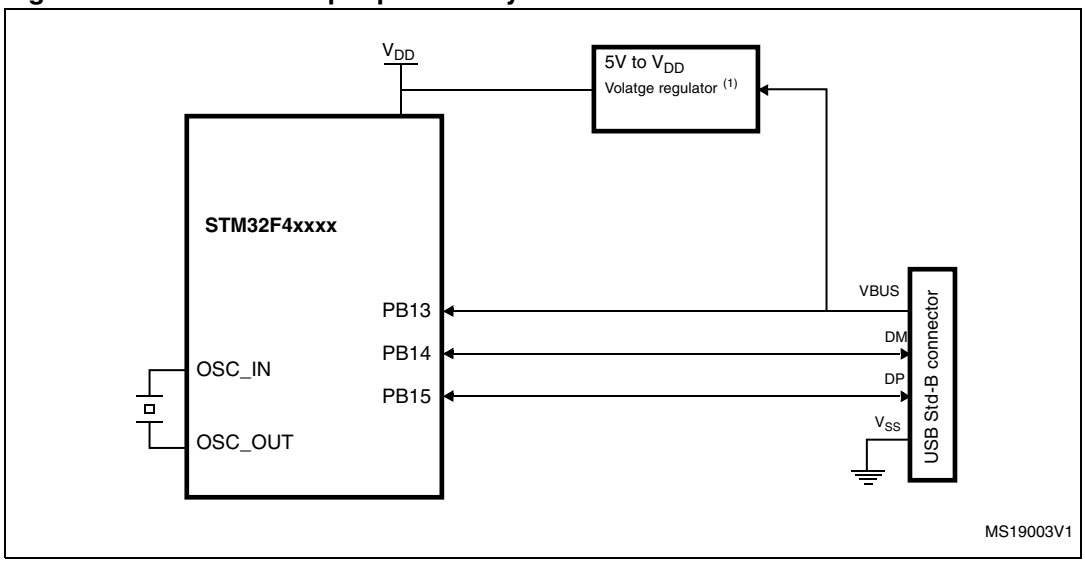
Figure 78. OTG FS connection dual-role with internal PHY



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. STMPS2141STR/STULPI01B needed only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The same application can be developped using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

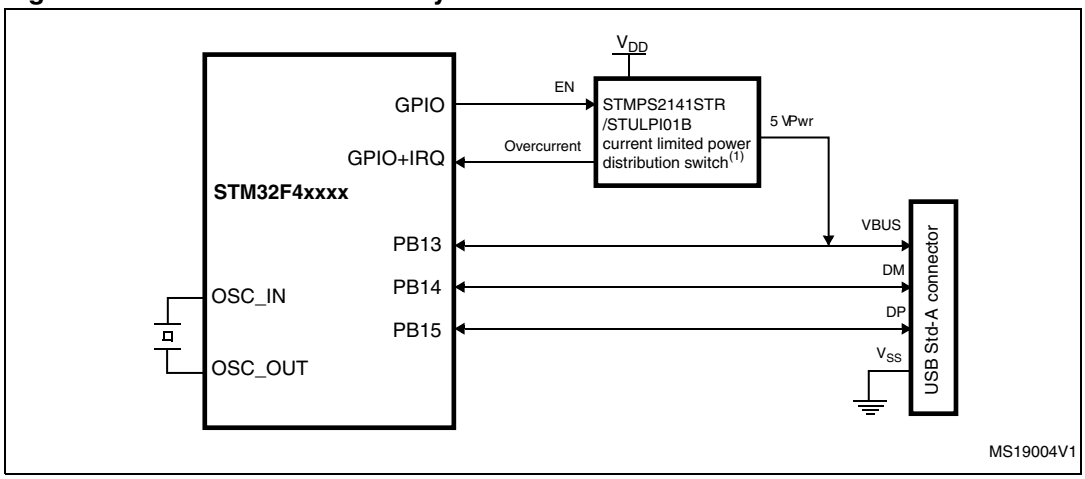
A.4 USB OTG high speed (HS) interface solutions

Figure 79. USB OTG HS peripheral-only connection in FS mode



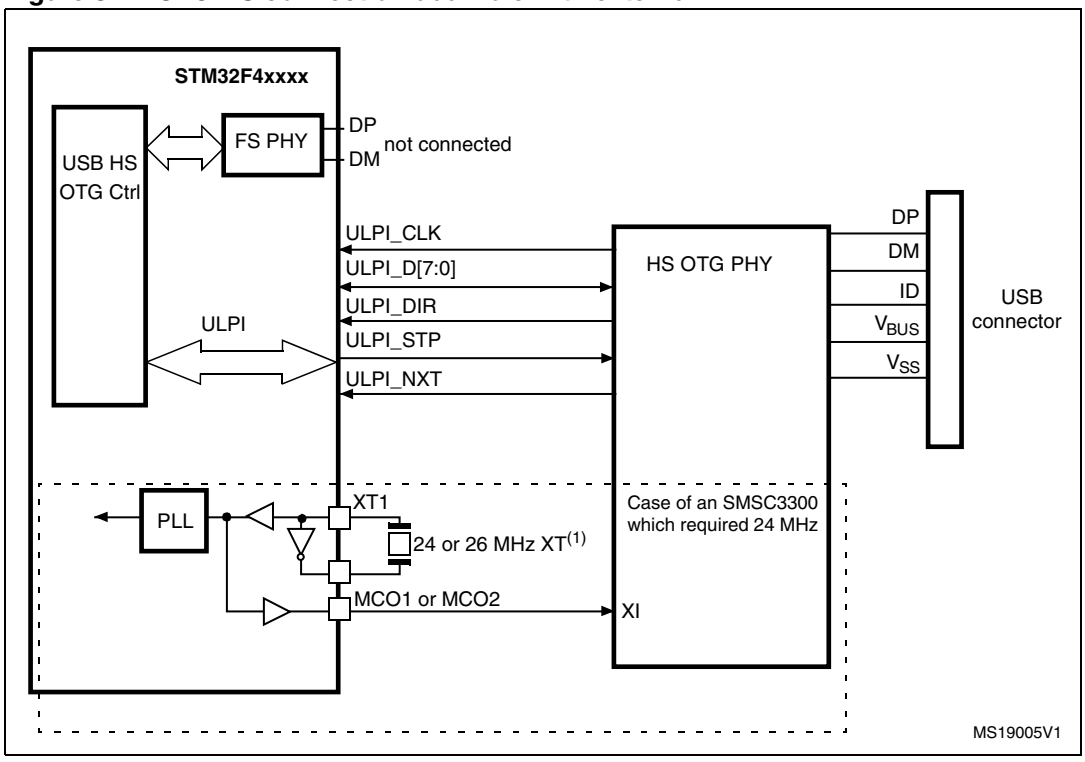
1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 80. USB OTG HS host-only connection in FS mode



1. STMPS2141STR/STULPI01B needed only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

Figure 81. OTG HS connection dual-role with external PHY



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F40x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.

A.5 Complete audio player solutions

Two solutions are offered, illustrated in *Figure 82* and *Figure 83*.

Figure 82 shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I^2S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 82. Complete audio player solution 1

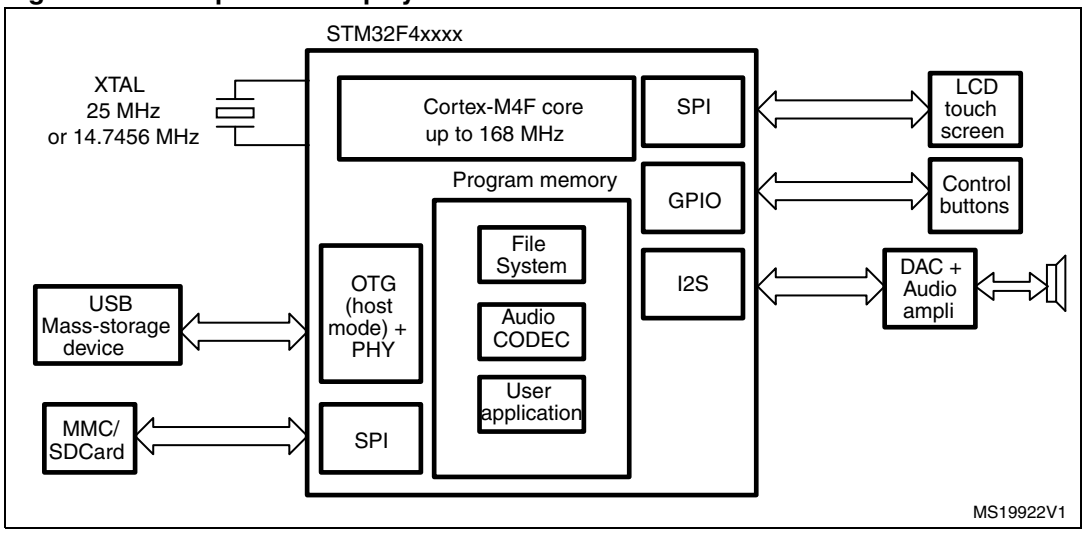


Figure 83 shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

Figure 83. Complete audio player solution 2

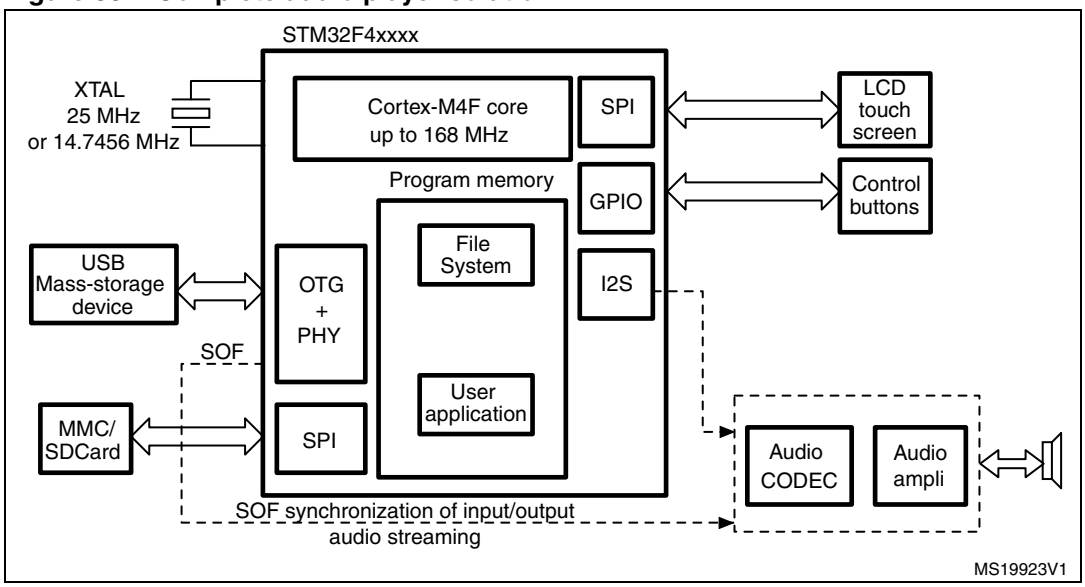


Figure 84. Audio player solution using PLL, PLLI2S, USB and 1 crystal

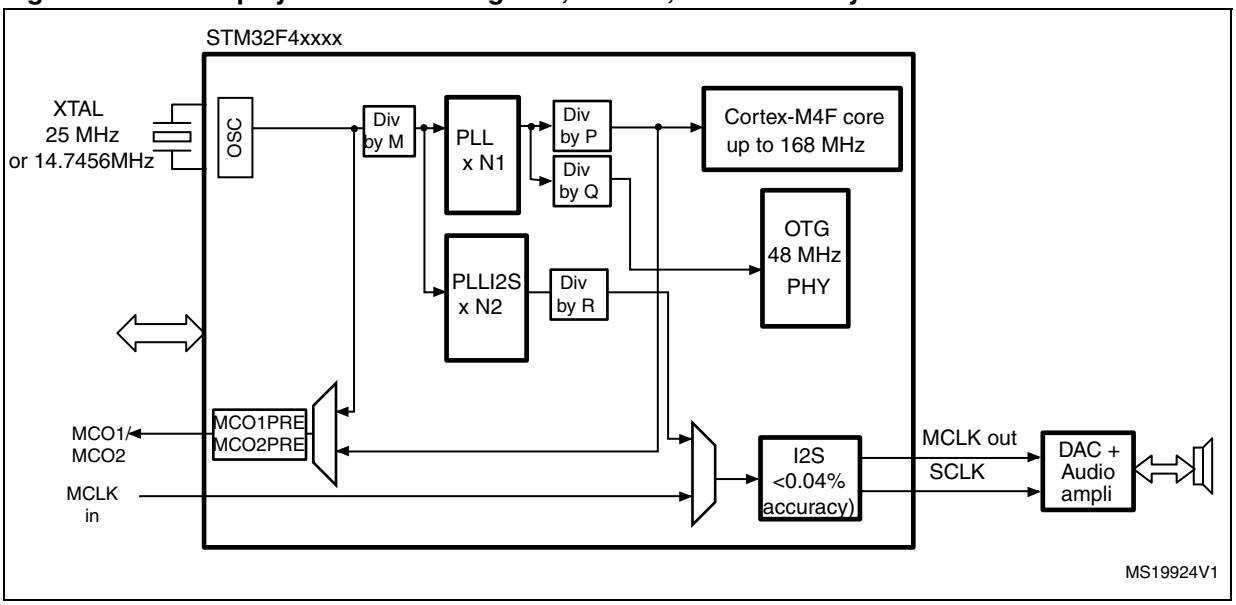


Figure 85. Audio PLL (PLLI2S) providing accurate I2S clock

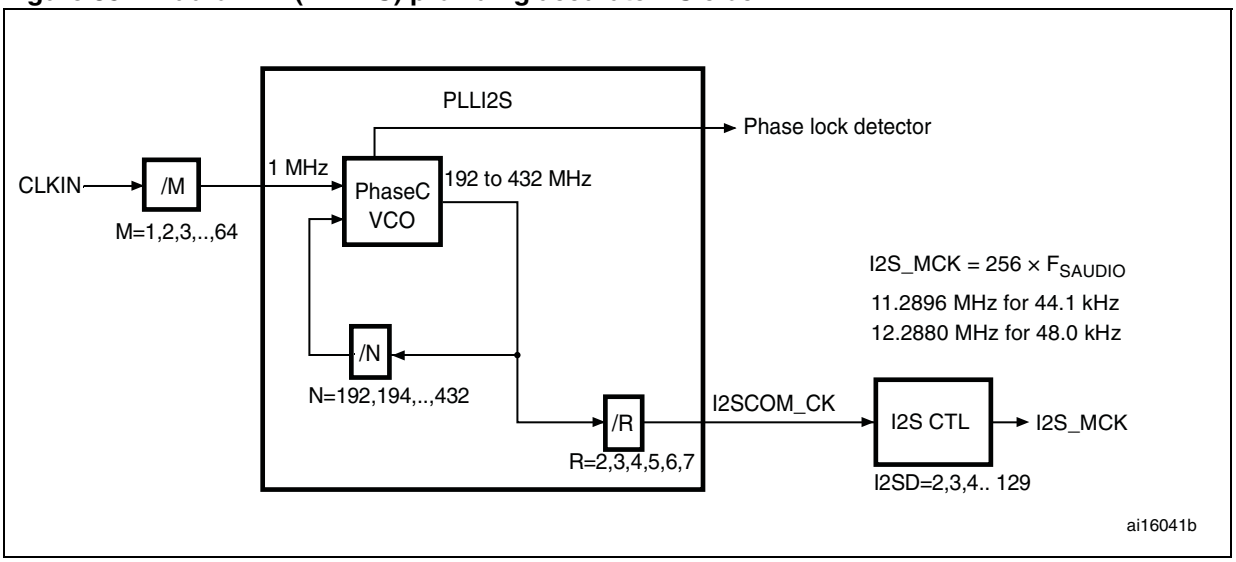
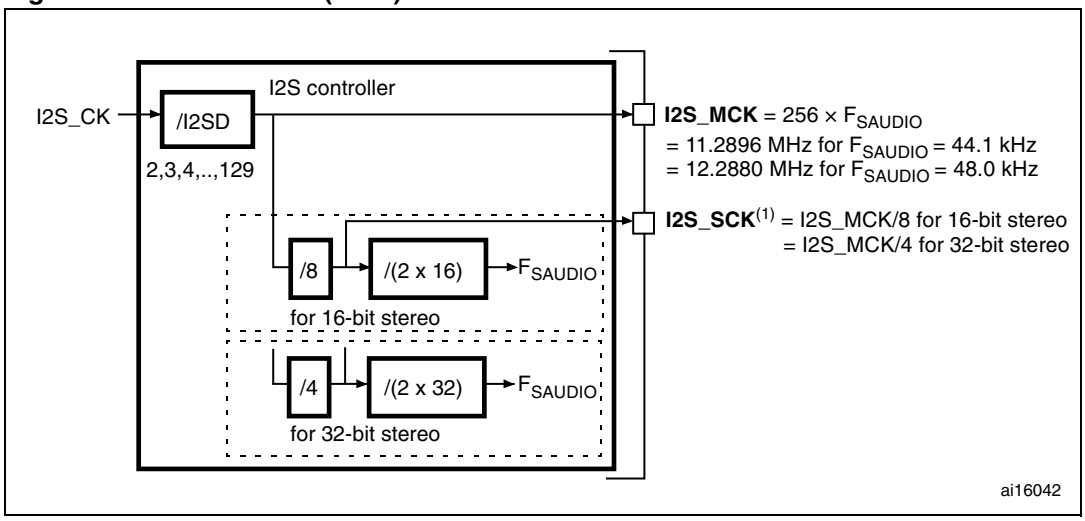
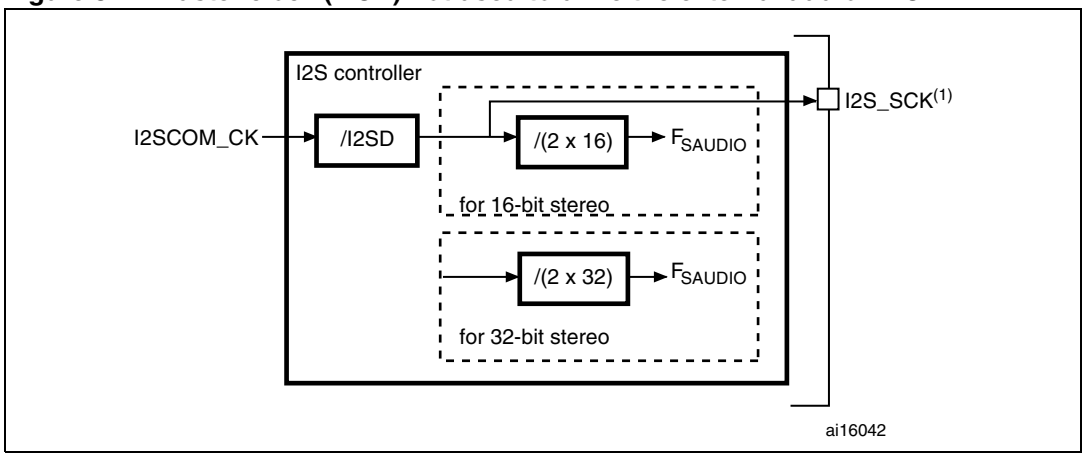


Figure 86. Master clock (MCK) used to drive the external audio DAC



1. I2S_SCK is the I2S serial clock to the external audio DAC (not to be confused with I2S_CK).

Figure 87. Master clock (MCK) not used to drive the external audio DAC



1. I2S_SCK is the I2S serial clock to the external audio DAC (not to be confused with I2S_CK).

Revision history

Table 91. Document revision history

Date	Revision	Changes
15-Sep-2011	1	Initial release.

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