DATA SHEET

TEA6100
FM/IF system and microcomputer-based tuning interface

Product specification
File under Integrated Circuits, IC01

August 1987

Philips Semiconductors

PHILIPS

FM/IF system and microcomputer-based tuning interface

TEA6100

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I²C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz) .

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146); SOT146-1; 1996 August 13.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19,					
	f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18,					
	f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

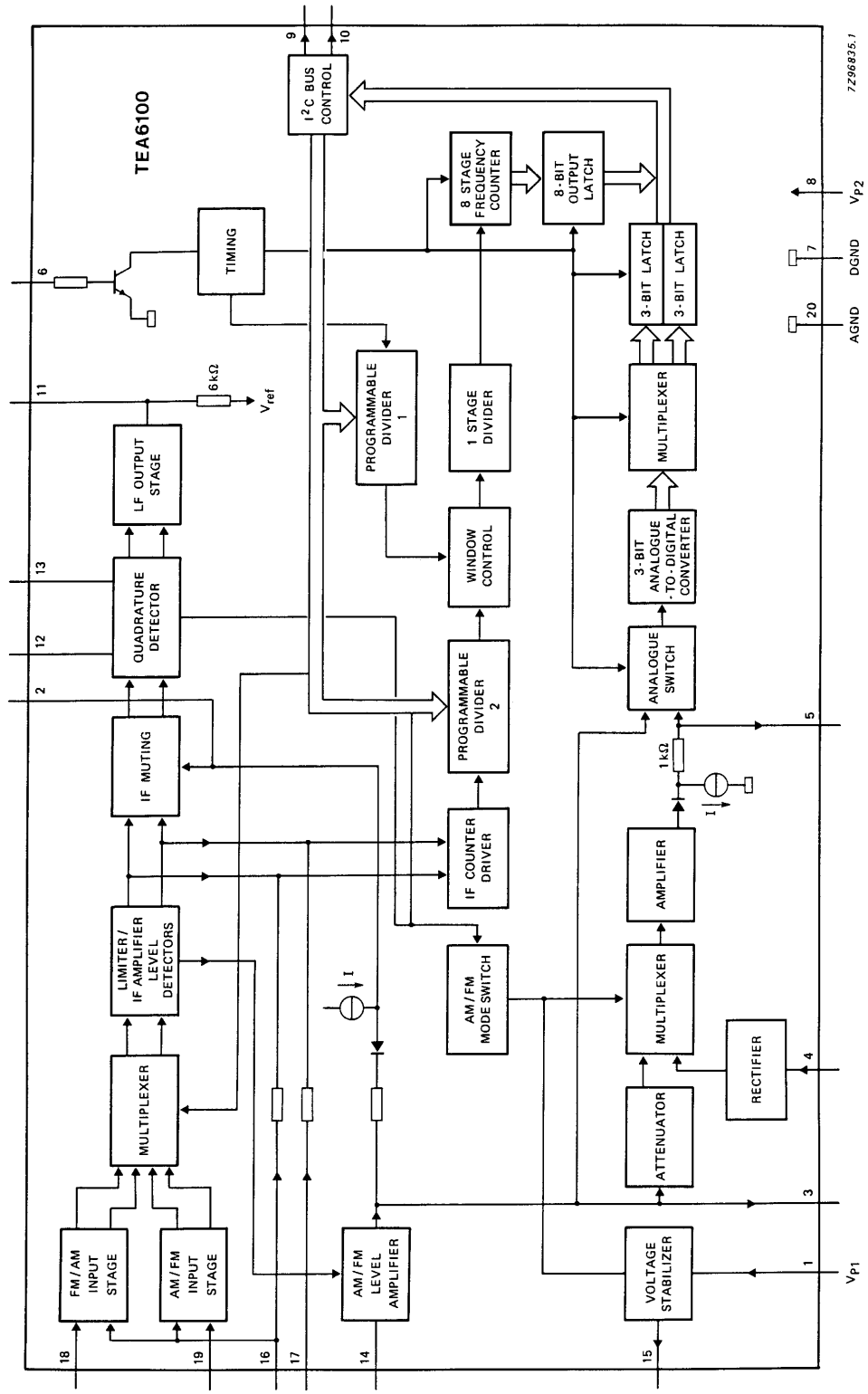


Fig.1 Block diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line; I^2C bus
10	SDA	serial data line; I^2C bus
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

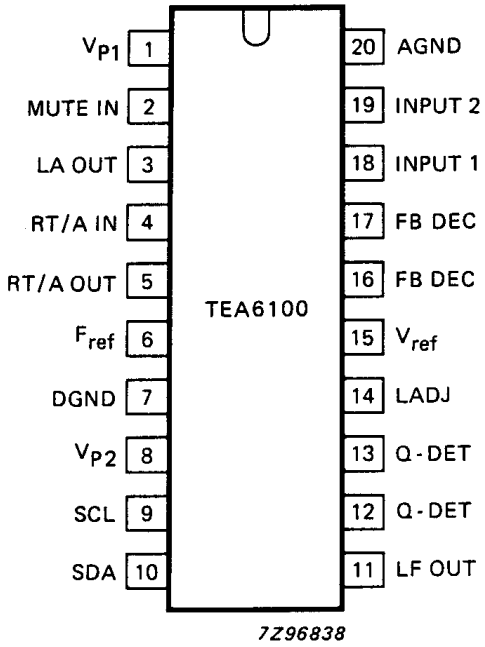


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION (see Figs 1 and 16)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the –3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3- bit words is shown in Table 1.

Table 1 3-bit words

WORD	POSITION	
	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '–3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = $\pm$ counter resolution
- bit 7 = 1, accuracy = $\pm \frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I^2C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

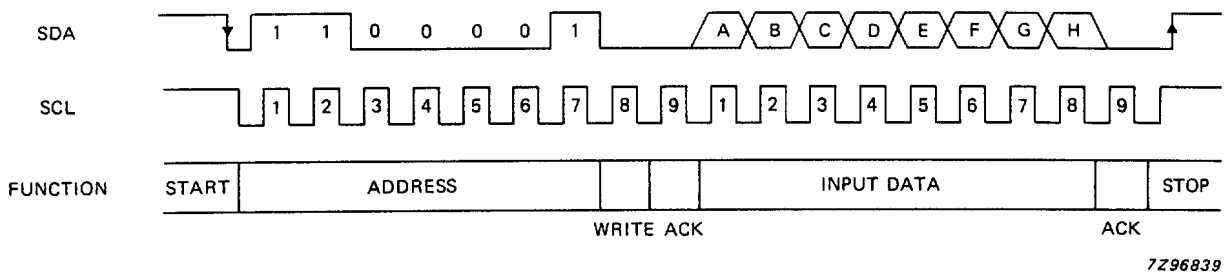


Fig.3 Input data format waveforms.

Table 2 Input bits

BIT	FUNCTION	LOGIC 0	LOGIC 1	**SEE** Fig.5 **AND** 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

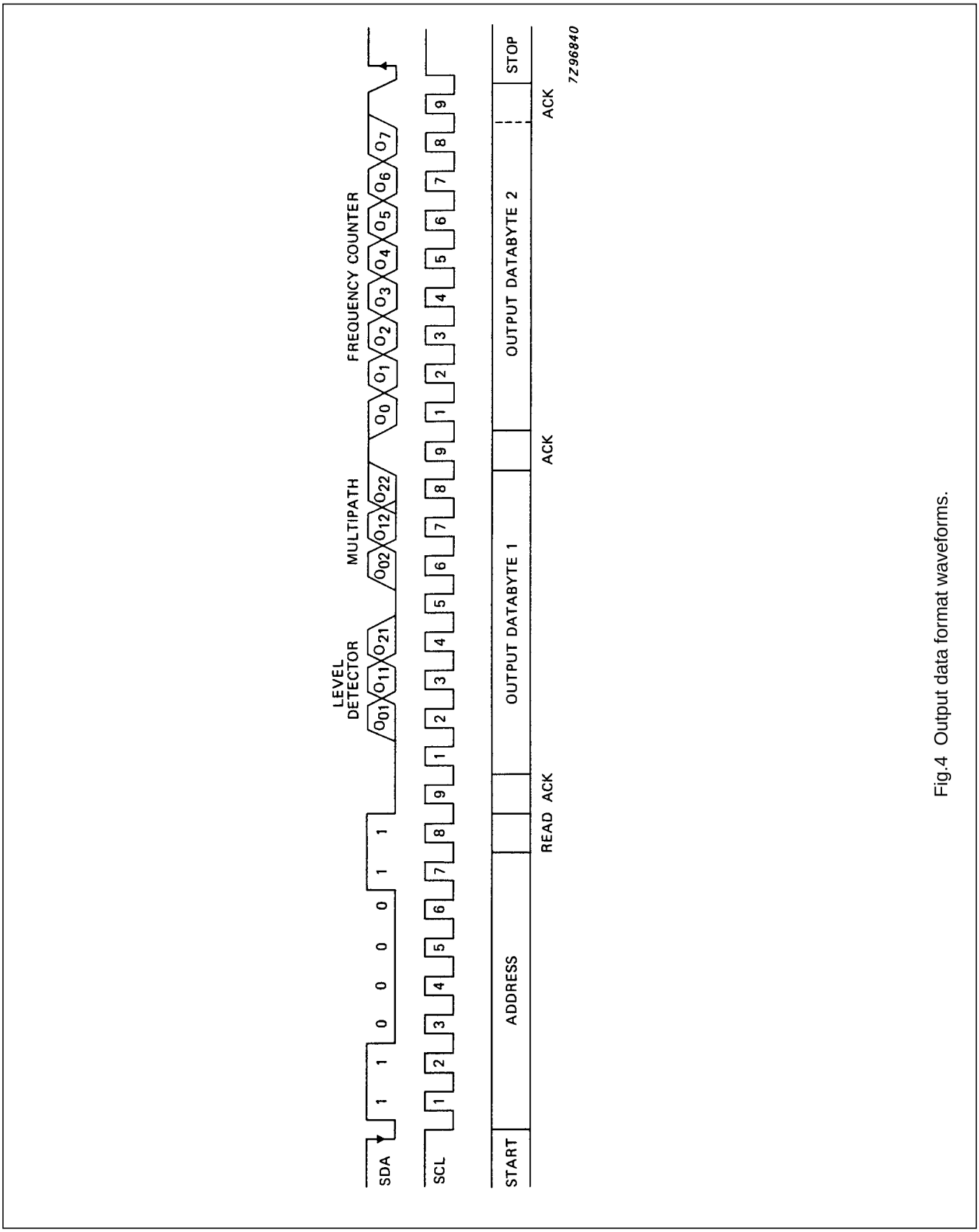


Fig.4 Output data format waveforms.

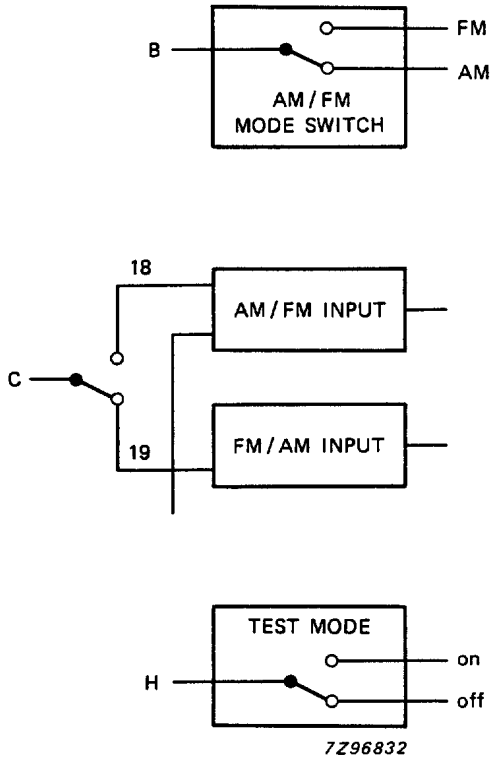


Fig.5 Switch positions, analogue part (switches drawn in logic 0 state).

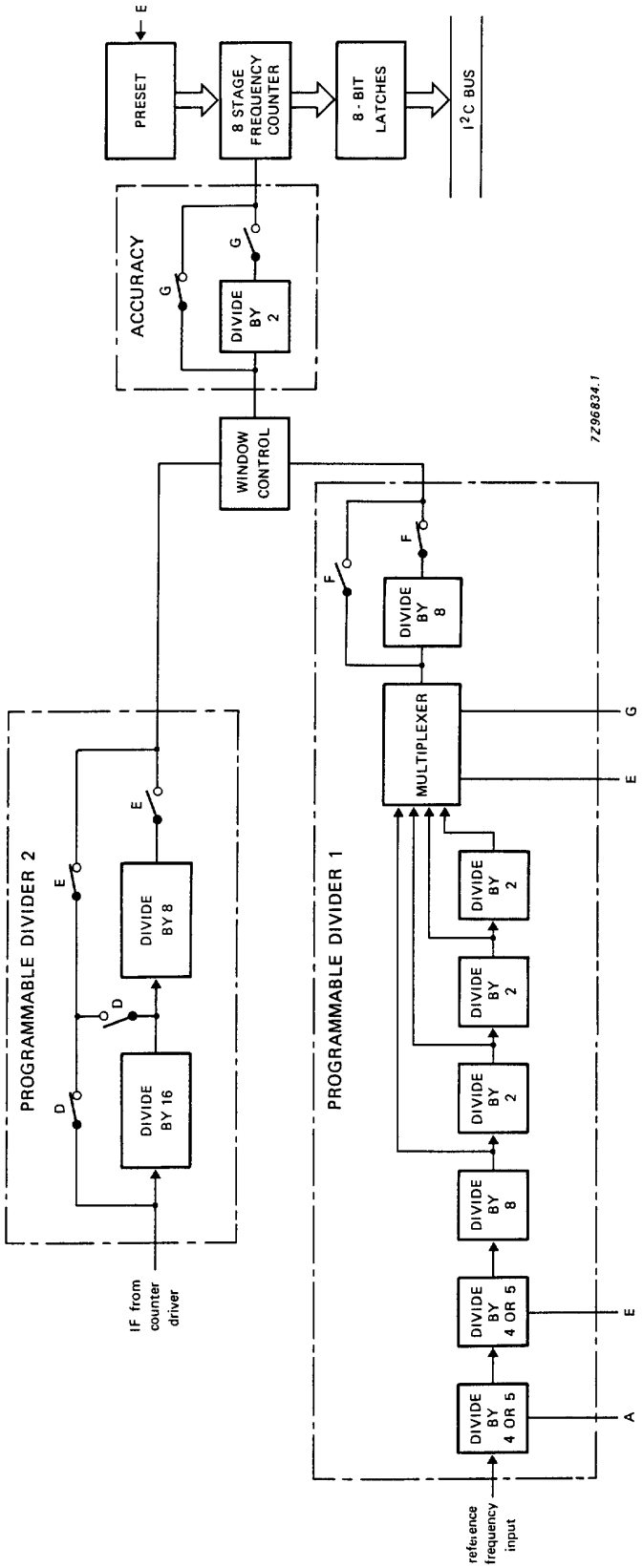


Fig.6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs 5 and 6)

POSITION OF SWITCH ADEFG	WINDOW (ms)	COUNTER RESOLUTION Hz / COUNT	IF FREQUENCY (kHz)	READ OUT BY IF FREQUENCY (HEX)	RANGE (kHz)	
					MIN.	MAX.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig.7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

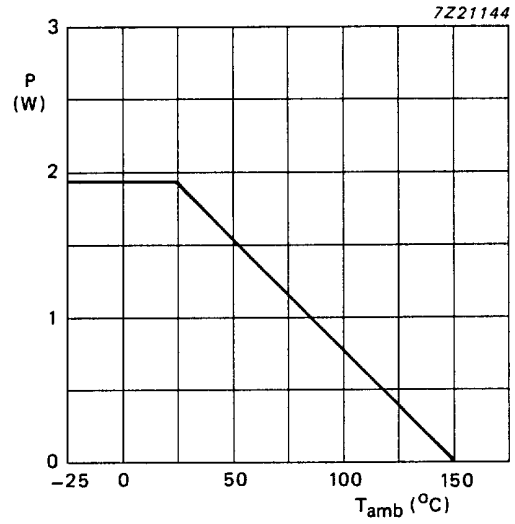


Fig.7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$°C; all currents positive into the IC; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

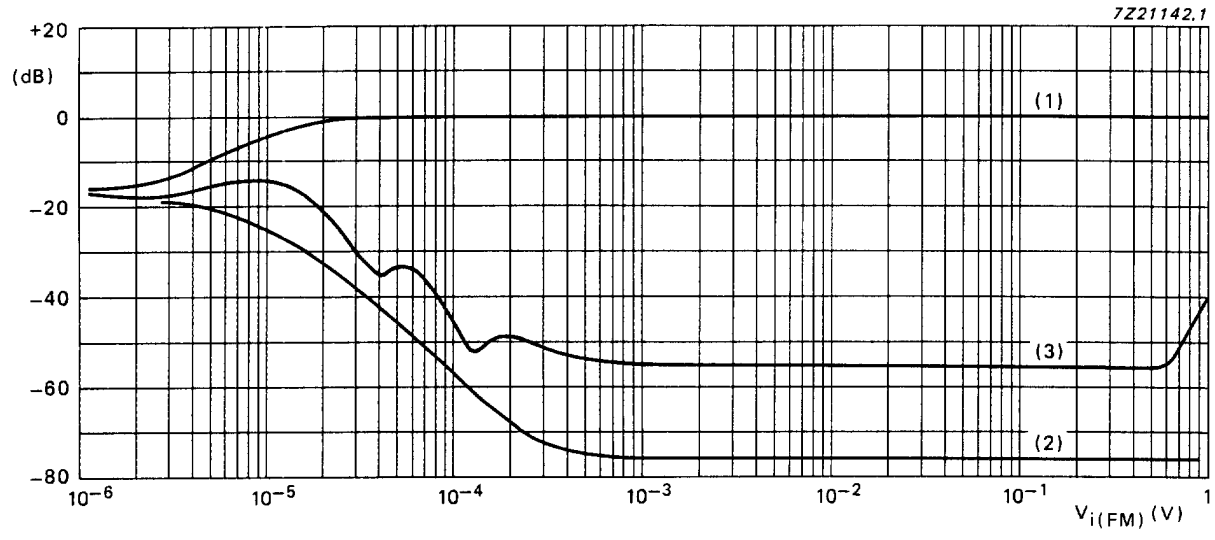
PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwidth = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 db	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Figs 8, 9 and 10; $V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i / V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ±1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
FM level performance	see Fig.11					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec(6)
Output impedance of level amplifier	V_{LFM} > 1 V	$\|Z_o\|$	–	100	–	Ω
AM level performance	see Fig.12					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}$ / V_{ADJ}	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec(6)
IF soft muting	V_{LFM}; pin 3; see Fig.13					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	µA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	µA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain	pins 4 and 5;					
AC to DC	bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig.16; note 3					
Discharge current		I_o	–	200	–	µA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 µV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Figs 14 and 15; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I^2C bus data format	see Fig.3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	µA

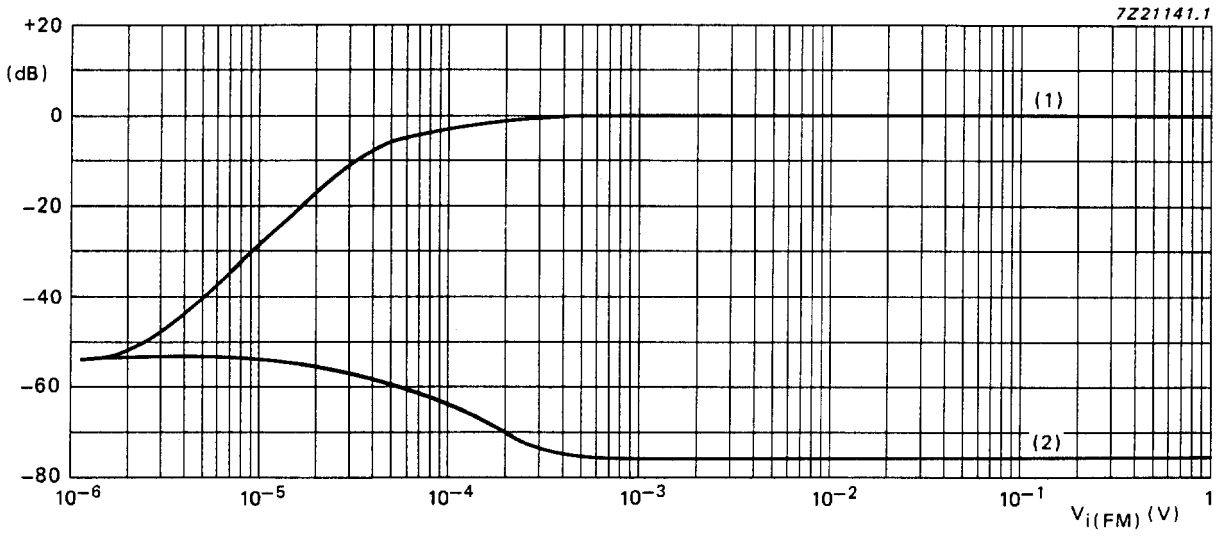
Notes

1. All characteristics are measured from the circuit shown in Fig.16.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL}) / 6 \pm 0{,}07$ V.
6. V/dec = voltage per decade.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig.8 Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig.9 Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

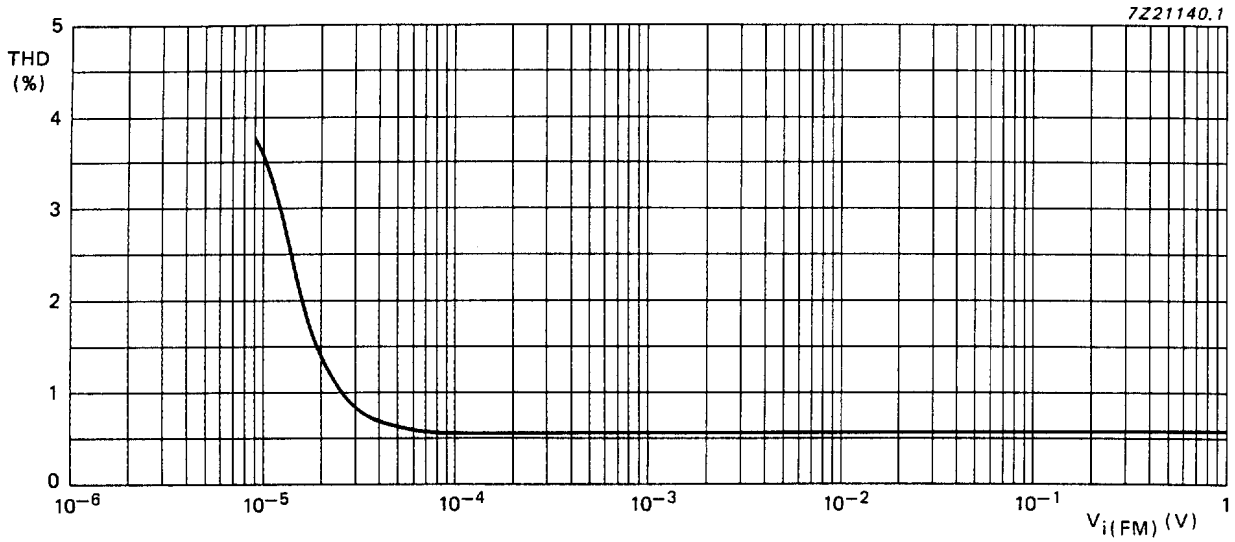
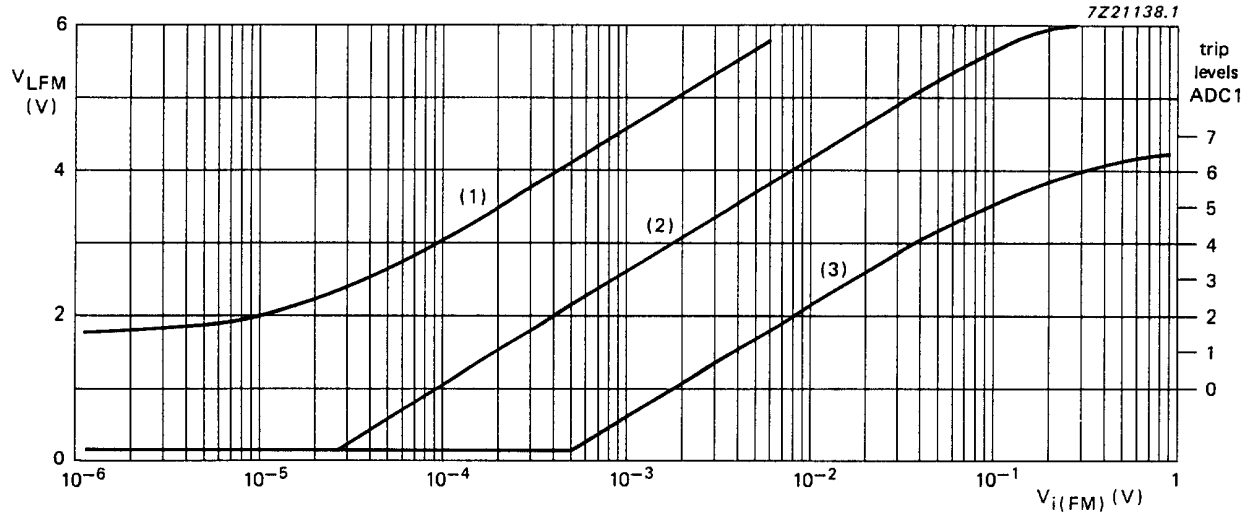
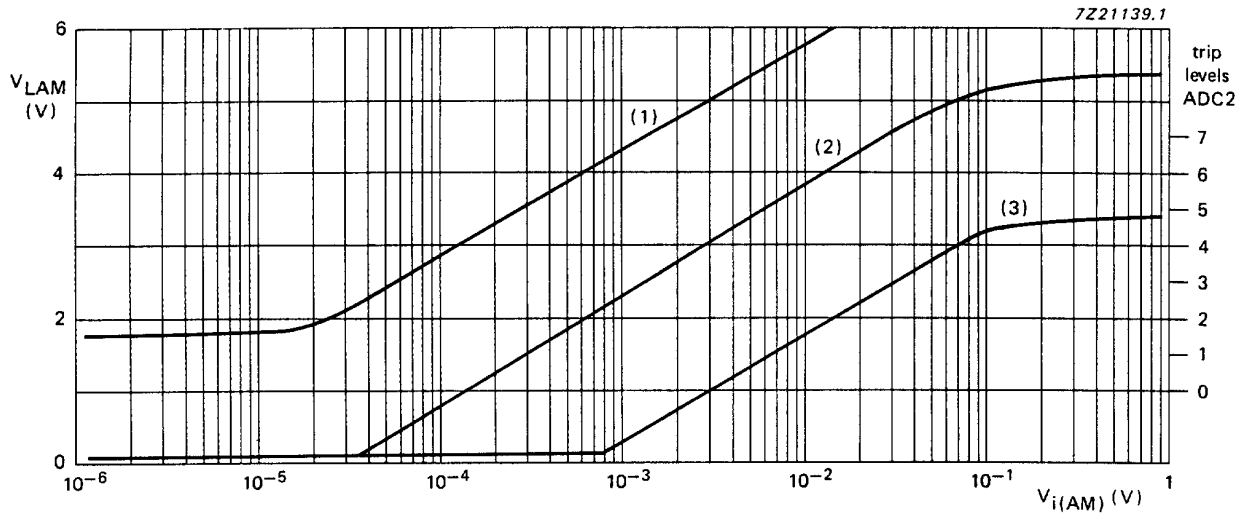


Fig.10 Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = O V.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig.11 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig.12 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

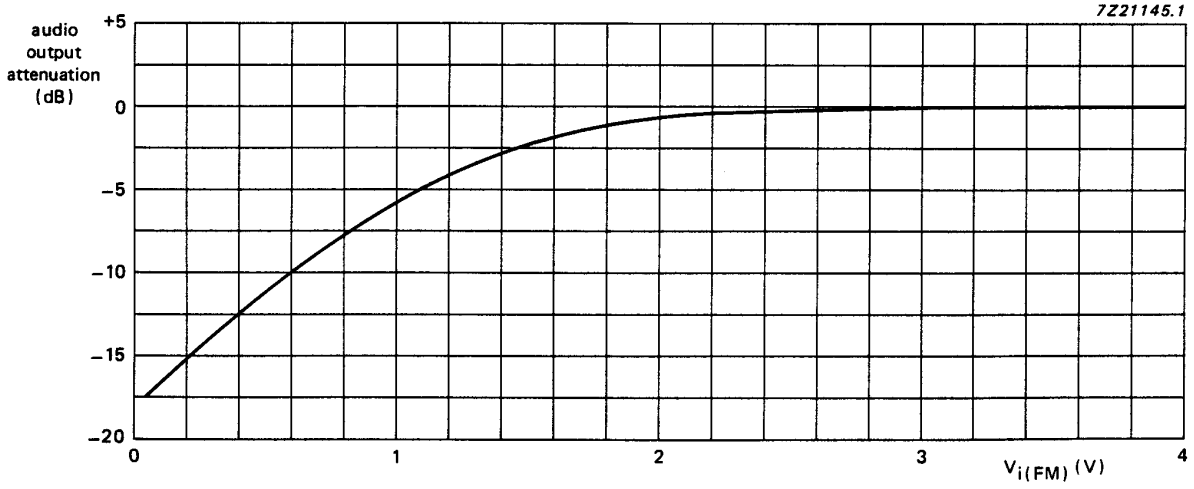
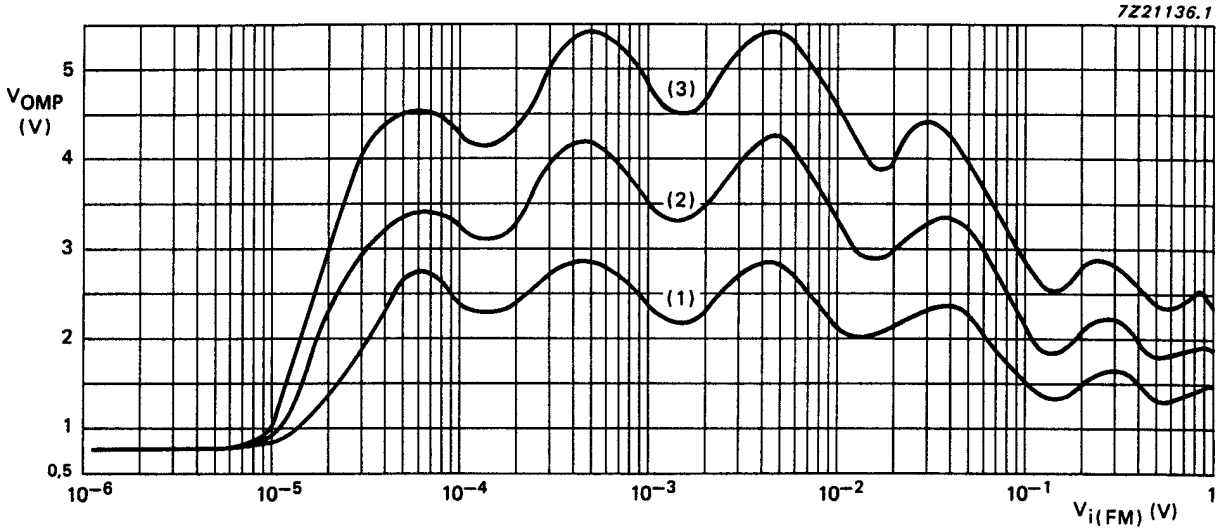
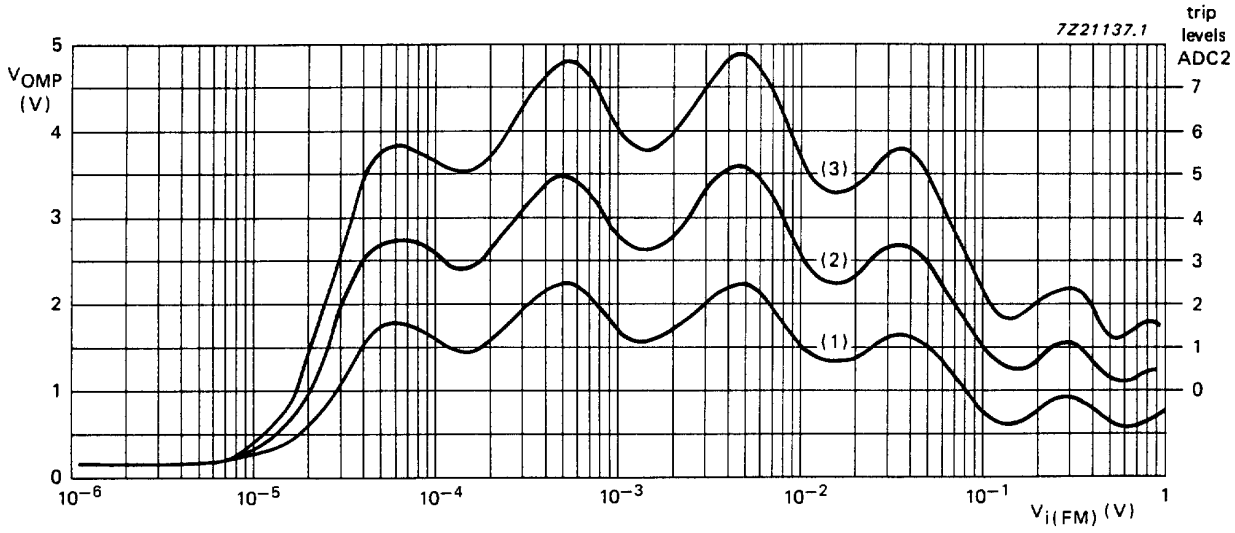


Fig.13 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig.14 Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig.15 Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

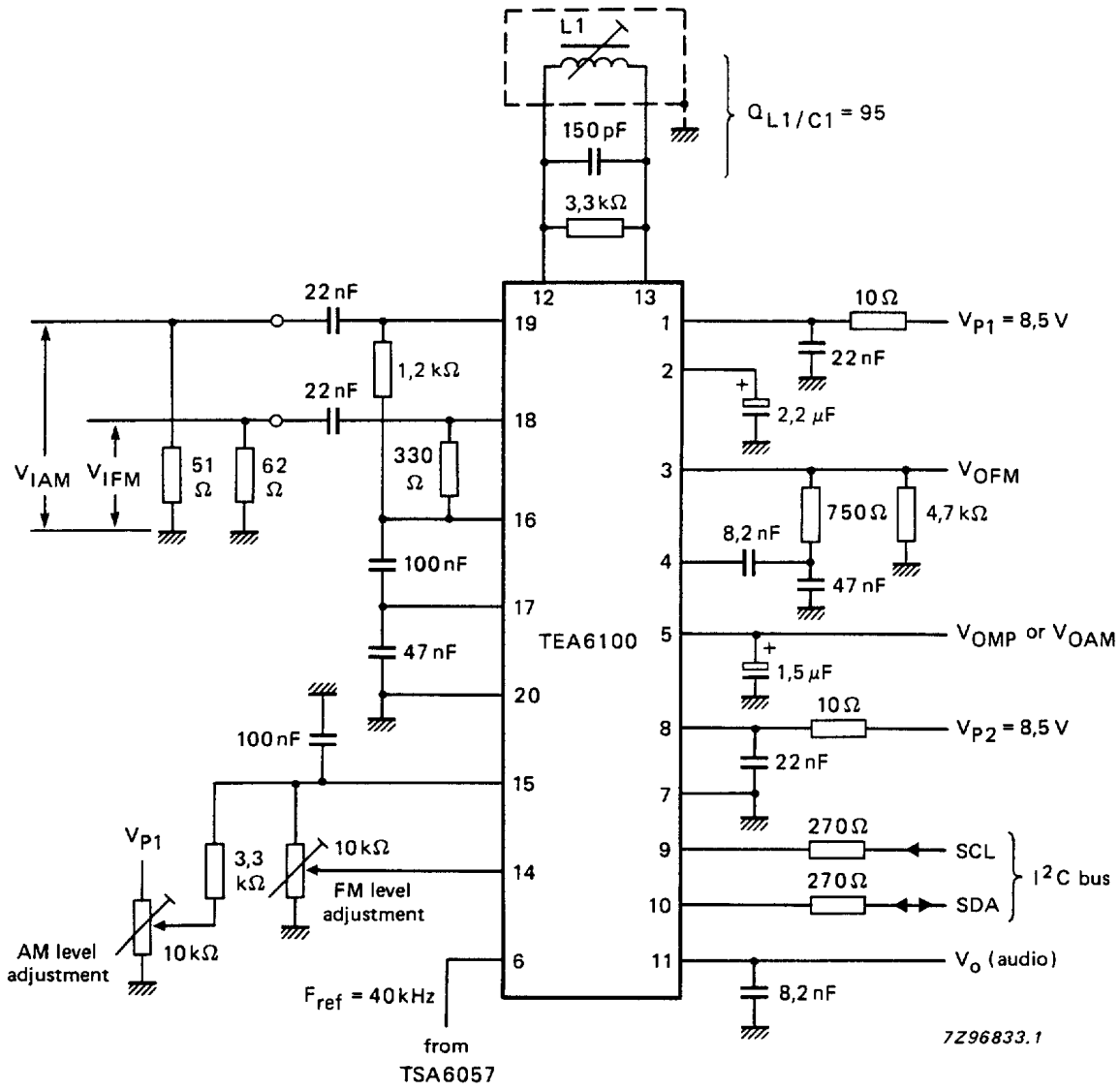


Fig.16 Application diagram.

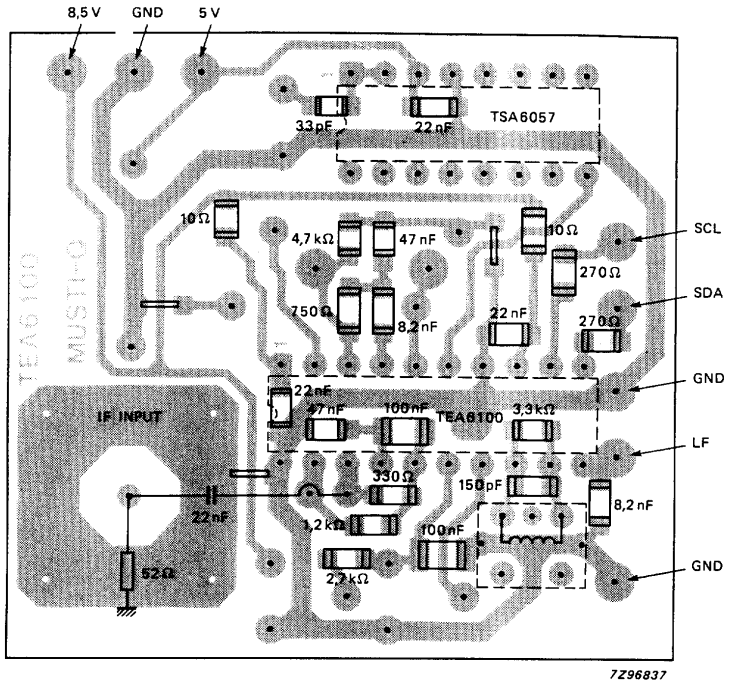


Fig.17 Track side of printed circuit board.

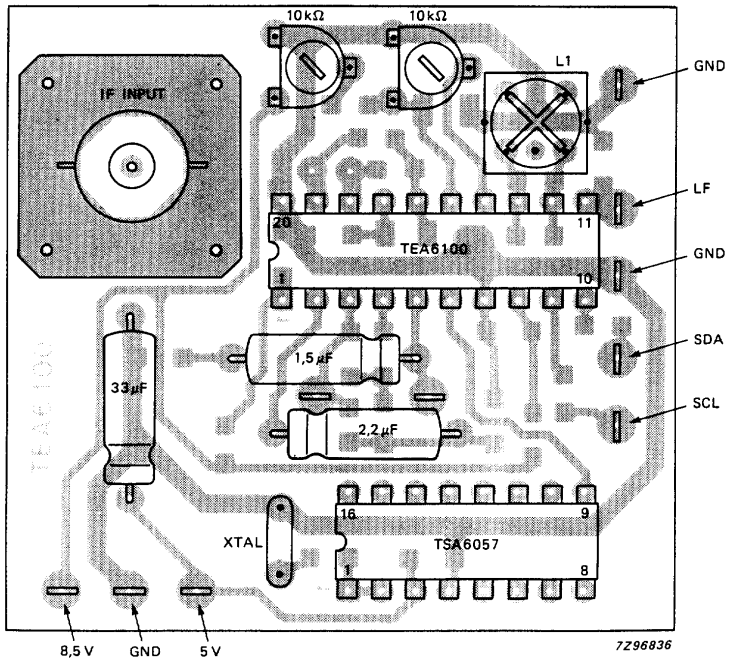
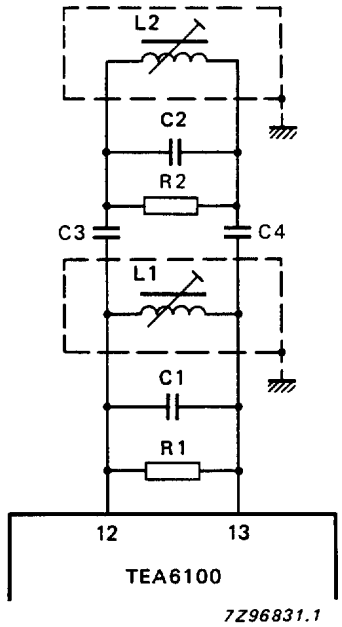


Fig.18 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig.19 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

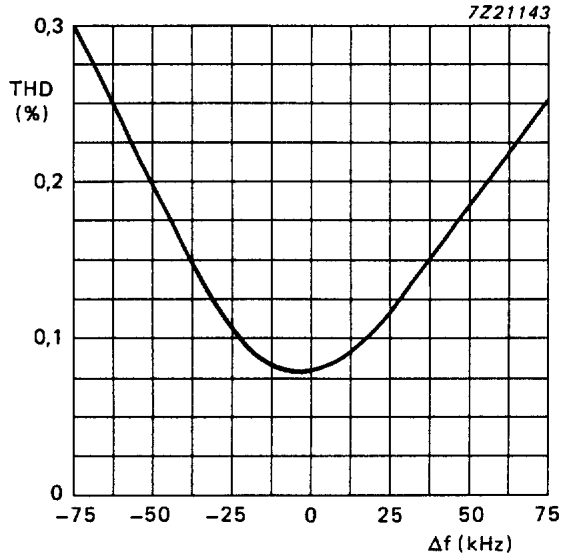


Fig.20 Total harmonic distortion plotted against IF detuning; for $\Delta f = \pm 75$ kHz, $f_{mod} = 1$ kHz and $V_O = 500$ mV.

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

$N1 = (0 \times 4 + 1 \times 5) \times (0 \times 4 + 1 \times 5) \times 8 \times (2^{[1 \times 2 + 0 \times 1]}) \times (1 \times 1 + 0 \times 8) = 800$

T = 800/40 = 20 ms

$N2 = (1 \times 16 \times 8 + 0 \times [1 \times 1 + 0 \times 16]) \times (0 \times 2 + 1 \times 1) = 128$

$TDEC = 20 \times 10{,}7/128 + (1 \times 247 + 0 \times 79) = 1919$

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

R = 128/20 = 6400 Hz/count

Assume the readout is '6E', the measured frequency will be:

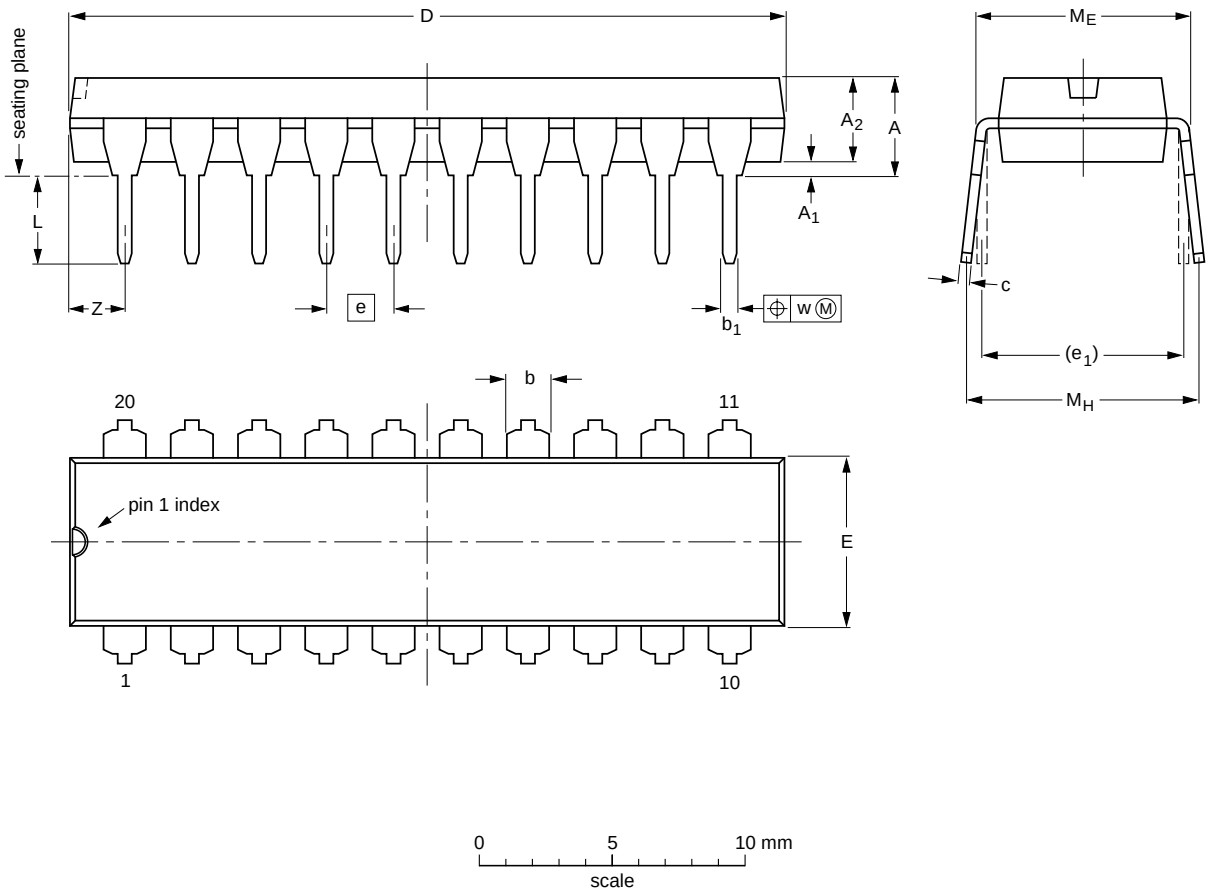
- $F_I = 10{,}7 + (6E - 7F) \times 6400 = 10{,}59$ MHz

Assume the readout is '83', the measured frequency will be:

- $F_I = 10{,}7 + (83 - 7F) \times 6400 = 10{,}726$

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.