TPL5000 Nano Power Programmable Timer with Watchdog Functionality

Check for Samples: TPL5000

FEATURES

- **Supply Voltage from1.8V to 5.0V**
- **Current Consumption 30nA (typ, at 2.5V)**
- **Watchdog Functionality**
- **Reset Functionality**
- **Selectable Timer Intervals 1s to 64s**

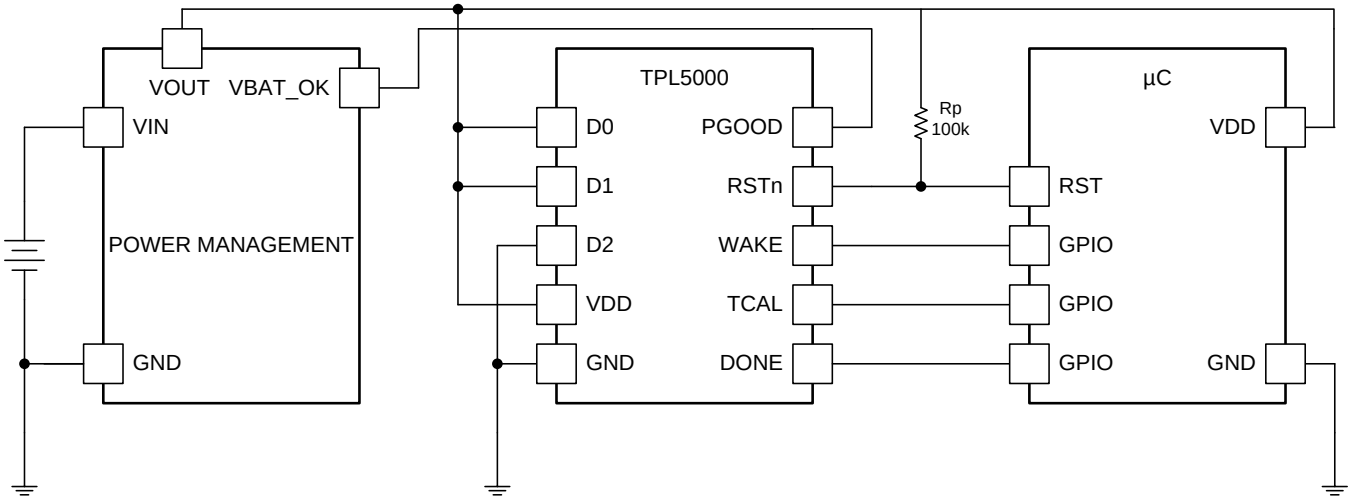
APPLICATIONS

- **Battery powered systems**
- **Energy harvesting systems**
- **Remote data-logger**
- **Sensor node**
- **Building automation**
- **Consumer electronic**
- **Low power wireless**
- **Safety and security platforms**

DESCRIPTION

The TPL5000 is a long-term timer IC optimized for low power applications. The TPL5000 can replace a micro controller's (µC) internal timer, allowing the µC to stay in low power sleep mode instead of running a timer, providing a total power consumption reduction of 60 to 80%. The TPL5000 is designed for use in interrupt-driven applications and provides selectable timing from 1 second to 64 seconds. Some Standards (i.e. EN50271) require implementation of a watchdog function for safety. The TPL5000 realizes this watchdog function without consuming additional power. The TPL5000 can also monitor a battery management IC via a power-good digital input and reset the µC if necessary. The device is packaged in a 10-pin VSSOP package.

Simplified Application Schematic



BLOCK DIAGRAM

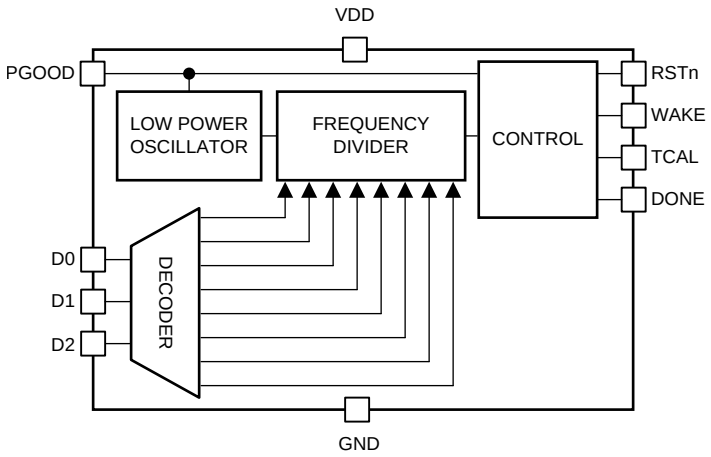


Figure 1. Block Diagram

Table 1. Ordering Information

PACKAGE	PART NUMBER	PACKAGE MARKING	TRANSPORT MEDIA	TI DRAWING
10-pin DGS (VSSOP)	TPL5000DGST	ARAA	250 Units Tape and Reel	DGS0010A
	TPL5000DGSR		3.5k Units Tape and Reel	

PIN FUNCTIONS

Connection Diagram

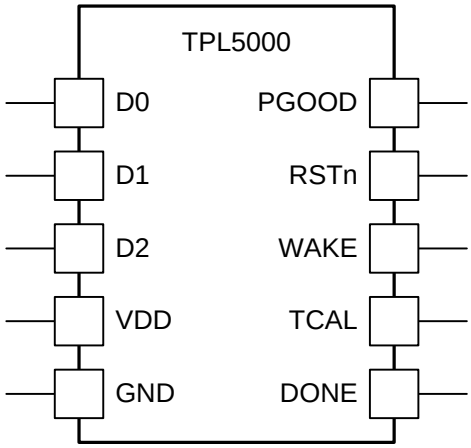


Figure 2. Top View
10-Lead VSSOP

Pin Descriptions

Pin(s)	Name	Description	Application Information
1	D0	Logic Input to set period delay (t_{DP})	Connect to either GND (low logic value) or VDD (high logic value)
2	D1	Logic Input to set period delay (t_{DP})	Connect to either GND (low logic value) or VDD (high logic value)
3	D2	Logic Input to set period delay (t_{DP})	Connect to either GND (low logic value) or VDD (high logic value)
4	VDD	Supply voltage	
5	GND	Ground	
6	DONE	Logic Input for watchdog functionality	
7	TCAL	Short duration pulse output for estimation of TPL5000 timer delay.	
8	WAKE	Timer output signal generated every t_{DP} period.	
9	RSTn	Reset Output (open drain output)	
10	PGOOD	Digital power good input	

Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
Supply Voltage		-0.3	6.0	V
Input Voltage[3]		-0.3	VDD + 0.3	V
Voltage between any two pins			VDD + 0.3	V
Input Current on any pin		-5	+5	mA
Operating Temperature, TA		-40	105	°C
Storage Temperature, T_{stg}		-65	150	°C
Junction Temperature, TJ[4]			150	°C
ESD Rating	Human Body Model[5]		1000	V
	Charged Device Model		250	V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) All voltages referenced to ground unless otherwise noted.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supply (V_{DD}), the current on that pin must not exceed 5mA and must not exceed 6.0V.
(4) The maximum power dissipation is a function of T_J(MAX), θJA, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = (T_J(MAX) - T_A)/ θJA. All numbers apply for packages soldered directly onto a PC board.
(5) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Thermal Characteristics

			UNIT
θ_{JA}	Package thermal impedance[1][2]	196.8	°C/W

(1) The maximum power dissipation is a function of T_J(MAX), θJA, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = (T_J(MAX) - T_A)/ θJA. All numbers apply for packages soldered directly onto a PC board.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.0	V
Temperature Range	-40	105	°C

Electrical Characteristics (1)

Specifications with standard typeface are for $T_A = T_J$ = 25°C, VDD-GND=2.5V, unless otherwise stated.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
POWER SUPPLY						
IVDD	Supply current (4)	PGOOD = VDD		30	50	nA
		PGOOD = GND		12		nA
TIMER						
t_{DP}	Timer Delay Period			1, 2, 4, 8, 10, 16, 32, 64		s
	Timer Delay drift over life time (5)			0.06		%
	Timer Delay drift over temperature			400		ppm/°C
t_{CAL}	Calibration pulse width		14.063	15.625	17.188	ms
	t_{DP} to t_{CAL} matching error (6)	VDD ≤ 3.0V			0.1	%
t_{DONE}	DONE Pulse width (6)		100			ns
t_{RSTn}	RSTn Pulse width			15.625		ms
t_{WAKE}	WAKE Pulse width			31.25		ms
DIGITAL LOGIC LEVELS						
VIH	Logic High Threshold	PGOOD, DONE	0.7xVDD			V
VIL	Logic Low Threshold	PGOOD, DONE			0.3xVDD	V
VOH	Logic output High Level	WAKE, TCAL Iout = 100uA	VDD-0.3			V
		WAKE, TCAL Iout = 1mA	VDD-0.7			V
VOL	Logic output Low Level	WAKE, TCAL Iout = -100uA			0.3	V
		WAKE, TCAL Iout = -1mA			0.7	V
VOL_{RSTn}	RSTn Logic output Low Level	IOL= -1mA			0.3	V
IOH_{RSTn}	RSTn High Level output current	VOH_{RSTn}=VDD		1		nA
TIMING TCAL, RSTn, WAKE, DONE, PGOOD - Refer to Timing Diagram						
tr_{TCAL}	Rise Time TCAL	Capacitive load 15pF		50		ns
$tf_{TCAL,}$	Fall Time TCAL	Capacitive load 15pF		50		ns
$tr_{RSTn,}$	Rise Time RSTn	Capacitive load 15pF, Rpull-up 100Kohm		4		ns
$tf_{RSTn,}$	Fall Time RSTn	Capacitive load 15pF, Rpull-up 100Kohm		50		ns
tr_{WAKE}	Rise Time WAKE	Capacitive load 15pF		50		ns
tf_{WAKE}	Fall Time WAKE	Capacitive load 15pF		50		ns
tD_{DONE}	DONE to RSTn or WAKE delay	Min delay		100		ns
		Max delay		t_{DP}-5*t_{CAL}		ms
tD_{TCAL}	TCAL to RSTn or WAKE delay			t_{CAL}/2		ms

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current doesn't take in account load and pull-up resistor current. Input pins are at GND or VDD.
(5) Operational life time test procedure equivalent to10 years.
(6) Guaranteed by design.

Timing Diagram

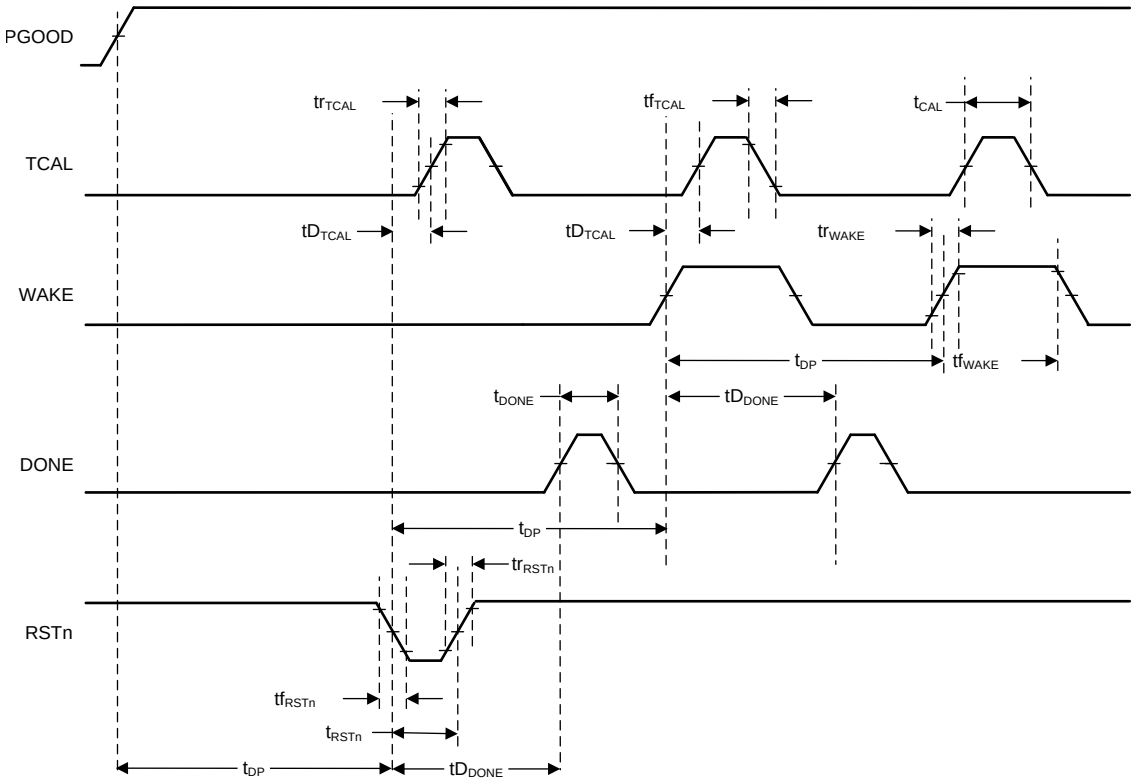
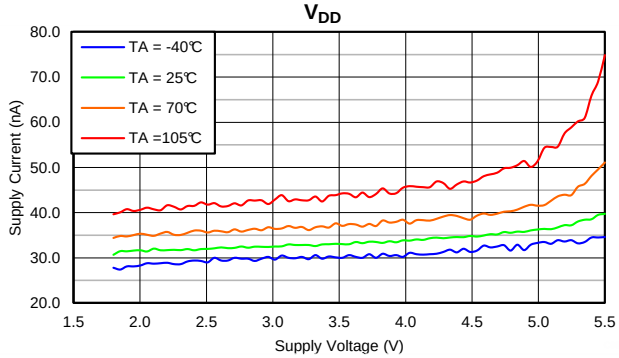


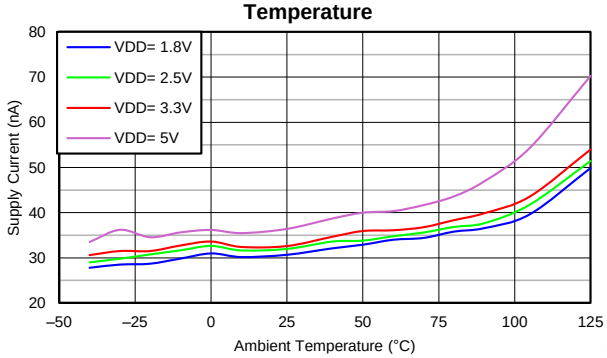
Figure 3. Timing characteristics

Typical Performance Characteristics

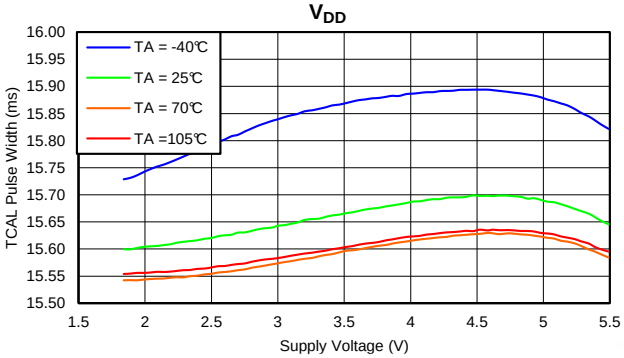
I_{DD} vs V_{DD}



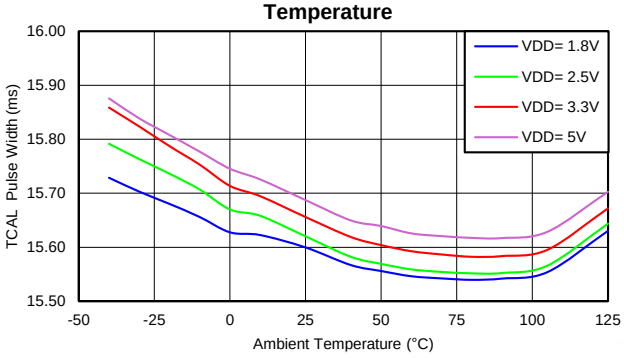
I_{DD} vs Temperature



TCAL Pulse Width vs V_{DD}



TCAL Pulse Width vs Temperature



APPLICATION INFORMATION

The TPL5000 is a long-term timer with a watchdog feature, for low power applications. The TPL5000 is designed for use in interrupt-driven applications and provides selectable timing from 1s to 64s. An additional supervisor feature is achieved through interfacing the TPL5000 to a power management IC.

Configuration and Interface

The time interval between 2 adjacent WAKE pulses (or 2 adjacent RSTn pulses or RSTn and WAKE pulses) is selectable through 3 digital input pins (D0, D1, D2). These pins can be strapped to either VDD (1) or GND (0). Eight possible time delays can be selected, as shown in Table 2.

Table 2. Timer Delay Period

D2	D1	D0	Time (s)	Factor N
0	0	0	1	2^6
0	0	1	2	2^7
0	1	0	4	2^8
0	1	1	8	2^9
1	0	0	10	$10*2^6$
1	0	1	16	2^{10}
1	1	0	32	2^{11}
1	1	1	64	2^{12}

Overview of the Timing Signals: WAKE, RSTn, TCAL and DONE

Figure 4 shows the timing of WAKE, RSTn, and TCAL with respect to DONE. The frame, A, shows a typical sequence after the PGOOD, low to high, transition. As soon as PGOOD is high, the internal oscillator is powered ON. At the end of the delay period (t_{DP}), a reset signal (RSTn), followed by a calibration pulse, TCAL, is sent out. The calibration pulse starts after a half period of the internal oscillator from the falling edge of the reset, and lasts one internal oscillator period.

The frame, B, shows a standard sequence. A "DONE" signal has been received in the previous delay period, so at the end of the next delay period, a "WAKE", followed by a calibration pulse, is sent out. The WAKE signal stays high for 2 internal oscillator periods. The calibration pulse starts after a half period of the internal oscillator from the rising edge of the WAKE signal, and lasts one internal oscillator period. In this frame, the TPL5000 receives a "DONE" signal before the end of the delay period.

The frame, C, still shows a standard sequence, but in this case, the TPL5000 receives the DONE signal when both WAKE and TCAL pulses are still high. As soon as the TPL5000 recognizes the DONE resets the counter and puts WAKE and TCAL in the default condition (both signal low).

The frame, D, shows a typical PGOOD, high to low transition. As soon as PGOOD is low, the internal oscillator is powered OFF and the digital output pins, TCAL, RSTn, and WAKE, are asynchronously reset by the falling edge of the PGOOD signal, such that TCAL and WAKE reset at low logical values, while RSTn resets at a high logical value.

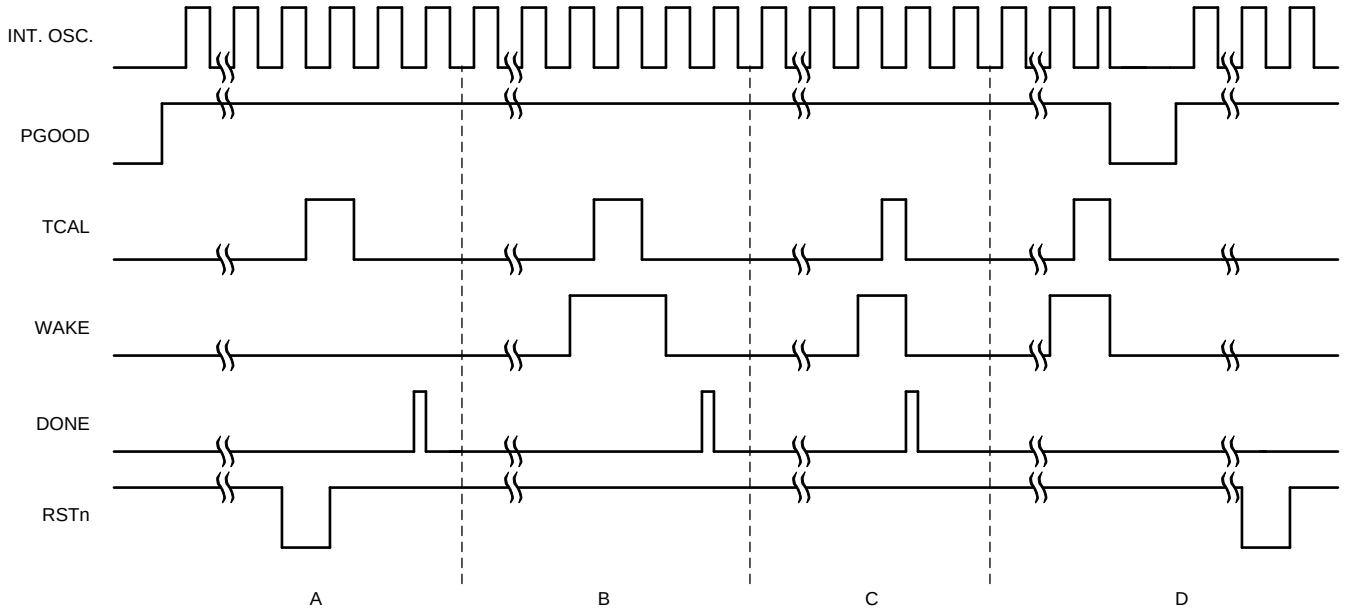


Figure 4. Timing PGOOD, WAKE, RSTn, TCAL

Watchdog Feature

Most of the µC based systems need to be self-reliant; if the software hangs for any reason, the µC must be reset. The TPL5000 can provide this functionality by connecting a µC programmable output pin to the DONE input pin. If the DONE line does not toggle within the selected delay period, then the µC is not operating properly and must be reset.

The TPL5000 recognizes a valid DONE signal as a low to high transition; if two DONE signlas are received within the delay period the second signal is ignored.

In the TPL5000, the watchdog window and the delay period are equivalent. A valid "DONE" signal resets the watchdog counter only, and not the delay time counter. A PGOOD low to high transition clears both the watchdog and delay time counters.

Figure 5 shows the watchdog feature of the TPL5000. The sequence A, B, C is a standard sequence with the µC working properly. In this normal sequence, the µC sends a valid "DONE" (arrow B) before the end of the delay period. The sequence C, D ,E is an anomalous sequence in which the µC is not in a valid state, and it does not send the DONE signal (dashed pulse) before the end of the delay period. The TPL5000 determines the µC is hung and sends a RESET signal (arrow E) when the period delay has elapsed.

Supervisor Feature

A critical event that can corrupt the memory of a µC is a voltage supply drop (supply lower than minimum operating range), and a reset of the µC is mandatory if this occurs. Since the TPL5000 is the right choice in systems which stay most of the time in deep sleep, due to its ultra low power consumption, it is fundamental that it takes into account the voltage drop events.

The TPL5000 implements a supervisory functionality when working with some power management ICs which indicate the status of the supply voltage with a power good or battery good output. The supervisory functionality is enabled by simply connecting the Battery management power good output to the TPL5000 PGOOD pin. If this feature is not used connect the PGOOD pin to VDD.

In case the power management IC detects a voltage drop, lowering the PGOOD line, while the µC is in deep sleep mode (in which internal supervisors are usually off), the TPL5000 internally latches that event, and when the PGOOD returns to high, it sends out a RESET signal to the µC at the end of the elapsed delay period.

Figure 5 shows the supervisor feature of the TPL5000. The sequence F, G is a standard sequence where the µC is in deep sleep and a voltage supply drop occurs (which is highlighted by the PGOOD high to low transition). When PGOOD is high again, a reset pulse at the end of the delay period is sent to the µC (arrow F), then the µC executes its routine (memory has been reloaded upon reset) and sends the "DONE" signal.

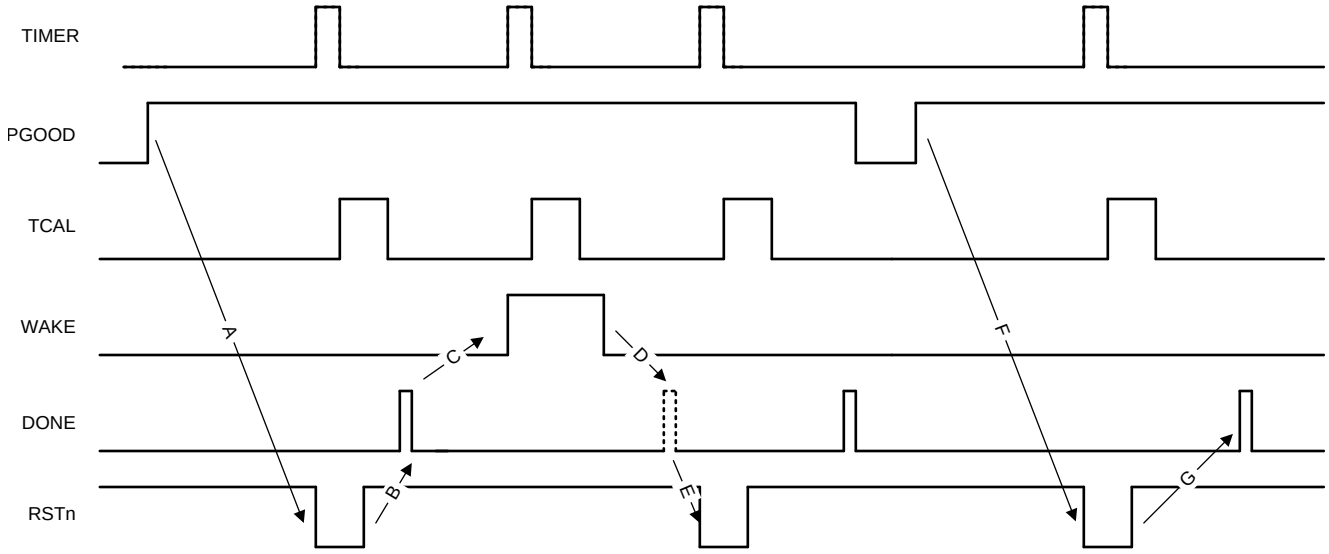


Figure 5. Watchdog and Supervisor Feature

Calibration Pulse

The TPL5000 is based on a ultra-low power oscillator which has a relatively low frequency and low accuracy; however, it shows very good cycle to cycle repeatability and very low temperature drift. In most of the applications, the accuracy of the oscillator is enough, but if a more accurate measure of the delay period is required, it is possible to measure the base period of the internal oscillator. A single pulse, which has the same duration as the base period of the internal oscillator, is present at the TCAL pin of the TPL5000. This pulse starts after a half period of the internal oscillator from either the falling edge of the RESET pulse, or the rising edge of the WAKE pulse.

A µC connected to the TPL5000 can routinely measure the width of the TCAL pulse using a counter and an external crystal. Once the base period of the TPL5000 is measured, the actual time delay is calculated by multiplying the measured period by a factor, N (see Table 2), dependent on the nominal selected time delay.

The resolution and the accuracy of the measurement depend on the external crystal. Since the frequency of the internal oscillator of the TPL5000 is very stable, the measurement of the calibration pulse is suggested only when a high gradient of ambient temperature is observed. The measurement of the TCAL pulse is useful in battery-powered applications that implement a precise battery life counter in the µC.

Different Utilizations of the TPL5000

When either the watchdog or the supervisor feature of the TPL5000 are not required, it is possible to disable them reducing the interconnections between the TPL5000 and the µC.

Connecting the DONE pin either to GND or to TCAL pin disables the watchdog feature. If connected to GND, the TPL5000 only sends a reset pulse when the time delay elapses. If DONE is connected to TCAL, the TPL5000 sends out just one RESET pulse after a PGOOD low to high transition, when the time delay elapses and then WAKE pulses when the successive time delay elapses.

Connecting the PGOOD pin to the supply pin of the TPL5000 disables the supervisor feature.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5000DGSR	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	ARAA	Samples
TPL5000DGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	ARAA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

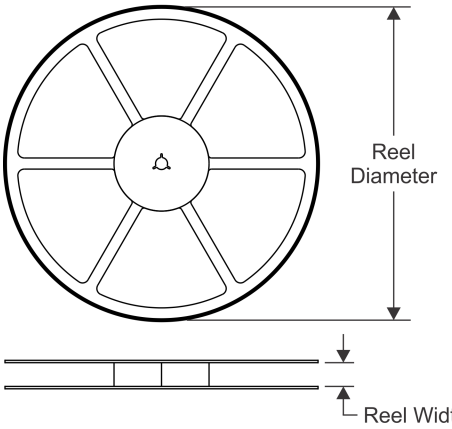
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

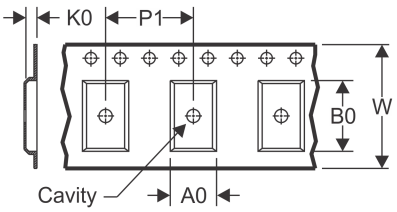
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

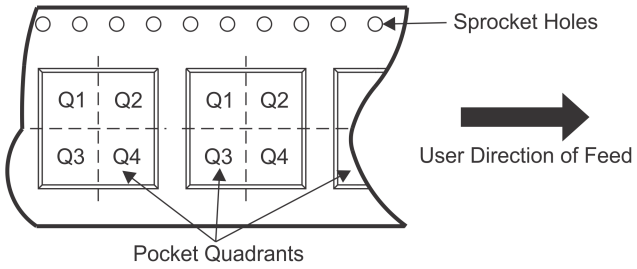


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

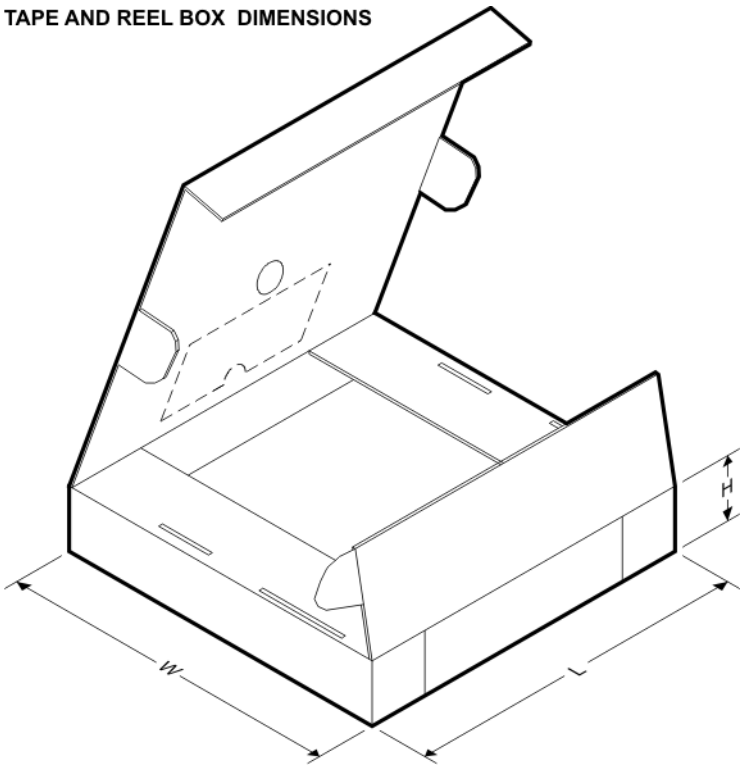
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5000DGSR	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPL5000DGST	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

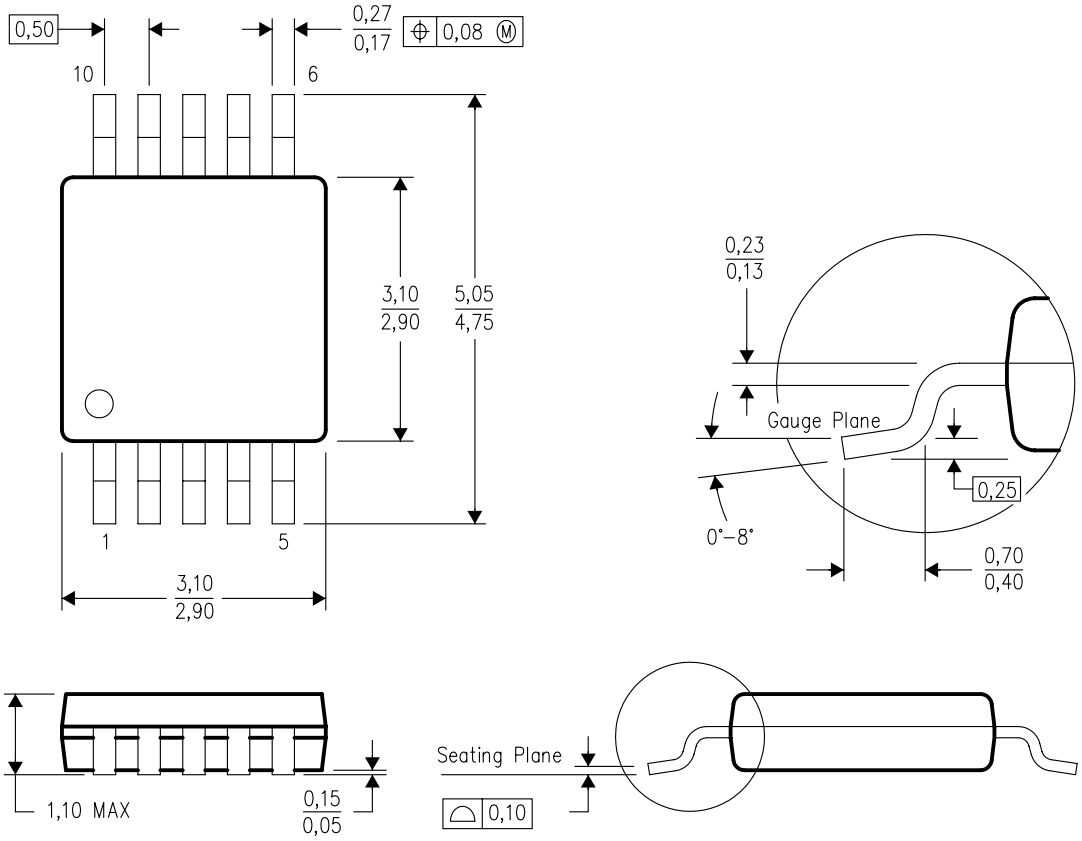
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5000DGSR	VSSOP	DGS	10	3500	367.0	367.0	35.0
TPL5000DGST	VSSOP	DGS	10	250	210.0	185.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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