PRODUCT NOTIFICATION

DEVICE	LITERATURE NO.
TLV320AIC12	SLWS115
TLV320AIC13	SLWS139
TLV320AIC14	SLWS140
TLV320AIC15	SLWS141
TLV320AIC20	SLAS363
TLV320AIC21	SLAS365
TLV320AIC24	SLAS366
TLV320AIC25	SLAS367

Texas Instruments (TI) has recently identified a problem in the product models listed above related to DLL clock-generation. When a clock-generation mode is used that powers up the delay-locked-loop (DLL), the DLL may not startup properly when initiated, resulting in the audio master clock not functioning. This results in the codec in the products not functioning. This issue does not affect applications that do not enable the product's DLL.

Since this issue does not affect operation if the DLL is not enabled, customers are recommended to ensure their system does not enable the product's DLL. The DLL is enabled anytime the *P* value in control register #4 (pertaining to clock generation) is NOT set equal to 8. The DLL is used whenever the part is in *fine* sampling mode, as described in Section 3.1 of the data manual, so the recommended mode to use is the *coarse* sampling mode, which requires P=8.

At present, TI does not have a screening procedure in place to detect product with the DLL issue, but the company also realizes that many customers do not use the DLL in their systems and will be unaffected by this issue.

TI is not confident of the operation of the DLL in this product at this time. To ensure customers have been made aware of this issue, orders for these parts will only be filled upon return of a signed waiver until this issue is resolved. The company has initiated an investigation to fully understand the root cause of this problem and determine what appropriate long-term corrective action should be taken. TI recommends that all customers presently using these parts contact the company immediately, so they can receive updates on this investigation and plans for its resolution.

We apologize for the inconvenience placed upon customers in ordering this product. However, we wish to ensure that our customers are aware of the device shortcomings from the specification. We are working in earnest to remove this waiver requirement.

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TEXAS INSTRUMENTS

TLV320AIC20

Low Power, Highly-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec

Data Manual

May 2002

HPA Data Acquisition

SLAS363A

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1 Introduction

The TLV320AIC20 is a true low-cost low-power highly-integrated high-performance dual voice codec designed with new technological advances. It features two 16-bit analog-to-digital (A/D) channels and two 16-bit digital-to-analog (D/A) channels, which can be connected to a handset, headset, speaker, microphone, or a subscriber line via a programmable analog crosspoint.

The TLV320AIC20 provides high resolution signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology with programmable sampling rate.

The TLV320AIC20 innovation is the smart time division multiplexed serial port (SMARTDM™) that optimizes the DSP performance with its most advanced synchronous synchronous 4-wire serial port in TDM format for glue-free interface to popular DSP (i.e., C5x, C6x) and microcontrollers. The SMARTDM™ supports both continuous data transfer mode and on-the-fly reconfiguration programming mode (both ADC/DAC and control data). The SMARTDM™ maximizes the bandwidth of data transfer (ADC/DAC data only) between the TLV320AIC20 DSPcodec and the DSP. In normal operation, it automatically detects the number of codecs in the serial interface and adjusts the number of time slots to match the number of codecs so that no time slot in the TDM frame is wasted. In the turbo operation, it maintains the same number of time slots but maximizes the bit transferred rate to 25 MHz to allow other serial DSP peripheral devices to share the same serial bus within the same sampling period. The TLV320AIC20 can be gluelessly cascaded to any SMARTDM-based device to form a multichannel codec and up to eight TLV320AIC20 codecs can be cascaded to a single serial port.

The TLV320AIC20 provides a flexible host port. The host port interface is a two-wire serial interface that can be programmed to be either an industrial standard I^2C or a simple S^2C (start-stop communication protocol).

The TLV320AIC20 also integrates all of the critical functions needed for most voice-band applications including MIC preamp, handset amp headset amp, 8-Ω speaker driver, sidetone control, antialiasing filter (AAF), input/output programmable gain amplifier (PGA), and selectable low-pass IIR/FIR filters.

The TLV320AIC20 implements an extensive power management; including device power-down, independent software control for turning off ADC, DAC, op-amps, and IIR/FIR filter (bypassable) to maximize system power conservation. The TLV320AIC20 consumes only 20 mW at 3 V.

The TLV320AIC20's low power operation from 2.7 V to 3.6-V for analog and I/O and 1.65 V to 1.95 V for digital core power supplies, along with extensive power management, make it ideal for portable applications including wireless accessories, hands-free car kits, VOIP, cable modem, and speech processing. Its low group delay characteristic makes it suitable for single or multichannel active control applications.

The TLV320AIC20 is characterized for commercial operation from 0°C to 70°C and industrial operation from –40°C to 85°C.

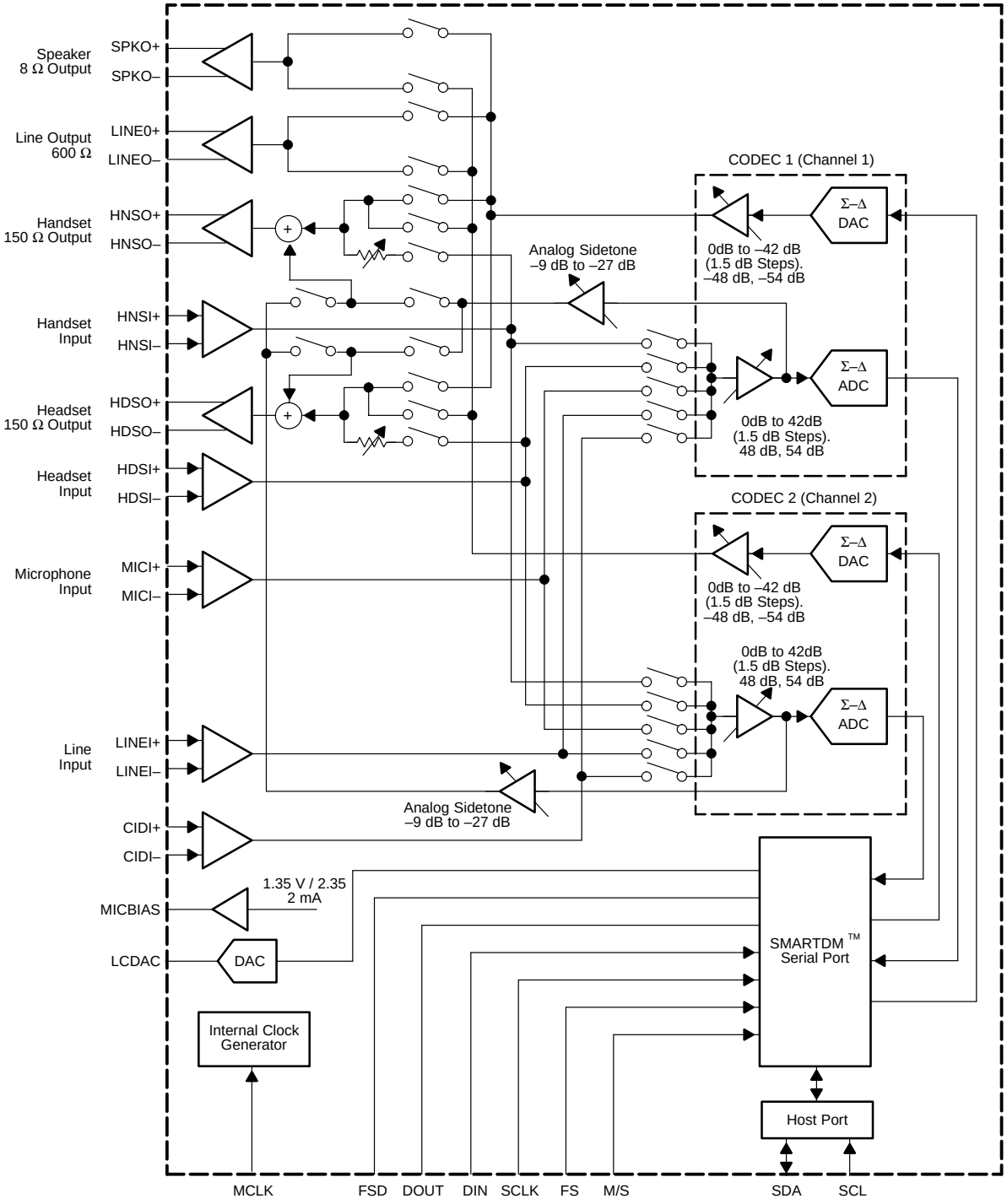
1.1 Features

- C54x Software driver available
- Two 16-bit oversampling sigma-delta A/D converter
- Two 16-bit oversampling sigma-delta D/A converter
- Support maximum master clock of 100 MHz to allow DSPs output clock to be used as master clock
- Selectable FIR/IIR filter with bypassing option
- Programmable sampling rate up to:
  - Max 26 KSPS with on-chip IIR/FIR filter
  - Max 104 KSPS with IIR/FIR bypassed
- On-chip FIR produced 87-dB Dynamic range for ADC and 92 dB for DAC at 8-KSPS sampling rate.
- ADC and DAC filters are G.712 and G.722 compliant

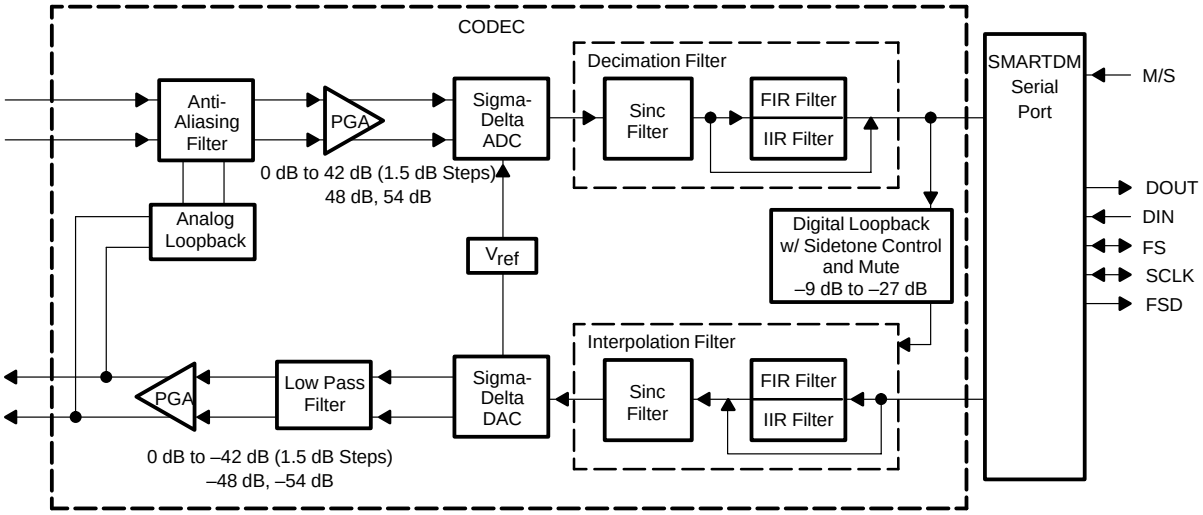
SMARTDM is a trademark of Texas Instruments.

- Smart time division multiplexed serial port (SMARTDM)
  - Glueless 4-wire interface to DSP
  - Automatic cascade detection (ACD) self-generates master/slave device addresses
  - Programming mode to allow on-the-fly reconfiguration (control frame) and ADC/DAC data (data frame) to share the same port
  - Continuous data transfer mode (transfer ADC/DAC data only) to support DSP's DMA/autobuffering mode
  - Turbo mode to maximize bit clock for faster data transfer and allow multiple serial devices to share the same bus
  - Total number of time slots proportional to number of codecs in the cascade to eliminate unused time slots and optimize DSP memory allocation
  - Allows up to 8 AIC20s to be connected to a single serial port
- Host port
  - 2-Wire interface
  - Selectable I^2C or S^2C
- Differential and single-ended analog input and differential output
- Built-in functions:
  - Analog and digital sidetone
  - Antialiasing filter (AAF)
  - Programmable input and output gain control (PGA)
  - Microphone/handset/headset amplifiers
  - 8-Ω speaker driver
  - Power management with hardware/software power-down modes 30 μW
- Separate software control for ADC and DAC power down
- Fully compatible with TI C54x DSP power supplies
  - 1.65-V–1.95-V Digital core power
  - 2.7-V–3.6-V Digital I/O
  - 2.7-V–3.6-V Analog
- Power dissipation (P_D)
  - 20 mW at 3 V in standard operation
  - 30 mW at 3 V with headset/handset drivers
- Internal reference voltage (V_{ref})
- 2s Complement data format
- Test mode which includes digital loopback and analog loopback

1.2 Functional Block Diagram

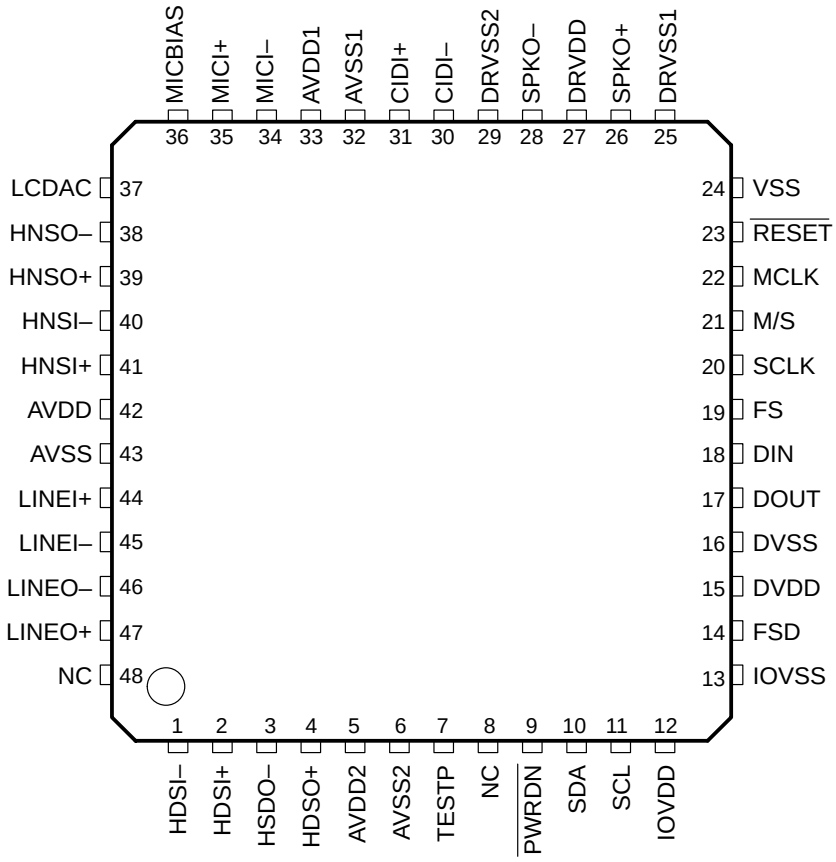


1.3 Functional Block Diagram (One of Two Codecs Shown)



2 Terminal Descriptions

PFB
TOP VIEW



2.1 Ordering Information

T_A	48-TQFP PFB PACKAGE
0°C to 70°C	TLV320AIC20C
–40°C to 85°C	TLV320AIC20I

2.2 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AVDD	42	I	Analog supply
AVDD1	33	I	Analog supply
AVDD2	5	I	Analog power supply
AVSS	43	I	Analog ground
AVSS1	32	I	Analog ground
AVSS2	6	I	Analog ground
CIDI– CIDI+	30 31	I	Caller-ID input
DRVDD	27	I	Driver supply
DRVSS1	25	I	Driver ground
DRVSS2	29	I	Driver ground
DVDD	15	I	Digital supply (1.8 V)
DVSS	16	I	Digital ground
DOUT	17	O	Data OUT
DIN	18	I	Data IN
FS	19	I/O	Frame sync
FSD	14	O	Frame sync delayed
HDSI– HDSI+	1 2	I	Head-set input
HNSI– HNSI+	40 41	I	Hand-set input
IOVDD	12	I	I/O power supply
IOVSS	13	I	I/O ground
LCDAC	37	O	6-Bit DAC output may be used to drive LCDAC
LINEI+ LINEI–	44 45	I	Line input
MCLK	22	I	Master clock
M/S	21	I	Master slave select applied to CODEC1 only. CODEC2 is always a slave.
MICBIAS	36	I	Microphone bias
MICI–	34	I	Microphone input
MICI+	35	I	Microphone input
NC	8, 48		Not connected
SPKO– SPKO+	28 26	O	8-Ω output
HDSO– HDSO+	3 4	O	150-Ω output
HNSO– HNSO+	38 39	O	150-Ω output
LINEO– LINEO+	46 47	O	600-Ω output
$\overline{\text{PWRDN}}$	9	I	Power down
$\overline{\text{RESET}}$	23	I	Reset
SCL	11	I	I^2C/S^2C clock
SCLK	20	I/O	Serial clock
SDA	10	I/O	I^2C/S^2C data
TESTP	7	I	Test pin. Should be connected to digital ground.
VSS	24	I	Device ground

2.3 Definitions and Terminology

Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks, and the data transfer is initiated by the falling edge of the FS signal.
Signal Data	This refers to the input signal and all of the converted representations through the ADC channel and the signal through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
Frame Sync	Frame sync refers only to the falling edge of the signal FS that initiates the data transfer interval
Frame Sync and Sampling Period	Frame sync and sampling period is the time between falling edges of successive FS signals.
f_S	The sampling frequency
ADC Channel	ADC channel refers to all signal processing circuits between the analog input and the digital conversion result at DOUT.
DAC channel	DAC channel refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Dxx	Bit position in the primary data word (xx is the bit number)
DSxx	Bit position in the secondary data word (xx is the bit number)
d	The alpha character d represents valid programmed or default data in the control register format (see Section 3.2, Secondary Serial Communication) when discussing other data bit portions of the register.
PGA	Programmable gain amplifier
IIR	Infinite impulse response
FIR	Finite impulse response

3 Functional Description

3.1 Operating Frequencies (see Notes)

The sampling frequency is the frequency of the frame sync (FS) signal whose falling edge starts digital-data transfer for both ADC and DAC. The sampling frequency is derived from the master clock (MCLK) input by the following equations:

- Coarse sampling frequency (default):

  The coarse sampling is selected by programming P = 8 in the control register 4, which is the default configuration of AIC20 on power-up or reset.

  FS = Sampling (conversion) frequency = MCLK / (16 × M × N × 8)

- Fine sampling frequency (see Note 5):

  FS = Sampling (conversion) frequency = MCLK/ (16 × M × N × P)

NOTES:
1. Use control register 4 to set the following values of M, N, and P
2. M = 1,2, . . . ,128
3. N = 1,2, . . . ,16
4. P = 1,2, . . . ,8
5. The fine sampling rate needs an on-chip Delay Lock Loop (frequency multiplier) to generate internal clocks. The DLL requires the relationship between MCLK and P to meet the following condition: 10 MHz ≤ (MCLK/P) ≤ 25 MHz
6. Both equations of FS require that the following conditions should be met:
   • (M × N × P) ≥ (devnum × mode) if the FIR/IIR filter is not bypassed.
   • [Integer(M/4) × N × P] ≥ (devnum × mode) if the FIR/IIR filter is bypassed.
   where
   devnum is the number of codec channels connecting in cascade (devnum = 2 for standalone AIC20)
   mode is equal to 1 for continuous data transfer mode and 2 for programming mode
   EXAMPLE:
   The MCLK comes from the DSP C5402's CLKOUT and equals to 20.48 MHz and the conversion rate of 8 kHz is desired. First, set P = 1 to satisfy the condition 5 so that (MCLK/P) = 20.48 MHz/1 = 20.48 MHz. Next, pick M = 10 and N = 16 to satisfy condition65 and derive 8 kHz for FS. That is,

   FS = 20.48 MHz/ (16 × 10 × 16 × 1) = 8 kHz

3.2 Internal Architecture

3.2.1 Antialiasing Filter

The built-in antialiasing filter is a two-pole filter that has a 20-dB attenuation at 1 MHz.

3.2.2 Sigma-Delta ADC

The sigma-delta analog-to-digital converter is a sigma-delta modulator with 128-x oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques. Due to the oversampling employed, only single pole R-C filters are required on the analog inputs.

3.2.3 Decimation Filter

The decimation filters are either FIR filters or IIR filters selected by bit D5 of the control register 1. The FIR filter provides linear-phase output with $17/f_S$ group delay, whereas the IIR filter generates nonlinear phase output with negligible group delay. The decimation filters reduce the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:128. The output of the decimation filter is a 16-bit 2s-complement data word clocking at the sample rate selected for that particular data channel. The BW of the filter is (0.45 × FS) and scales linearly with the sample rate.

3.2.4 Sigma-Delta DAC

The sigma-delta digital-to-analog converter is a sigma-delta modulator with 128-x oversampling. The DAC provides high-resolution, low-noise performance using oversampling techniques. The oversampling ratio (OSR) in DAC is programmable to 256/512 using bits D0–D1 of register 3C, the default being 128. The OSR of 512 is recommended when the FS is a maximum of 8 KSPS, and an OSR of 256 is recommended when the FS is a maximum of 16 KSPS.

3.2.5 Interpolation Filter

The interpolation filters are either FIR filters or IIR filters selected by bit D5 of the control register 1. The FIR filter provides linear-phase output with $18/f_S$ group delay, whereas the IIR filter generates nonlinear phase output with negligible group delay. The interpolation filter resamples the digital data at a rate of 128 times the incoming sample rate. The high-speed data output from the interpolation filter is then used in the sigma-delta DAC. The BW of the filter is ($0.45 \times$ FS) and scales linearly with the sample rate.

3.2.6 Analog/Digital Loopback

The analog and digital loopbacks provide a means of testing the data ADC/DAC channels and can be used for in-circuit system level tests. The analog loopback always has the priority to route the DAC low pass filter output into the analog input where it is then converted by the ADC to a digital word. The digital loopback routes the ADC output to the DAC input on the device. Analog loopback is enabled by writing a 1 to bit D2 in the control register 1. Digital loopback is enabled by writing a 1 to bit D1 in control register 1.

3.2.7 Analog Sidetone

The analog sidetone attenuates the analog input and mixes it with the output of the DAC. The control register 5C selects the attenuation level of the analog sidetone.

3.2.8 Digital Sidetone

The digital sidetone attenuates the ADC output and mixes it with the input of the DAC. The control register 5C selects the attenuation level of the digital sidetone.

3.3 Analog Input/Output

To produce excellent common-mode rejection of unwanted signal performance, the analog signal is processed differentially until it is converted to digital data. The signal source driving the analog inputs should have low source impedance for lowest noise performance and accuracy. To obtain maximum dynamic range, the signal must be ac coupled to the input terminal. The analog output is differential from the digital-to-analog converter.

3.3.1 Analog Crosspoint

The analog crosspoint is a lossless analog switch matrix controlled via the serial control port. It allows any source device to be connected to any sink device. Additionally, special summing connections with adjustable loss (7×3 dB steps) are included to implement sidetone for the headset and handset ports. (Also included is muting function on any of the sink devices). The control of the analog crosspoint, defined in the control register 6, is to allow any analog input or output to connect to a codec at one time. If more than one input is selected, these inputs are mixed together before the conversion. Caution needs to be taken to make sure that both DAC channels are not connected to the same output.

3.3.2 Analog Input Amplifier

The integrated programmable gain amplifier (PGA) controls the amplification of any analog input before the analog-to-digital converter converts the signal. The PGA's gain from 0 dB to 42 dB in 1.5-dB steps and 48 dB and 54 dB are selected using the control register 5A.

3.3.3 Microphone Bias

To operate electret microphones properly, a bias voltage and current are provided. Typically, the current drawn by the microphone is in the order of 100 μA to 800 μA and the bias voltage is specified across the microphone at 1.35 V or 2.35 V. The MICBIAS has good power supply noise rejection in the audio band and the bias voltage is selectable, via the serial control bus, for each interface.

3.3.4 Handset and Headset Drivers

The HSNO and HDSO are output from two audio amplifiers to drive low-voltage speakers like those in the handset and headset. They can drive a load of 150 Ω. The drive amplifier is differential to minimize noise and EMC immunity problems. The frequency response is flat up to 26 kHz.

3.3.5 Speaker Driver

The SPKO is output from the audio amplifier that can drive an 8-Ω speaker load. The drive amplifier is differential to minimize noise and EMC immunity problems. The frequency response is flat up to 26 kHz.

3.4 IIR/FIR Control

3.4.1 Overflow Flags

The decimation IIR/FIR filter sets an overflow flag (bit D7) of control register 1 indicating that the input analog signal has exceeded the range of internal decimation filter calculations. The interpolation IIR/FIR filter sets an overflow flag (bit D4) of control register 1 indicating that the digital input has exceeded the range of internal interpolation filter calculations. When the IIR/FIR overflow flag is set in the register, it remains set until the user reads the register. Reading this value resets the overflow flag. These flags need to be reset after power up by reading the register. If FIR/IIR overflow occurs, the input signal should be attenuated by either the PGA or some other method.

3.4.2 IIR/FIR Bypass Mode

An option is provided to bypass IIR/FIR filter sections of the decimation filter and the interpolation filter. This mode is selected through bit D6 of control register 2 and effectively increases the frequency of the FS signal to four times normal output rate of the IIR/FIR-filter. For example, for a normal sampling rate of 8 Ksps (i.e., FS = 8 kHz) with IIR/FIR, if the IIR/FIR is bypassed, the frequency of FS is readjusted to 4×8 kHz = 32 kHz. The sync filters of the two paths can not be bypassed. A maximum of eight devices in cascade can be supported in the IIR/FIR bypass mode.

In this mode , the ADC channel outputs data which has been decimated only till 4Fs. Similarly DAC channel input needs to be preinterpolated to 4Fs before being given to the device. This mode allows users the flexibility to implement their own filter in DSP for decimation and interpolation. M should be a multiple of 4 during IIR/FIR bypass mode.

3.5 System Reset and Power Management

3.5.1 Software and Hardware Reset

The TLV320AIC20 resets internal counters and registers in response to either of two events:

- A low-going reset pulse is applied to terminal RESET
- A 1 is written to the programmable software reset bits (D3 of control register 3A)

NOTE: The TLV320AIC20 requires a power-up reset applied to the RESET pin.

Either event resets the control registers and clears all sequential circuits in the device. The H/W RESET (active low) signal is at least 6 master clock periods long. As soon as the RESET input is applied, the TLV320AIC20 enters the initialization cycle that lasts for 132 MCLKs, during which the DSPs serial port is put in 3-state. For a cascaded system the rise time of H/W RESET must be less than the MCLK period and should satisfy setup time requirement of 2 ns with respect to MCLK rise-edge. In stand-alone-slave mode SCLK must be running during reset. RESET must be synchronized with MCLK in all cases.

3.5.2 Power Management

Most of the device (all except the digital interface) enters the power-down mode when D5 and D4, in control register 3A, are set to 1. When the $\overline{\text{PWRDN}}$ pin is low, the entire device is powered down. In either case, register contents are preserved and the output of the amplifier is held at midpoint voltage to minimize pops and clicks.

The amount of power drawn during software power down is higher than during a hardware power down because of the current required to keep the digital interface active. Additional differences between software and hardware power-down modes are detailed in the following paragraphs.

3.5.2.1 Software Power-Down

Data bits D5 and D4 of control register 3A are used by TLV320AIC20 to turn on or off the software power-down mode, which takes effect in the next frame FS. The ADC and DAC can be powered down individually. In the software power-down, the digital interface circuit is still active while the internal ADC and DAC channel and all differential analog outputs are disabled, and DOUT is put in 3-state in the data frame only. Register data in the control frame is still accepted via DIN, but data in the data frame is ignored. The device returns to normal operation when D7 and D6 of control register 3A are reset.

3.5.2.2 Hardware Power-Down

The TLV320AIC20 requires the $\overline{\text{PWRDN}}$ signal to be synchronized with MCLK. When $\overline{\text{PWRDN}}$ is held low, the device enters hardware power-down mode. In this state, the internal clock control circuit and the differential outputs are disabled. All other digital I/Os are disabled and DIN can not accept any data input. The device can only be returned to normal operation by holding $\overline{\text{PWRDN}}$ high. When not holding the device in the hardware power-down mode, $\overline{\text{PWRDN}}$ must be tied high.

3.6 Digital Interface

3.6.1 Clock Source (MCLK, SCLK)

MCLK is the external master clock input. The clock circuit generates and distributes necessary clocks throughout the device. SCLK is the bit clock used to receive and transmit data synchronously. When the device is in the master mode, SCLK and FS are output and derived from MCLK in order to provide clocking the serial communications between the device and a digital signal processor (DSP). When in the slave mode, SCLK and FS are inputs. SCLK is controlled by TURBO bit (D7) in control register 2. In the standard operation (non-turbo, TURBO = 0), SCLK frequency is defined by:

$$\text{SCLK} = (16 \times \text{FS} \times \#\text{Devices} \times \text{mode})$$

Where:

FS is the frame-sync frequency.
#Device is the number of the codec channels in cascade. (#Device = 2 for stand-alone AIC20)
Mode is equal to 1 for continuous data transfer mode and 2 for programming mode.

3.6.2 Serial Data Out (DOUT)

DOUT is placed in the high-impedance state after transmission of the LSB is completed. In data frame, the data word is the ADC conversion result. In the control frame, the data is the register read results when requested by the read/write (R/W) bit. If a register read is not requested, the low eight bits of the secondary word are all zeroes. Valid data on DOUT is taken from the high-impedance state by the falling edge of frame-sync (FS). The first bit transmitted on the falling edge of FS is the MSB of valid data.

3.6.3 Serial Data In (DIN)

The data format of DIN is the same as that of DOUT, in which MSB is received first on the falling edge of first SCLK after FS. In a data frame, the data word is the input digital signal to the DAC channel. If (15+1)-bit data format is used, the LSB (D0) of every DAC channel is set to 1 to switch from the continuous data transfer mode to the programming mode. In a control frame, the data is the control and configuration data that sets the device for a particular function as described in Section 3.9, Control Register Programming.

3.6.4 Frame-Sync FS

The frame-sync signal (FS) indicates the device is ready to send and receive data. FS is an output if the M/S pin is connected to HI (master mode) and an input if the M/S pin is connected to LO (slave mode).

Data is valid on the falling edge of the FS signal.

The frequency of FS is defined as the sampling rate of the TLV320AIC20 and derived from the master clock MCLK as followed (see Section 3.1 Operating Frequencies for details):

$$FS = MCLK / (16 \times P \times N \times M)$$

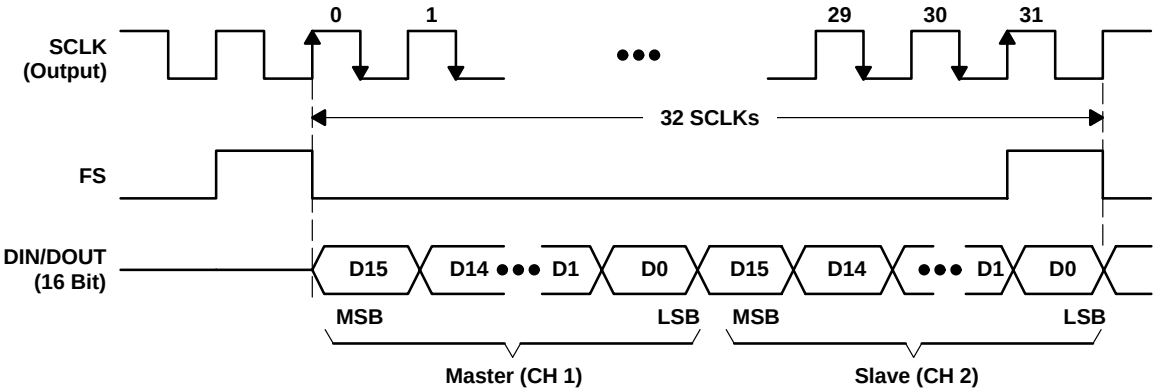


Figure 3–1. Timing Diagram for FS in the Continuous Transfer Mode

3.6.5 Cascade Mode and Frame-Sync Delayed (FSD)

In cascade mode, the DSP receives all frame-sync pulses from the master though the master's FS. The master's FSD is output to the first slave and the first slave's FSD is output to the second slave device and so on. Figure 3–2 shows the cascade of four TLV320AIC20s in which the closest one to DSP is the master and the rest are slaves. The FSD output of each device is input to the FS terminal of the succeeding device. Figure 3–3 shows the FSD timing sequence in the cascade.

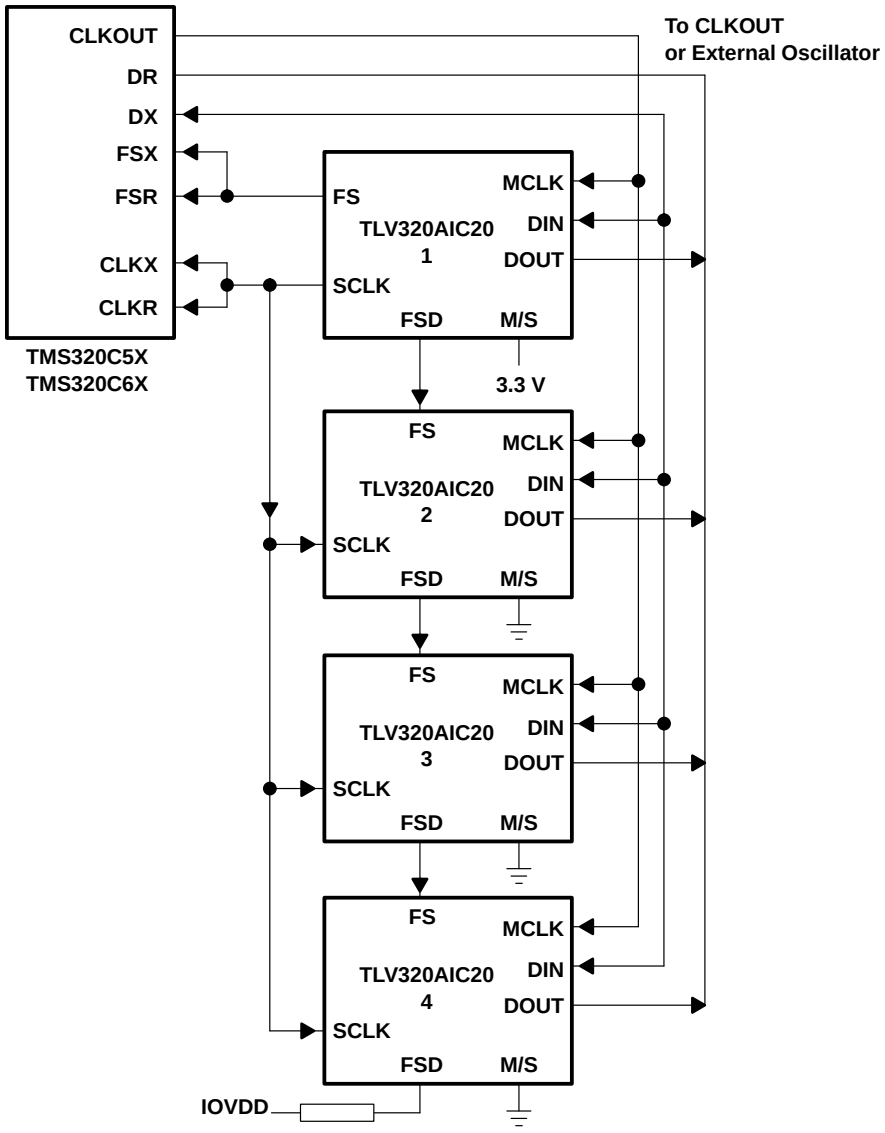


Figure 3–2. Cascade Connection (to DSP Interface)

3.6.6 Stand-Alone Slave

In the stand-alone slave connection, the FS and SCLK inputs must be synchronized to each other and programmed according to Section 3.1 (Operating Frequencies). The FS and SCLK input are not required to synchronize to the MCLK input but must remain active at all times to assure continuous sampling in the data converter. FSD must be connected to LOW for stand-alone-slave. FS is output for initial 132 MCLK and it is kept low. DSP needs to keep FS low or high-impedance state for this period to avoid contention on FS.

3.6.7 Asynchronous Sampling (Codecs in cascade are sampled at different sampling frequency)

The AIC20's SMARTDM support different sampling frequency between the different channels in cascade connecting to a single to serial port in which all codecs is sampled at the same frequency of FS as followed. For example: fs1 and fs2 are desired sampling rates for CH1 and CH2 respectively:

1. FS = MCLK/(16xMxNxP)

2. FS = n1 x fs1 (n1 = 1,2, . . ., 8 defined in the control register 3A of CH1)
3. FS = n2 x fs2 (n2 = 1,2, . . .,8 defined in the control register 3A of CH2)

For validating the conversion data from this operation:

For DAC: DSP need to give same data for n1 samples. CH1 picks one of n1 samples.

For ADC: CH1 gives same data for n1 samples. DSP should pick one of n1 samples.

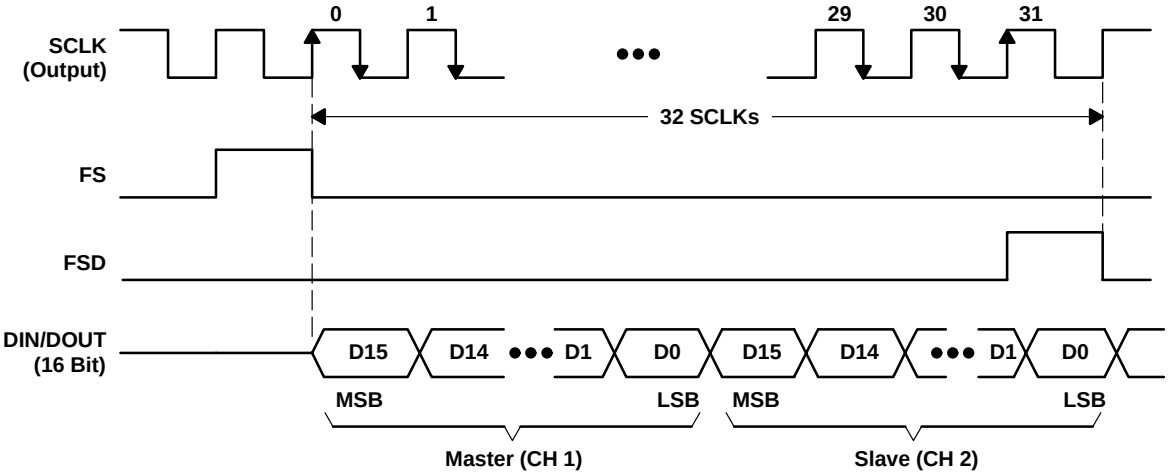
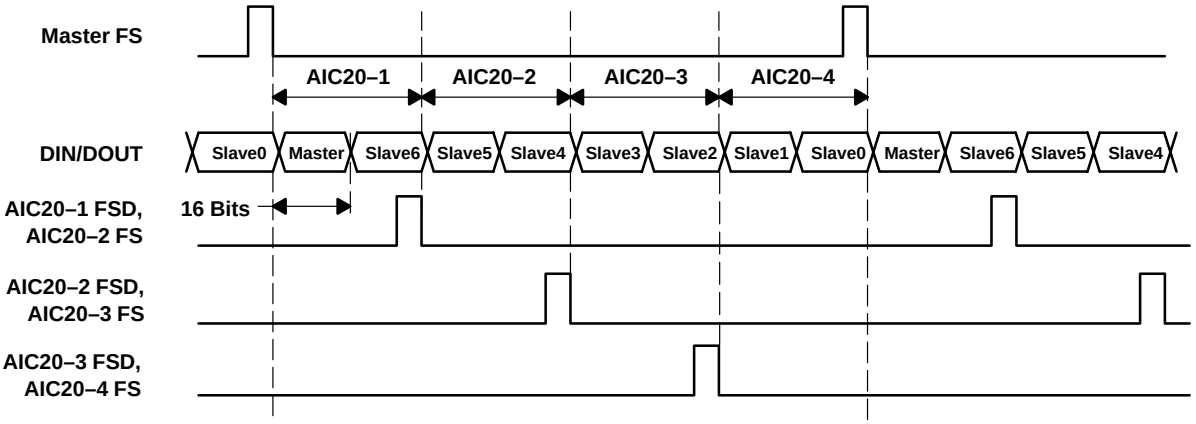


Figure 3–3. Timing Diagram for FSD Output



NOTE: AIC20 #4 FSD should be pulled high.

Figure 3–4. Cascading FS/FSD Timing of Four AIC20s in Continuous Data Transfer Mode

3.7 Host Port Interface

The host port uses a 2-wire serial interface (SCL, SDA) to program each codec channel's six control registers and selectable protocol between S^2C mode and I^2C mode. The S^2C is a write-only mode and the I^2C is a read-write mode selected by bits D1–D0 (HPC bits) of control register 2. If the host interface is not needed, the two pins of SCL and SDA can be programmed to become general-purpose I/Os. If selected to be used as I/O pins, the SDA and SCL pins become output and input pins respectively, determined by D1 and D0.

Both S^2C and I^2C require a SMARTDM device address to communicate with the AIC20. One of SMARTDM's advanced features is the automatic cascade detection (ACD) that enables SMARTDM to automatically detect the total number of codecs in the serial connection and use this information to assign each codec a distinct SMARTDM device address. Table 3–1 lists device addresses assigned to each codec in the cascade by the SMARTDM. The master always has the highest position in the cascade. For example in Figure 3–2, there is a total of 4 codecs in the cascade (i.e., one master and 3 slaves), then the device addresses in row 4 are used in which the master is codec 1 with a device address of 0000.

Table 3–1. SMARTDM Device Addresses

TOTAL CHANNELS	CHANNELs POSITION IN CASCADE (1 CODEC HAS 2 CHANNELS)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1																0000
2															0001	0000
3														0010	0001	0000
4													0011	0010	0001	0000
5												0100	0011	0010	0001	0000
6											0101	0100	0011	0010	0001	0000
7										0110	0101	0100	0011	0010	0001	0000
8									0111	0110	0101	0100	0011	0010	0001	0000
9								1000	0111	0110	0101	0100	0011	0010	0001	0000
10							1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
11						1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
12					1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
13				1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
14			1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
15		1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
16	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000

3.7.1 S^{2}C (Start-Stop Communication)

The S^{2}C is a write-only interface selected by programming bits D1-D0 of control register 2 to 01. The SDA input is normally in a high state, pulled low (START bit) to start the communication, and pulled high (STOP bit) after the transmission of the LSB. Figure 3–5 shows the timing diagram of S^{2}C. The S^{2}C also supports a broadcast mode in which the same register of all devices in cascade is programmed in a single write. To use S^{2}C's broadcast mode, execute the following steps:

1. Write 111 1000 1111 1111 after the start bit to enable the broadcast mode.
2. Write data to program control register as specified in Figure 3–5 with bits D14–D11 = XXXX (don't care).
3. Write 111 1000 0000 0000 after the start bit to disable the broadcast mode.

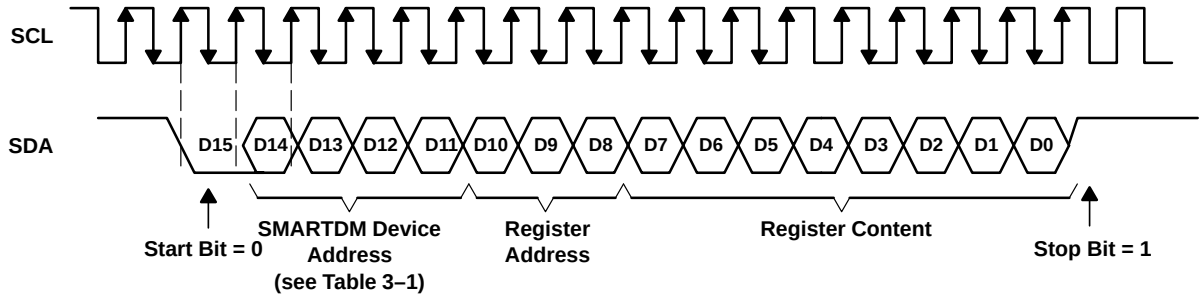


Figure 3–5. S^{2}C Programming

3.7.2 I2C

- Each I2C read-from or write-to each codec,s control register is given by an index register address.
- Read/write sequence always starts with the first byte as I2C address followed by 0. During the second byte, default/broadcast mode is set and the index register address is initialized. For write operation control register, data to be written is given from the third byte onwards. For read operation, stop-start is performed after the second byte. Now the first byte is I2C address followed by 1. From the second byte onwards, control register data appears.
- Each time read/write is performed, the index register address is incremented so that the next read/write is performed on the next control register.
- During the first write cycle and all write cycles in the broadcast, only the device with address 0000 issues ACK to the I2C.

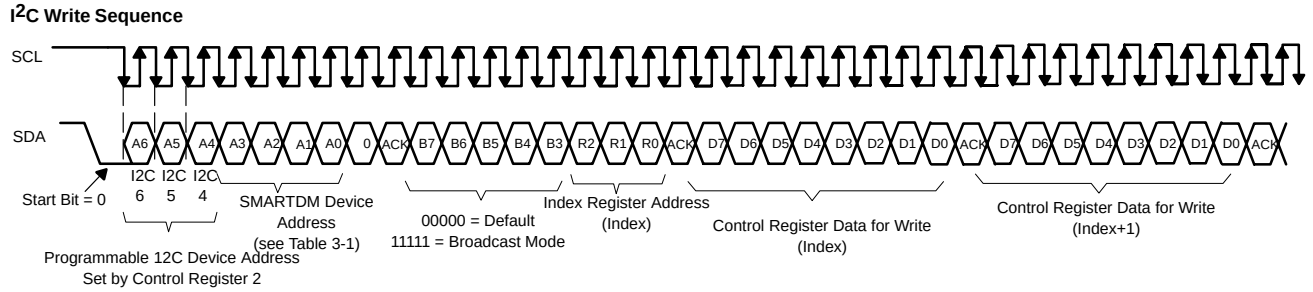


Figure 3–6. I2C Write Sequence

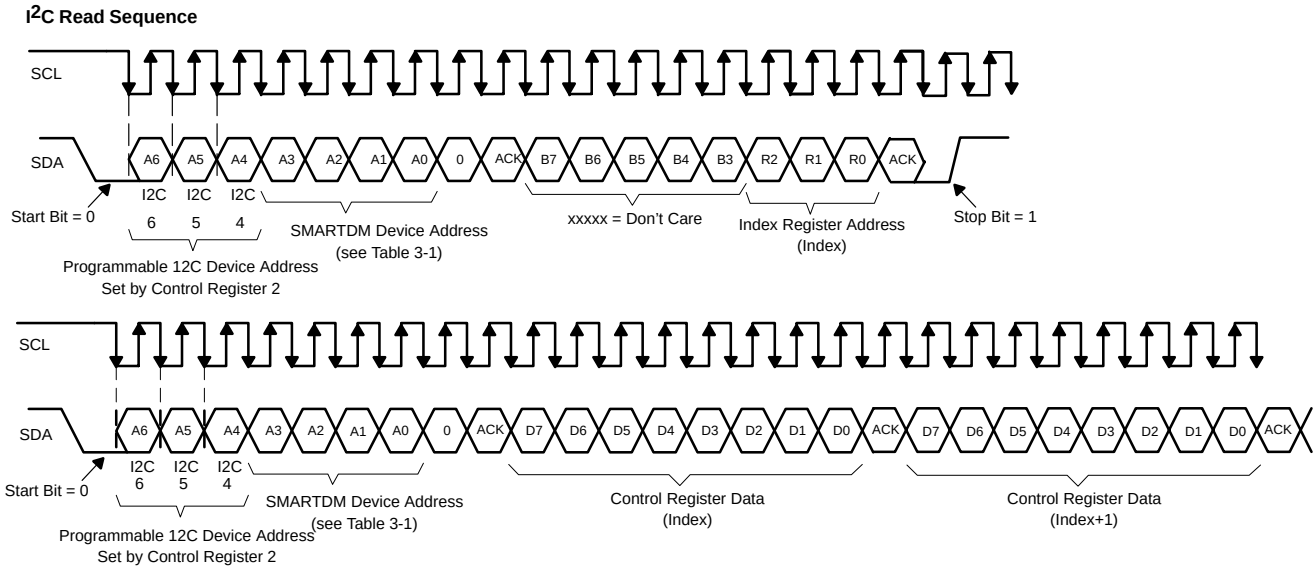


Figure 3–7. I2C Read Sequence

Each codec has an index register address. To perform a write operation, make the LSB of the first byte as 0 (write) (see Figure 3–8). During the second byte, the index register address is initialized and mode (broadcast/default) is set. From the third byte onwards, write data to the control register (given by index register) and increment the index register until stop or repeated start occurs. For operation, make the LSB of the first byte as 1 (read). From the second byte onwards, AIC starts transmitting data from the control register (given by the index register) and increments the index register. For setting the index register perform operation the same as write case for 2 bytes, and then give a stop or repeated start.

S/Sr –> Start/Repeated Start.

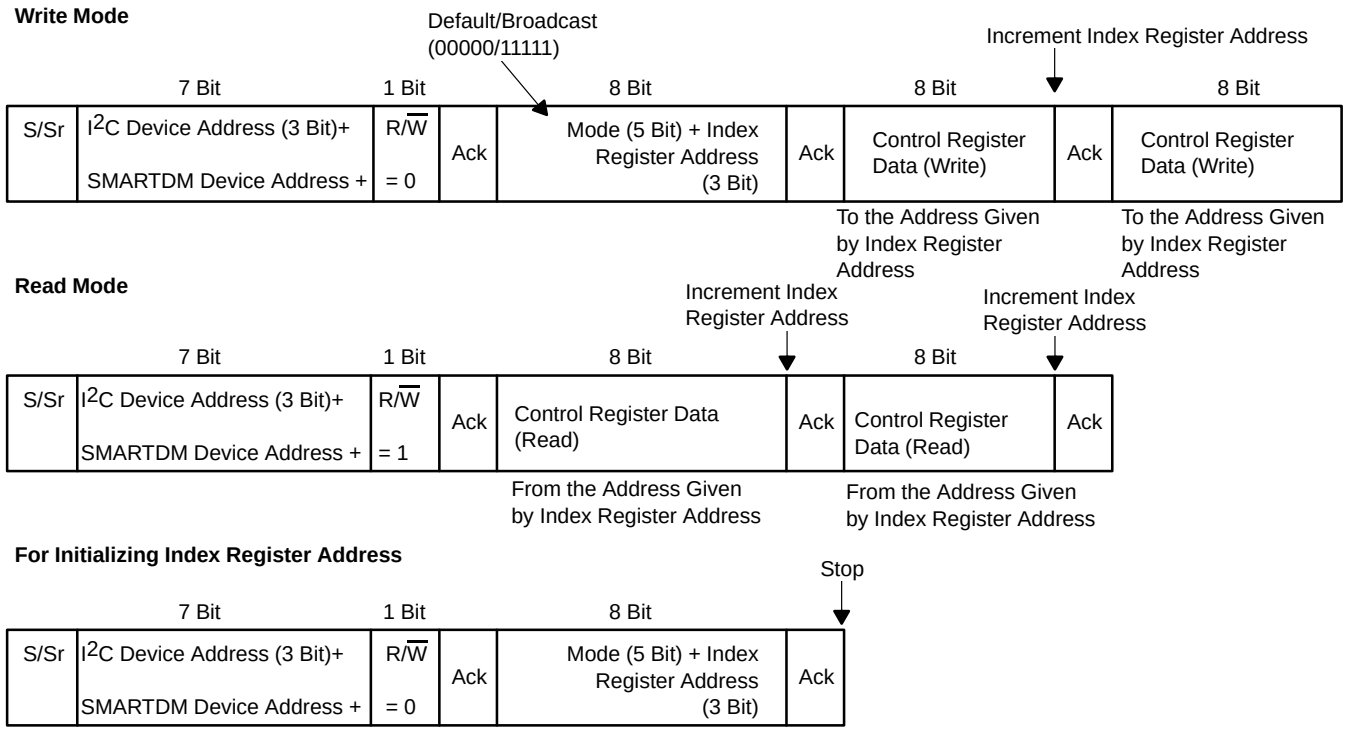


Figure 3–8. Index Register Addresses

3.8 Smart Time Division Multiplexed Serial Port (SMARTDM)

The SMART time division multiplexed serial port (SMARTDM) uses the four wires of DOUT, DIN, SCLK, and FS to transfer data into and out of the AIC20. The TLV320AIC20s SMARTDM supports three serial interface configurations (see Table 3–2): stand-alone master, stand-alone slave, and master-slave cascade, employing a time division multiplexed (TDM) scheme (a cascade of only-slaves is not supported). The SMARTDM allows for a serial connection of up to 16 codecs to a single serial port. Data communication in the three serial interface configurations can be carried out in either standard operation (Default) or turbo operation. Each operation has two modes: programming mode (default mode) and continuous data transfer mode. To switch from the programming mode to the continuous data transfer mode, set bit D6 of control register 1 to 1, which is reset automatically after switching back to programming mode. The TLV320AIC20 can be switched back from the continuous data transfer mode to the programming mode by setting the LSB of the data on DIN to 1, only if the data format is (15+1), as selected by bit 0 of control register 1. The SMARTDM automatically adjusts the number of time slots per frame sync (FS) to match the number of codecs in the serial interface so that no time slot is wasted. Both the programming mode and the continuous data transfer mode of the TLV320AIC20 are compatible with the TLV320AIC12. The TLV320AIC20 provides primary/secondary communication and continuous data transfer with improvements and eliminates the requirements for hardware and software requests for secondary communication as seen in the TLV320AIC10. The TLV320AIC20 continuous data transfer mode now supports both master/slave stand-alone and cascade.

Table 3–2. Serial Interface Configurations

TLV320AIC20 CONNECTIONS	M/S PIN		FSD PIN		COMMENTS
	MASTER	SLAVE	MASTER	SLAVE	
Stand-alone	High	Low	Pull high	Low	
Master-slave cascade	High	Low	Connect to the next slave's FS (see Figure 3–4)		Last slave's FSD pin is pulled high
Slave-slave cascade	NA	NA	NA	NA	Not supported

3.8.1 Programming Mode

In the programming mode, the FS signal starts the input/output data stream. Each period of FS contains two frames as shown in Figures 3–10 and 3–11: data frame and control frame. The data frame contains data transmitted from the ADC or to the DAC. The control frame contains data to program each codec control register. The SMARTDM automatically sets the number of time slots per frame equal to the number of codec channels in the interface. Each time slot contains 16-bit data. The SCLK is used to perform data transfer for the serial interface between the AIC20 codecs and the DSP. The frequency of SCLK varies, depending on the selected mode of serial interface. In the stand alone-mode, there are 64 SCLKs (or four time slots) per sampling period. In the master-slave cascade mode, the number of SLCKs equals 32x(number of codec channels in the cascade). The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronization clock for the serial communication data and the frame-sync is taken from SCLK. The frame-sync signal that starts the ADC and DAC data transfer interval is taken from FS. The SMARTDM also provides a turbo operation, in which the FS's frequency is always the device's sampling frequency, but SCLK is running at a much higher speed. Thus, there are more than 64 SCLKs for each AIC20 per sampling period, in which the data frame and control frame occupy only the first 64 SCLKs from the falling edge of the frame-sync FS (also see Section 3.6 for more details).

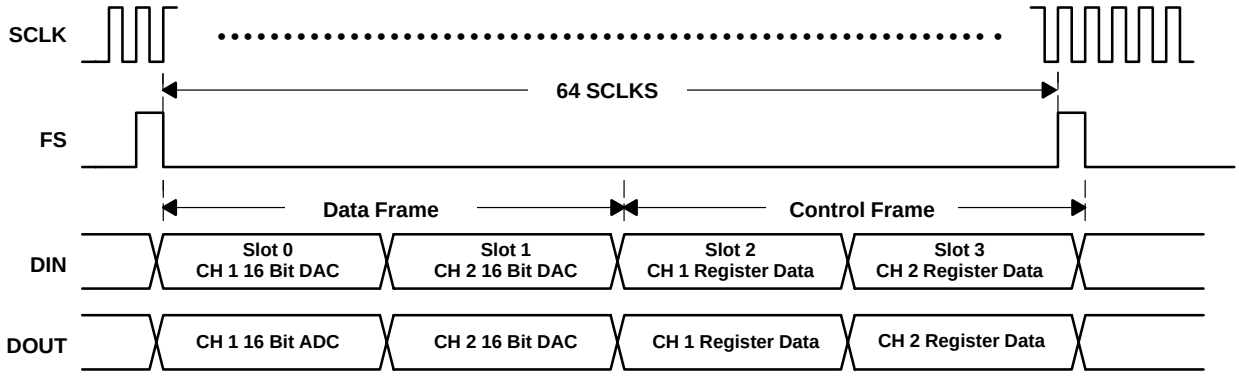
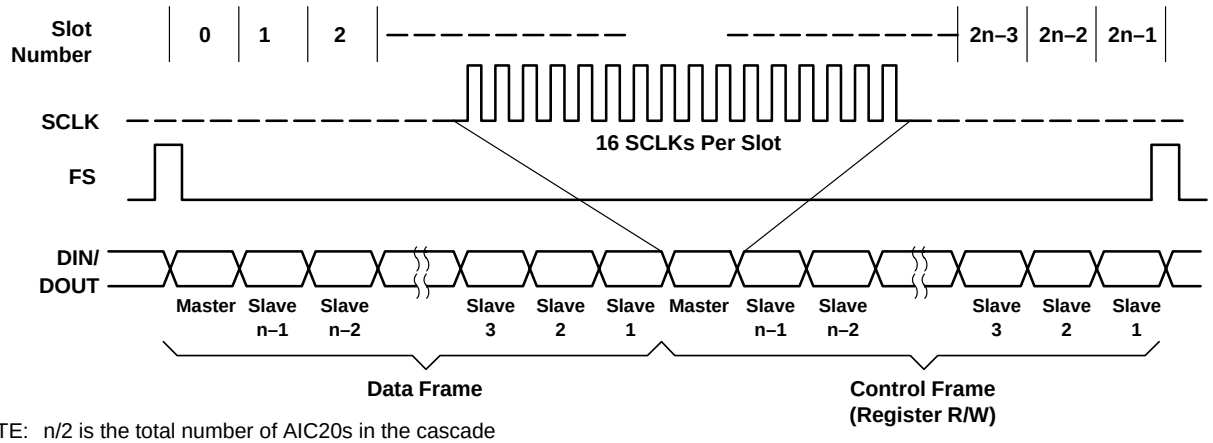


Figure 3–9. Programming Mode: Stand-Alone Timing



NOTE: n/2 is the total number of AIC20s in the cascade

Figure 3–10. Standard Operation/Programming Mode: Master-Slave Cascade Timing

3.8.2 Continuous Data Transfer Mode

The continuous data transfer mode, selected by setting bit D6 of each codec's control register 1 to 1, contains conversion data only. In continuous data transfer mode, the control frame is eliminated, and the period of FS signal contains only the data frame in which the 16-bit data is transferred contiguously, with no inactivity between bits. The control frame can be reactivated by setting the LSB of DIN data to 1 if the data is in the 15+1 format. To return the programming mode in the 16-bit DAC data format mode, write 0 in bit D6 of each codec's control register 1 using I^2C or S^2C, or do a hardware reset to come out of continuous data transfer mode. The continuous data transfer mode can support the TI DSP McBSPs autobuffering unit (ABU) operation in the serial port interrupts are not generated with each word transferred to prevent CPU's ISR overheads.

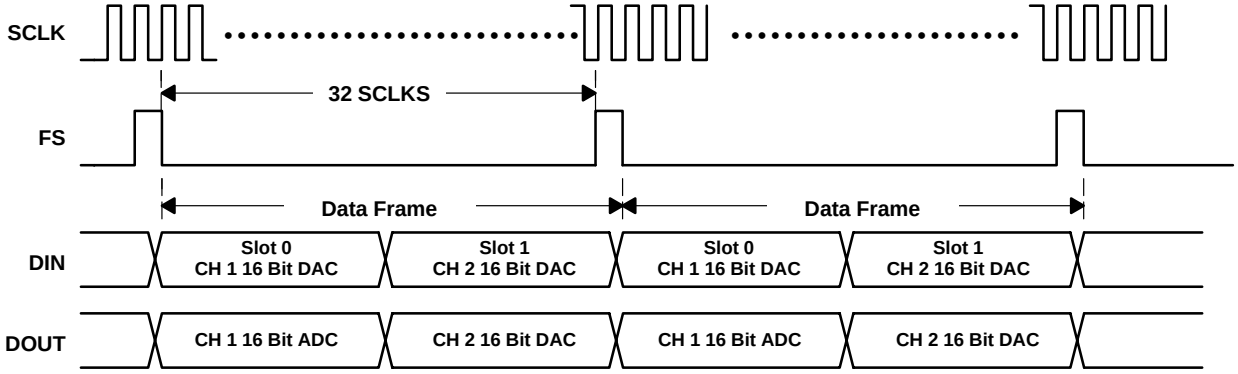
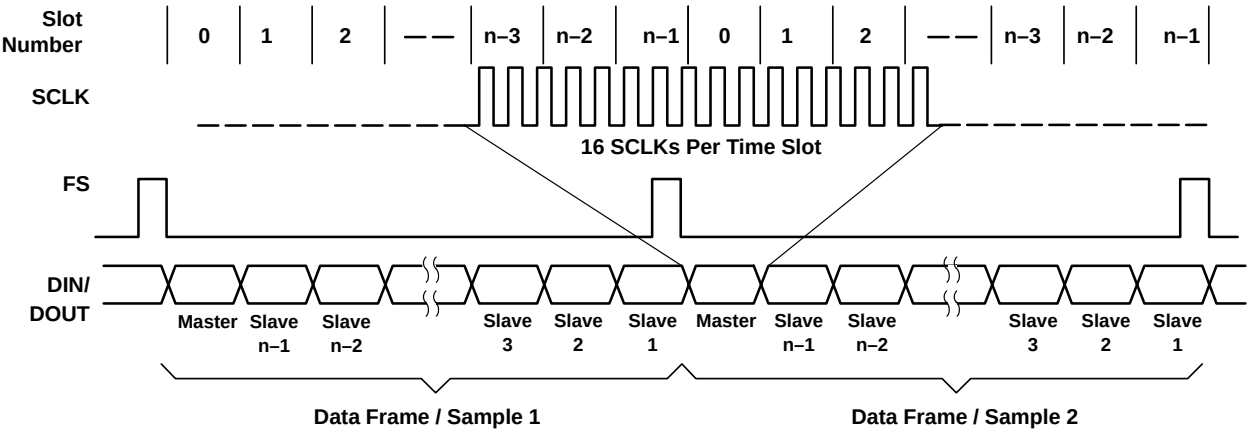


Figure 3–11. Standard Operation/Continuous Data Transfer Mode: Stand-Alone Timing



NOTE: n/2 is the total number of AIC20s in the cascade

Figure 3–12. Standard Operation/Continuous Data Transfer Mode: Master-Slave Cascade Timing

3.8.3 Turbo Operation (SCLK)

Setting TURBO = 1 (bit D7) in each codec's control register 2 enables the AIC20's turbo mode that requires the following condition to be met:

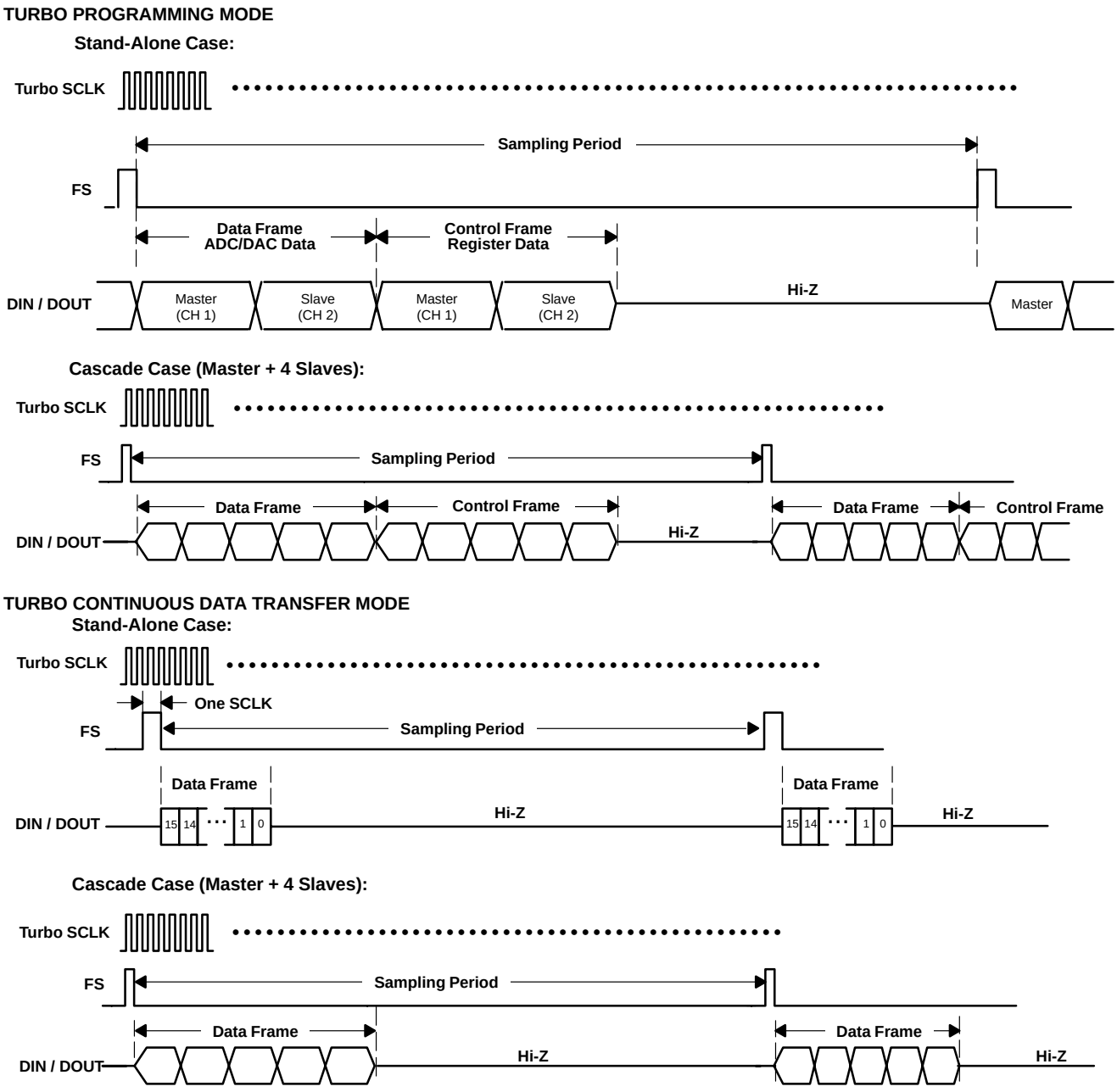
- M × N > #Devices × mode

Where:

M, N, and P are clock divider values defined in the control register 4.
#Device is the number of codec channels in cascade. (#Device = 2 for stand-alone AIC20)
Mode is equal to 1 for continuous data transfer mode and 2 for programming mode.

The turbo operation is useful for applications that require more bandwidth for multitasking processing per sampling period. In the turbo mode (see Figure 3–13), the FSs frequency is always the device's sampling frequency, but the

SCLK is running at much higher speed than that described in Section 3.6.1. The output SCLK frequency is equal to (MCLK/P) and up to a maximum speed of 25 MHz. The data/control frame is still 32-SCLK long and the FS is one-SCLK pulse. Therefore, the DSP can maximize its data processing bandwidth by taking advantage of time available between the end of AIC20 control frame and the next frame-sync FS to process other tasks.



NOTE: SCLK is not drawn to scale.

Figure 3–13. Timing Diagram for Turbo Operation

3.9 Control Register Programming

Each channel in the TLV320AIC20 contains six control registers that are used to program available modes of operation. All register programming occurs during the control frame through DIN. New configuration takes effect after a delay of one frame sync. The TLV320AIC20 is defaulted to the programming mode upon power up. Set bit 6 in control register 1 to switch to continuous data transfer mode. If the 15+1 data format of DIN has been selected, the LSB of the DIN to 1 to switch from continuous data transfer mode to programming set mode. Otherwise, either the device needs to be reset or the host port writes 0 to bit D6 of each codec's control register 1 during the continuous data transfer mode to switch back to the programming mode.

3.9.1 Data Frame Format

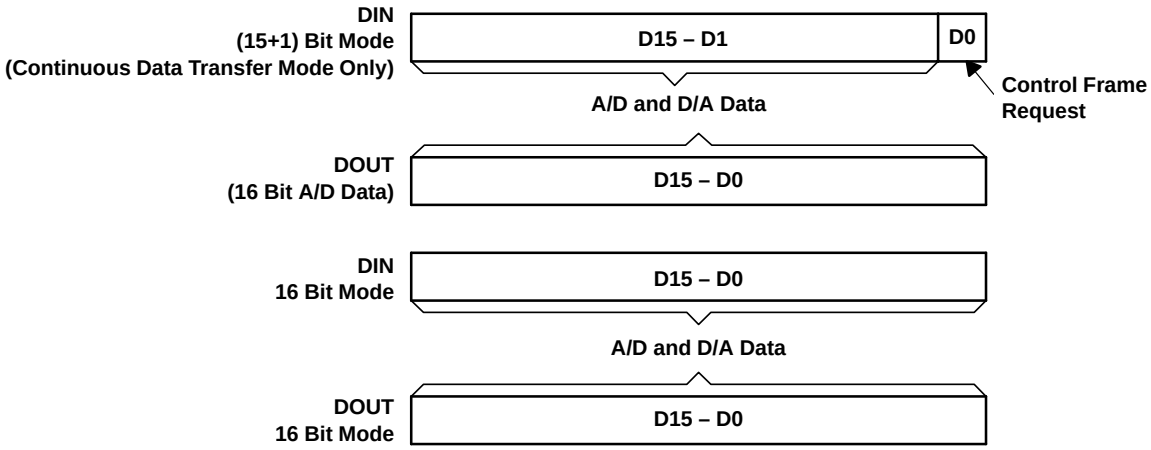


Figure 3–14. Data Frame Format

3.9.2 Control Frame Format (Programming Mode)

During the control frame, the DSP sends 16-bit words to each codec's time slot SMARTDM(TM) through DIN to read or write control registers in each codec shown in Table 3–4. The upper byte (Bits D15–D8) of the 16-bit control-frame word defines the read/write command. Bits D15–D13 define the control register address with register content occupied the lower byte D7–D0. Bit D12 is set to 0 for a write or to 1 for a read. Bit D11 in the write command is used to perform the broadcast mode. During a register write, the register content is located in the lower byte of DIN. During a register read, the register content is output in the lower byte of DOUT in the same control frame, whereas the lower byte of DIN is ignored.

3.9.3 Broadcast Register Write

Broadcast operation is very useful for a cascading system of SMARTDM DSP codecs in which all register programming can be completed in one control frame. During the control frame and in any register-write time slot, if the broadcast bit (D11) is set to 1, the register content of that time slot is written into the specified register of all devices in cascade (see Figure 3–16). This reduces the DSP's overhead of doing multiple writes to program the same data into cascaded devices.

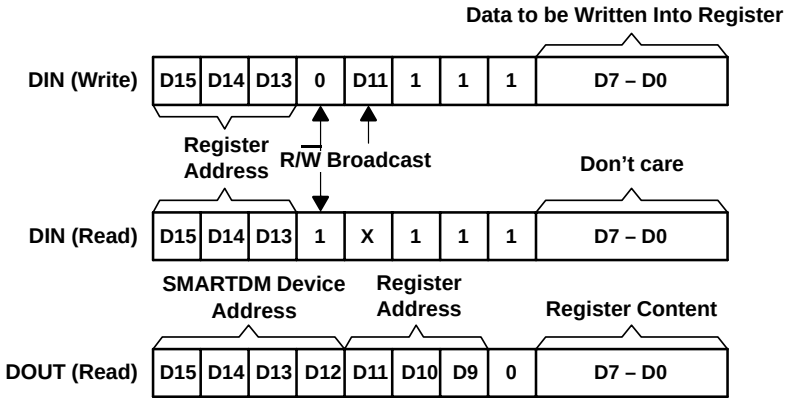
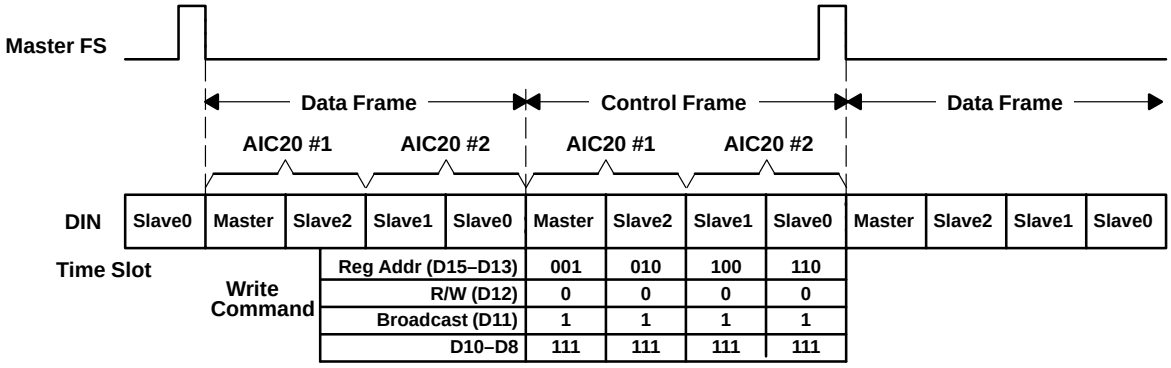


Figure 3–15. Control Frame Data Format



NOTE: In this example, the broadcast operation (D11 = 1) is used to program the four control registers of Reg.1, Reg.2, Reg.4, and Reg.6 in all four DSP codecs of two TLV320AIC20s in cascade (Master, Slave2, Slave1, and Slave0) during the same frame (i.e., register 1 of the four codecs contains the same data).

Figure 3–16. Broadcast Register Write Example

3.9.4 Register Map

Bits D15 through D13 represent the control register address that is written with data carried in D7 through D0. Bit D12 determines a read or a write cycle to the addressed register. When D12 = 0, a write cycle is selected. When D12 = 1, a read cycle is selected. Bit D11 controls the broadcast mode as described above, in which the broadcast mode is enabled if D11 is set to 1. Always write 1s to the bits D10 through D8.

Table 3–3 shows the register map.

Table 3–3. Register Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address			RW	BC	1	1	1	Control Register Content							

Table 3–4. Register Addressing

REGISTER NO.	D15	D14	D13	REGISTER NAME
0	0	0	0	No operation
1	0	0	1	Control 1
2	0	1	0	Control 2
3	0	1	1	Control 3
4	1	0	0	Control 4
5	1	0	1	Control 5
6	1	1	0	Control 6

4 Control Register Content Description

4.1 Control Register 1

D7	D6	D5	D4	D3	D2	D1	D0
ADOVF	CX	IIR	DAOVF	BIASV	ALB	DLB	DAC16
R	R/W	R/W	R	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–1. Control Register 1 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	ADOVF	0	ADC over flow. This bit indicates whether the ADC is overflow. ADOVF = 0 No overflow ADOVF = 1 A/D is overflow.
D6	CX	0	Continuous data transfer mode. This bit selects between programming mode and continuous data transfer mode. CX = 0 Programming mode CX = 1 Continuous data transfer mode
D5	IIR	0	IIR Filter. This bit selects between FIR and IIR for decimation/interpolation low-pass filter. IIR = 0 FIR filter is selected. IIR = 1 IIR filter is selected.
D4	DAOVF	0	DAC over flow. This bit indicates whether the DAC is overflow DAOVF = 0 No overflow DAOVF = 1 DAC is overflow
D3	BIASV	0	Bias voltage. This bit selects the output voltage for BIAS pin BIASV = 0 BIAS pin = 1.35 V BIASV = 1 BIAS pin = 2.35 V
D2	ALB	0	Analog loop back ALB = 0 Analog loopback disabled ALB = 1 Analog loopback enabled
D1	DLB	0	Digital loop back DLB = 0 Digital loopback disabled DLB = 1 Digital loopback enabled
D0	DAC16	0	DAC 16-bit data format. This bit applies to the continuous data transfer mode only to enable the 16-bit data format for DAC input. DAC16 = 0 DAC input data length is 15 bits. Writing a 1 to the LSB of the DAC input to switch from continuous data transfer mode to programming mode. DAC16 = 1 DAC input data length is 16 bit.

4.2 Control Register 2

D7	D6	D5	D4	D3	D2	D1	D0
TURBO	DIFBP	I^2C6	I^2C5	I^2C4	GPO	HPC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–2. Control Register 2 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION

D7	TURBO	0	Turbo mode. This bit is used to set the SCLK rate.
			TURBO = 0 SCLK = (16 × FS × #Device × mode)
			TURBO = 1 SCLK = MCLK/P (P is determined in register 4)

D6	DIFBP	0	Decimation/interpolation filter bypass. This bit is used to bypass both decimation and interpolation filters. DIFBP = 0 Decimation/interpolation filters are operated. DIFBP = 1 Decimation/interpolation filters are bypassed.
D5–D3	I^2Cx	100	I^2C device address. These three bits are programmable to define three MSBs of the I^2C device address (reset value is 100). These three bits are combined with the 4-bit SMARTDM device address to form 7-bit I^2C device address.
D2	GPO	0	General-purpose output
D1–D0	HPC	00	Host port control bits. Write the following values into D1–D0 to select the appropriate configuration for two pins SDA and SCL. SDA pin is set to be equal to D2 if D1–D0 = 10. D1–D0 0 0 SDA and SCL pins are used for I^2C interface 0 1 SDA and SCL pins are used for S^2C interface 1 0 SDA pin = D2, input going into SCL pin is output to DOUT 1 1 SDA pin = Control frame flag.

4.3 Control Register 3

4.3.1 Control Register 3A

D7	D6	D5	D4	D3	D2	D1	D0
00		PWDN		SWRS	ASRF		
R/W	R/W	R/W		R/W	R/W		

NOTE: R = Read, W = Write

Table 4–3. Control Register 3A Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5–D4	PWDN	00	Power down PWDN = 00 No power down PWDN = 01 Power-down A/D PWDN = 10 Power-down D/A PWDN = 11 Software power down the entire device
D3	SWRS	0	Software reset. Set this bit to 1 to reset the device.
D2-D0	ASRF	001	Asynchronous sampling rate factor. These three bits define the ratio n between FS frequency and the desired sampling frequency fs (Applied only if different sampling rate between CODEC1 and CODEC2 is desired) ASRF = 001 n = FS/fs = 1 ASRF = 010 n = FS/fs = 2 ASRF = 011 n = FS/fs = 3 ASRF = 100 n = FS/fs = 4 ASRF = 101 n = FS/fs = 5 ASRF = 110 n = FS/fs = 6 ASRF = 111 n = FS/fs = 7 ASRF = 000 n = FS/fs = 8

4.3.2 Control Register 3B

D7	D6	D5	D4	D3	D2	D1	D0
01		8KBF	Reserved	MHNS	MHDS	MLDO	MSPK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–4. Control Register 3B Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5	8KBF	0	8 kHz band pass filter. Set this bit to 1 to enable the band-bass filter [300 Hz –3.3 kHz] with the sampling rate at 8 kHz.
D4	Reserved	0	
D3	MHNS	0	Mute handset. This bit controls the MUTE function of handset output driver. MHNS = 0 Handset output driver is not MUTE. MHNS = 1 Handset output driver is MUTE.
D2	MHDS	0	Mute headset. This bit controls the MUTE function of headset output driver. MHDS = 0 Headset output driver is not MUTE. MHDS = 1 Headset output driver is MUTE.
D1	MLNO	0	Mute line output. This bit controls the MUTE function of the 600-Ω output driver. MLNO = 0 The 600-Ω output driver is not MUTE. MLNO = 1 The 600-Ω output driver is MUTE.
D0	MSPK	0	Mute 8-Ω speaker. This bit controls the MUTE function of the 8-Ω speaker driver. MSPK = 0 The 8-Ω speaker driver is not MUTE. MSPK = 1 The 8-Ω speaker driver is MUTE.

4.3.3 Control Register 3C

D7	D6	D5	D4	D3	D2	D1	D0
10		Reserved	ICID			OSR	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–5. Control Register 3C Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5	Reserved	0	
D4–D2	ICID	000	Chip ID. These two bits represent the device version number. ICID = 000 Version 1 ICID = 001 Version 2 ICID = 010 Version 3 ICID = 011 Version 4 ICID = 100 Version 5 ICID = 101 Version 6 ICID = 110 Version 7 ICID = 111 Version 8
D1–D0	OSR option	00	OSR option D1–D0 = X1 OSR for DAC Channel is 512 (Max FS = 8 Ksps) D1–D0 = 10 OSR for DAC Channel is 256 (Max FS = 16Ksps) D1–D0 = 00 OSR for DAC Channel is 128 (Max FS = 26Ksps)

4.3.4 Control Register 3D

D7	D6	D5	D4	D3	D2	D1	D0
11		LCDAC					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–6. Control Register 3D Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5–D0	LCDAC	000000	LCD DAC. These bits represent the input value for the 6-bit LCD DAC.

NOTE: See section 5–16 for LCD DAC specification

4.4 Control Register 4

D7	D6	D5	D4	D3	D2	D1	D0
FSDIV	MNP						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–7. Control Register 4 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	FSDIV	0	Frame sync division factor FSDIV = 0 To write value of P to bits D2-D0 and value of N to bits D6-D3 FSDIV = 1 To write value of M to bits D6-D0
D6–D0	MNP	—	Divider values of M,N, and P to be used in junction with the FSDIV bit for calculation of FS frequency according to the formula FS = MCLK / (16xMxNxP) • M = 1,2,…,128 Determined by D6-D0 with FSDIV = 1 D7-D0 = 10000000 M = 128 D7-D0 = 10000001 M = 1 • • D7-D0 = 11111111 M = 127 • N = 1,2,…,16 Determined by D6-D3 with FSDIV = 0 D7-D0 = 00000xxx N = 16 D7-D0 = 00001xxx N = 1 • • D7-D0 = 01111xxx N = 15 • P = 1,2,…,8 Determined by D2-D0 with FSDIV = 0 D7-D0 = 0xxxx000 P = 8 D7-D0 = 0xxxx001 P = 1 • • D7-D0 = 0xxxx111 P = 7

NOTES: 1. It takes 2 sampling periods to update new values of M,N, and P.
2. In register read operation, first read receives N and P values and second read receives M value.
3. M(default) = 16, N(default) = 6, P(default) = 8
4. If P = 8, the device enters the coarse sampling mode as described in Section 3.1 Operating Frequencies

4.5 Control Register 5A

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ADPGA					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–8. A/D PGA Gain

D5	D4	D3	D2	D1	D0	ADPGA
0	1	1	1	1	1	ADC input PGA gain = MUTE
0	1	1	1	1	0	ADC input PGA gain = 54 dB
0	1	1	1	0	1	ADC input PGA gain = 48 dB
0	1	1	1	0	0	ADC input PGA gain = 42 dB
0	1	1	0	1	1	ADC input PGA gain = 40.5 dB
0	1	1	0	1	0	ADC input PGA gain = 39 dB
0	1	1	0	0	1	ADC input PGA gain = 37.5 dB
0	1	1	0	0	0	ADC input PGA gain = 36 dB
0	1	0	1	1	1	ADC input PGA gain = 34.5 dB
0	1	0	1	1	0	ADC input PGA gain = 33 dB
0	1	0	1	0	1	ADC input PGA gain = 31.5 dB
0	1	0	1	0	0	ADC input PGA gain = 30 dB
0	1	0	0	1	1	ADC input PGA gain = 28.5 dB
0	1	0	0	1	0	ADC input PGA gain = 27 dB
0	1	0	0	0	1	ADC input PGA gain = 25.5 dB
0	1	0	0	0	0	ADC input PGA gain = 24 dB
0	0	1	1	1	1	ADC input PGA gain = 22.5 dB
0	0	1	1	1	0	ADC input PGA gain = 21 dB
0	0	1	1	0	1	ADC input PGA gain = 19.5 dB
0	0	1	1	0	0	ADC input PGA gain = 18 dB
0	0	1	0	1	1	ADC input PGA gain = 16.5 dB
0	0	1	0	1	0	ADC input PGA gain = 15 dB
0	0	1	0	0	1	ADC input PGA gain = 13.5 dB
0	0	1	0	0	0	ADC input PGA gain = 12 dB
0	0	0	1	1	1	ADC input PGA gain = 10.5 dB
0	0	0	1	1	0	ADC input PGA gain = 9 dB
0	0	0	1	0	1	ADC input PGA gain = 7.5 dB
0	0	0	1	0	0	ADC input PGA gain = 6 dB
0	0	0	0	1	1	ADC input PGA gain = 4.5 dB
0	0	0	0	1	0	ADC input PGA gain = 3 dB
0	0	0	0	0	1	ADC input PGA gain = 1.5 dB
0	0	0	0	0	0	ADC input PGA gain = 0 dB

4.6 Control Register 5B

D7	D6	D5	D4	D3	D2	D1	D0
0	1	DAPGA					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–9. D/A PGA Gain

D5	D4	D3	D2	D1	D0	DAPGA
0	1	1	1	1	1	DAC input PGA gain = MUTE
0	1	1	1	1	0	DAC input PGA gain = –54 dB
0	1	1	1	0	1	DAC input PGA gain = –48 dB
0	1	1	1	0	0	DAC input PGA gain = –42 dB
0	1	1	0	1	1	DAC input PGA gain = –40.5 dB
0	1	1	0	1	0	DAC input PGA gain = –39 dB
0	1	1	0	0	1	DAC input PGA gain = –37.5 dB
0	1	1	0	0	0	DAC input PGA gain = –36 dB
0	1	0	1	1	1	DAC input PGA gain = –34.5 dB
0	1	0	1	1	0	DAC input PGA gain = –33 dB
0	1	0	1	0	1	DAC input PGA gain = –31.5 dB
0	1	0	1	0	0	DAC input PGA gain = –30 dB
0	1	0	0	1	1	DAC input PGA gain = –28.5 dB
0	1	0	0	1	0	DAC input PGA gain = –27 dB
0	1	0	0	0	1	DAC input PGA gain = –25.5 dB
0	1	0	0	0	0	DAC input PGA gain = –24 dB
0	0	1	1	1	1	DAC input PGA gain = –22.5 dB
0	0	1	1	1	0	DAC input PGA gain = –21 dB
0	0	1	1	0	1	DAC input PGA gain = –19.5 dB
0	0	1	1	0	0	DAC input PGA gain = –18 dB
0	0	1	0	1	1	DAC input PGA gain = –16.5 dB
0	0	1	0	1	0	DAC input PGA gain = –15 dB
0	0	1	0	0	1	DAC input PGA gain = –13.5 dB
0	0	1	0	0	0	DAC input PGA gain = –12 dB
0	0	0	1	1	1	DAC input PGA gain = –10.5 dB
0	0	0	1	1	0	DAC input PGA gain = –9 dB
0	0	0	1	0	1	DAC input PGA gain = –7.5 dB
0	0	0	1	0	0	DAC input PGA gain = –6 dB
0	0	0	0	1	1	DAC input PGA gain = –4.5 dB
0	0	0	0	1	0	DAC input PGA gain = –3 dB
0	0	0	0	0	1	DAC input PGA gain = –1.5 dB
0	0	0	0	0	0	DAC input PGA gain = 0 dB

4.7 Control Register 5C

D7	D6	D5	D4	D3	D2	D1	D0
1	0	ASTG			DSTG		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–10. Analog Sidetone Gain

D5	D4	D3	DSTG
1	1	1	Analog sidetone gain = MUTE
1	1	0	Analog sidetone gain = -27 dB
1	0	1	Analog sidetone gain = -24 dB
1	0	0	Analog sidetone gain = -21 dB
0	1	1	Analog sidetone gain = -18 dB
0	1	0	Analog sidetone gain = -15 dB
0	0	1	Analog sidetone gain = -12 dB
0	0	0	Analog sidetone gain = -9 dB

Table 4–11. Digital Sidetone Gain

D2	D1	D0	DSTG
1	1	1	Digital sidetone gain = MUTE
1	1	0	Digital sidetone gain = -27 dB
1	0	1	Digital sidetone gain = -24 dB
1	0	0	Digital sidetone gain = -21 dB
0	1	1	Digital sidetone gain = -18 dB
0	1	0	Digital sidetone gain = -15 dB
0	0	1	Digital sidetone gain = -12 dB
0	0	0	Digital sidetone gain = -9 dB

NOTE: Default value of ASTG = 111
Default value of DSTG = 111

4.8 Control Register 5D

D7	D6	D5	D4	D3	D2	D1	D0
1	1	SPKG		Reserved			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–12. Control Register 5D Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5–D4	SPKG	00	Speaker Gain SPKG = 00 0 dB Gain SPKG = 01 1 dB Gain SPKG = 10 2 dB Gain SPKG = 11 3 dB Gain
D3–D0	Reserved	0000	

4.9 Control Register 6A

D7	D6	D5	D4	D3	D2	D1	D0
0	HDSI2O	HNSI2O	CIDI	LINEI	MICI	HNSI	HDSI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–13. Control Register 6A Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D6	HDSI2O	0	Headset input to output HDSI2O = 0 The headset input is not connected to the headset output. HDSI2O = 1 The headset input is connected to the headset output.
D5	HNSI2O	0	Handset input to output HNSI2O = 0 The handset input is not connected to the handset output. HNSI2O = 1 The handset input is connected to the handset output.
D4	CIDI	0	Caller ID input select CIDI = 0 The caller ID input is not connected to ADC channel. CIDI = 1 The caller ID input is connected to ADC channel.
D3	LINEI	0	Line input select LINEI = 0 The line driver input is not connected to ADC channel. LINEI = 1 The line driver input is connected to ADC channel.
D2	MICI	0	MIC input select MICI = 0 The microphone input is not connected to ADC channel. MICI = 1 The microphone input is connected to ADC channel.
D1	HNSI	0	Handset input select HNSI = 0 The handset input is not connected to ADC channel. HNSI = 1 The handset input is connected to ADC channel
D0	HDSI	0	Headset input select HDSI = 0 The headset input is not connected to ADC channel. HDSI = 1 The headset input is connected to ADC channel.

4.10 Control Register 6B

D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved	ASTOHD	ASTOHN	SPKO	LINEO	HNSO	HDSO
R/W	R	R	R	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–14. Control Register 6B Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D6	Reserved	0	
D5	ASTOHD	0	Analog sidetone output select for headset. This bit connects the analog sidetone to headset output. ASTOHD = 0. The analog sidetone is not connected to headset output. ASTOHD = 1. The analog sidetone is connected to headset output.
D4	ASTOHN	0	Analog sidetone output select for handset. This bit connects the analog sidetone to handset output. ASTOHN = 0. The analog sidetone is not connected to handset output. ASTOHN = 1. The analog sidetone is connected to handset output.
D3	SPKO	0	Speaker output select. This bit connects the DAC output to the 8-Ω speaker driver SPKO = 0 The speaker driver output is not connected to DAC channel. SPKO = 1 The speaker driver output is connected to DAC channel.
D2	LINEO	0	Line output select. This bit connects the DAC output to the 600-Ω line driver LINEO = 0 The line driver output is not connected to DAC channel. LINEO = 1 The line driver output is connected to DAC channel.
D1	HNSO	0	Handset output select. This bit connects the DAC output to the 150-Ω handset driver HNSO = 0 The handset driver output is not connected to DAC channel. HNSO = 1 The handset driver output is connected to DAC channel.
D0	HDSO	0	Headset output select. This bit connects the DAC output to the 150-Ω headset driver HDSO = 0 The headset driver output is not connected to DAC channel. HDSO = 1 The headset driver output is connected to DAC channel.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range: DVDD, AVDD (see Note 1) . . . . . –0.3 V to 4 V
DRVDD (see Note 1) . . . . . –0.3 V to 4 V
Output voltage range, all digital output signals . . . . . –0.3 V to DVDD + 0.3 V
Input voltage range, all digital input signals . . . . . –0.3 V to DVDD + 0.3 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds: package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	Analog, AVDD	2.7	3.3	3.6	V
	Analog output driver, DRVDD (see Note 2)	2.7	3.3	3.6	
	Digital core, DVDD	1.65	1.8	1.95	V
	Digital I/O, IOVDD	2.7	3.3	3.6	V
Analog single-ended peak-to-peak input voltage, $V_{I(analog)}$				2	V
Output load resistance, R_L	Between LINEO+ and LINEO– (differential)	600			Ω
	Between HDSO+ and HDSO– (differential)	150			
	Between HNSO+ and HDSO– (differential)	150			
	Between SPKO+ and SPKO– (differential)	8			
Input impedance for hybrid amps (LINE+, LINE–)			10		kΩ
Analog output load capacitance, C_L				20	pF
Digital output capacitance				20	pF
Master clock				100	MHz
ADC or DAC conversion rate				26	kHz
Operating free-air temperature, T_A		–40		85	°C

NOTE 2: DRVDD should be kept at the same voltage as AVDD.

5.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, IOV_{DD} = 3.3 V (Unless Otherwise Noted)

5.3.1 Digital Inputs and Outputs, f_S = 8 kHz, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT		0.8 IOVDD			V
V_{OL}	Low-level output voltage, DOUT				0.1 IOVDD	V
I_{IH}	High-level input current, any digital input			5		µA
I_{IL}	Low-level input current, any digital input			5		µA
C_i	Input capacitance			3		pF
C_o	Output capacitance			5		pF

5.4 ADC Path Filter, Sampling Rate = 8 kHz

5.4.1 ADC Channel Transfer (FIR) Response (Also Handset and Headset) Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature(see Note 3)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal is 0 dBm0	0 Hz to 60 Hz			–27/0.07	dB
		60 Hz to 200 Hz			–1.0/0.07	
		200 Hz to 300 Hz			–0.03/0.05	
		300 Hz to 2.4 kHz	–0.10		0.15	dB
		2.4 kHz to 3 kHz	–0.05		0.15	dB
		3 kHz to 3.4 kHz	–0.40		0.10	
		3.4 kHz to 3.6 kHz			–0.40	
		4 kHz			–26.00	
		4.5 kHz to 72 kHz			–52.00	

NOTE 3: The filter gain for both outside the passband is measured with respect to gain at 1.02 kHz. The analog input test signal is a sinewave with 0 dB = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal. The –3 dB passband is 0 to 3.6 kHz for an 8-kHz sampling rate and is 0 to 7.2 kHz for a sampling rate of 16 kHz. This bandpass for both scales linearly with the sample rate.

5.4.2 ADC Channel Transfer (IIR) Response (Also Handset and Headset) Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (see Note 3)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal is 0 dBm0	0 Hz to 60 Hz			–27/0.15	dB
		60 Hz to 200 Hz			–0.75/0.15	
		200 Hz to 300 Hz			0.1/0.15	
		300 Hz to 2.4 kHz	–0.10		0.25	
		2.4 kHz to 3 kHz	–0.05		0.20	
		3 kHz to 3.4 kHz	–0.05		0.20	
		3.44 kHz to 3.6 kHz			0.15	
		4 kHz			–42.00	
		4.5 kHz to 72 kHz			–52.00	

NOTE 3: The filter gain for both outside the passband is measured with respect to gain at 1.02 kHz. The analog input test signal is a sinewave with 0 dB = 4 $V_{I(PP)}$ differential as the reference level for ADC analog input signal. The –3 dB passband is 0 to 3.6 kHz for an 8-kHz sampling rate and is 0 to 7.2 kHz for a sampling rate of 16 kHz. This bandpass for both scales linearly with the sample rate.

5.5 ADC Dynamic Performance, Sampling Rate = 8 kHz

5.5.1 ADC Signal-to-Noise With FIR Filter (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	V_I = –3 dB	81	84		dB
		V_I = –9 dB	73	76		

NOTE 4: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input common mode is 1.35 V.

5.5.2 ADC Signal-to-Noise With IIR Filter (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	V_I = –3 dB		82		dB
		V_I = –9 dB		76		

NOTE 3: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V

5.5.3 ADC Signal-to-Distortion With FIR Filter (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Signal-to-total harmonic distortion + noise	V_I = –3 dB	83	90		dB
		V_I = –9 dB	81	88		

NOTE 4: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V

5.5.4 ADC Signal-to-Distortion With IIR Filter (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Signal-to-total harmonic distortion	V_I = –3 dB		83		dB
		V_I = –9 dB		77		

NOTE 4: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V

5.5.5 ADC Signal-to-Distortion + Noise Using FIR Filter (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Signal-to-total harmonic distortion + noise	V_I = –3 dB	80	83		dB
		V_I = –9 dB	73	76		

NOTE 4: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V

5.5.6 ADC Signal-to-Distortion + Noise Using IIR Filter (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Signal-to-total harmonic distortion + noise	V_I = –3 dB		78		dB
		V_I = –9 dB		70		

NOTE 4: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V

5.5.7 Typical ADC performance With PGA Gain Setting Using FIR (see Note 5)

PGA GAIN SETTING	SNR	THD	SINAD	UNIT
9 dB	83	90	81	dB
18 dB	83	97	83	
24 dB	78	95	77	
36 dB	72	95	72	

NOTE 5: Test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. Input amplitude is given such that output of PGA is at –3 dB level.

5.5.8 ADC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Differential-ended input level	PGA gain = 0 dB			4	V
V_{IO}	Input offset voltage			±5		mV
I_B	Input bias current			125		µA
	Common-mode voltage			1.35		V
	Dynamic range	V_I = –3 dB		87		dB
	Mute attenuation	PGA = Mute		Zero digital code		
	Intrachannel isolation			87		dB
E_G	Gain error	V_I = –3 dB at 1020 Hz		–0.45		dB
$E_{O(ADC)}$	ADC converter offset error			±15		mV
CMRR	Common-mode rejection ratio at INMx and INPx	V_I = –100 mV at 1020 Hz		50		dB
	Idle channel noise	V_{IN} = 0 V		70		µVrms
R_i	Input resistance	T_A = 25°C		10		kΩ
C_i	Input capacitance			2		pF
IIR	Channel delay			$5/f_S$		s
FIR				$17/f_S$		s

5.6 DAC Path Filter, f_S = 8 kHz

5.6.1 DAC Channel Transfer (FIR) Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal is 0 dBm0	0 Hz to 200 Hz			0.10	dB
		200 Hz to 300 Hz			–0.05	
		300 Hz to 2.4 kHz	–0.25		0.15	
		2.4 kHz to 3 kHz	–0.30		0.10	
		3 kHz to 3.4 kHz	–0.55		0.05	
		3.4 kHz to 3.6 kHz			–0.30	
		4 kHz			–28.00	
		4.5 kHz to 72 kHz			–70.00	

NOTE 6: The filter gain outside of the bandpass is measured with respect to gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 4 $V_{I(PP)}$. The pass band is 0 Hz to 3.6 kHz for an 8-kHz sample rate. This pass band scales linearly with the conversion rate.

5.6.2 DAC Channel Transfer (IIR) Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal is 0 dBm0	0 Hz to 200 Hz			0.05	dB
		200 Hz to 300 Hz			0.05	
		300 Hz to 2.4 kHz	–0.10		0.10	
		2.4 kHz to 3 kHz	–0.20		0.10	
		3 kHz to 3.4 kHz	–0.25		0.05	
		3.4 kHz to 3.6 kHz			0	
		4 kHz			–34.00	
		4.5 kHz to 72 kHz			–70.00	

NOTE 6: The filter gain outside of the bandpass is measured with respect to gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 4 $V_{I(PP)}$. The pass band is 0 Hz to 3.6 kHz for an 8-kHz sample rate. This pass band scales linearly with the conversion rate.

5.7 DAC Dynamic Performance

5.7.1 DAC Signal-to-Distortion Using FIR Filter (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio (SNR)	V_I = 0 dB	88	92		dB
		V_I = –9 dB	81	83		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.2 Signal-to-Noise Using IIR Filter (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	V_I = 0 dB		83		dB
		V_I = –9 dB		74		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.3 DAC Signal-to-Distortion Using FIR Filter (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Signal-to-total harmonic distortion	V_I = 0 dB	84	90		dB
		V_I = –9 dB	77	84		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.4 DAC Signal-to-Distortion Using IIR Filter (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Signal-to-total harmonic distortion	V_I = 0 dB		85		dB
		V_I = –9 dB		80		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.5 DAC Signal-to-Distortion + Noise Using FIR Filter (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Signal-to-total harmonic distortion + noise	V_I = 0 dB	82	88		dB
		V_I = –9 dB	76	80		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.6 DAC Signal-to-Distortion + Noise Using IIR Filter (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Signal-to-total harmonic distortion + noise	V_I = 0 dB		80		dB
		V_I = –9 dB		73		

NOTE 7: The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.7 DAC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range	V_I = 0 dB at 1020 Hz		92		dB
	Interchannel isolation			90		dB
E_G	Gain error, 0 dB	V_O = 0 dB at 1020 Hz		–0.7		dB
	Mute attenuation	PGA = Mute		90		dB
	Common mode voltage			1.35		V
	Idle channel narrow band noise	0 kHz–4 kHz, See Note 8		40		Vrms
V_{OO}	Output offset voltage at OUTP1_150 (differential)	DIN = All zeros		±8		mV
V_O	Analog output voltage, (3.3 V)	HDSO+	0.25		2.35	V
IIR	Channel delay			$5/f_S$		s
FIR				$18/f_S$		

NOTE 8: The conversion rate is 8 kHz.

5.8 Speaker Interface

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker output power	V_{CC} = 3.3 V, fully differential, 8-Ω load		250		mW
Maximum output current	8-Ω load		250		mA

5.9 Handset and Headset Interface

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker output power	V_{CC} = 3.3 V, fully differential, 150-Ω load		13		mW
Maximum output current	150-Ω load		13		mA

5.10 Line Interface

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker output power	V_{CC} = 3.3 V, fully differential, 600-Ω load		3.5		mW
Maximum output current	600-Ω load		3.5		mA

5.11 Bias Amplifier Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage			1.35/2.35		V
Integrated noise	300 Hz–13 kHz		20		μV
Offset voltage			10		mV
Current drive			5		mA
Unity gain bandwidth			1		MHz
DC gain			90		dB
PSRR			70		dB

5.12 Power-Supply Rejection (see Note 9)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV_{DD}	Supply-voltage rejection ratio, analog supply (f_i = 0 to f_S/2) at 1 kHz	Differential		75		dB

NOTE 9: Power supply rejection measurements are made with both the ADC and DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

5.13 Current Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC channel (single channel)			1.7		mA
DAC channel (single channel)	Without drivers		1.1		
Speaker driver	No signal		2.8		
Handset driver	No signal		0.6		
Headset driver	No signal		0.6		
Lineout driver	No signal		0.6		
Reference			0.7		
Digital	Coarse sampling		1.9		
	Fine sampling		3.0		
Total analog with all sections on	No signal		10.9		

5.14 Power Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC channel (single channel)			5.7		mW
DAC channel (single channel)	Without drivers		3.5		
Speaker driver	No signal		9.3		
Handset driver	No signal		2.0		
Headset driver	No signal		2.0		
Lineout driver	No signal		2.0		
Reference			2.3		
Digital	Coarse sampling		3.4		
	Fine sampling		5.5		
Total analog with all sections on	No signal		35.8		

5.15 Power-Down Current

PARAMETER	MIN	TYP	MAX	UNIT
Hardware power-down current (no clock)		1		µA
Software power-down analog current		2		

5.16 LCD DAC

	MIN	TYP	MAX	UNIT
Output range	0.35		2.35	V
Sampling rate			104	kHz
INL		±0.5		LSB
DNL		±0.25		LSB
Offset voltage		±25		mV
Gain error		±0.02		dB

5.17 Timing Requirements (see Parameter Measurement Information)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{wH}	Pulse duration, MCLK high	C_L = 20 pF	5			ns
t_{wL}	Pulse duration, MCLK low		5			
t_{su1}	Setup time, $\overline{\text{RESET}}$, before MCLK high (see Figure 5–1)		3			
t_{h1}	Hold time, $\overline{\text{RESET}}$, after MCLK high (see Figure 5–1)		2			
t_{d1}	Delay time, SCLK↑ to FS/FSD↓				5	
t_{d2}	Delay time, SCLK↑ to FS/FSD↑				5	
t_{d3}	Delay time, SCLK↑ to DOUT				15	
t_{en}	Enable time, SCLK↑ to DOUT				15	
t_{dis}	Disable time, SCLK↑ to DOUT				15	
t_{su2}	Setup time, DIN, before SCLK↓		10			
t_{h2}	Hold time, DIN, after SCLK↓		10			

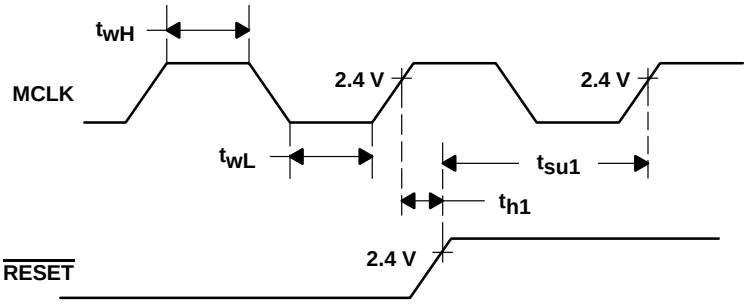


Figure 5–1. Hardware Reset Timing

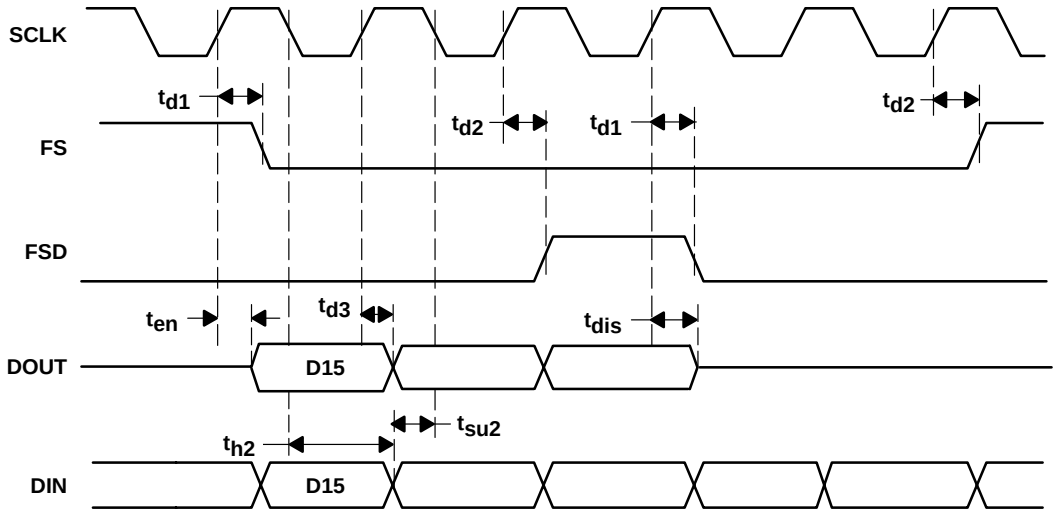


Figure 5–2. Serial Communication Timing

NOTE: Above Figures are meant to show timing delays only.

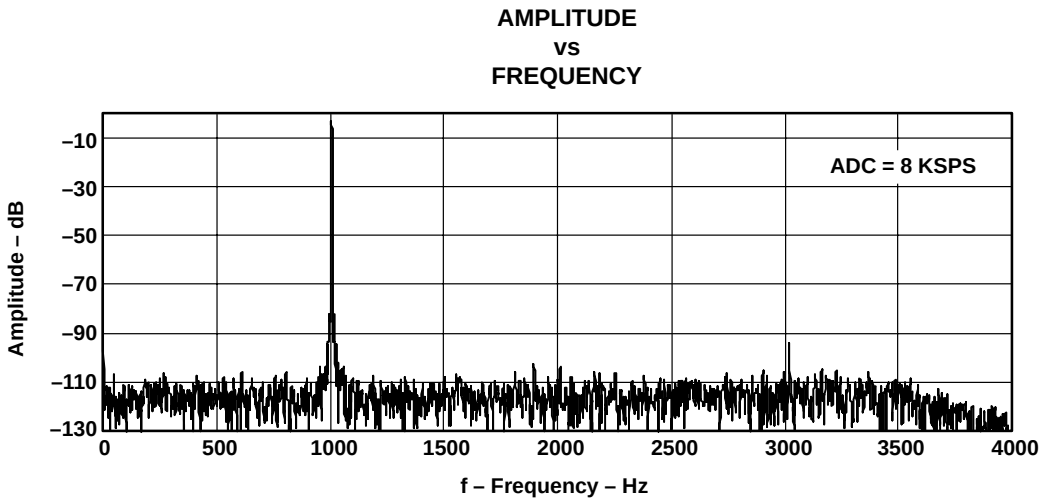


Figure 5–3. FFT—ADC Channel (–3 dB input)

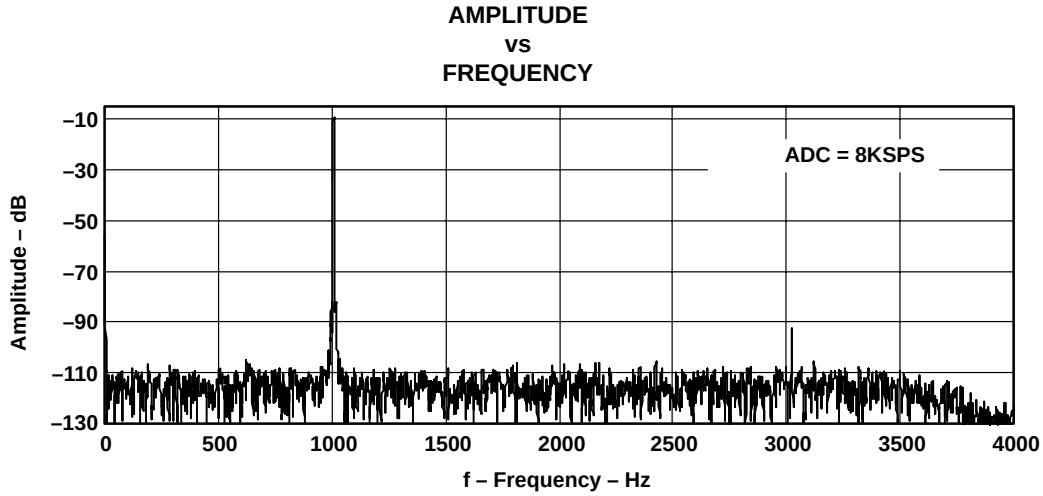


Figure 5–4. FFT—ADC Channel (–9 dB input)

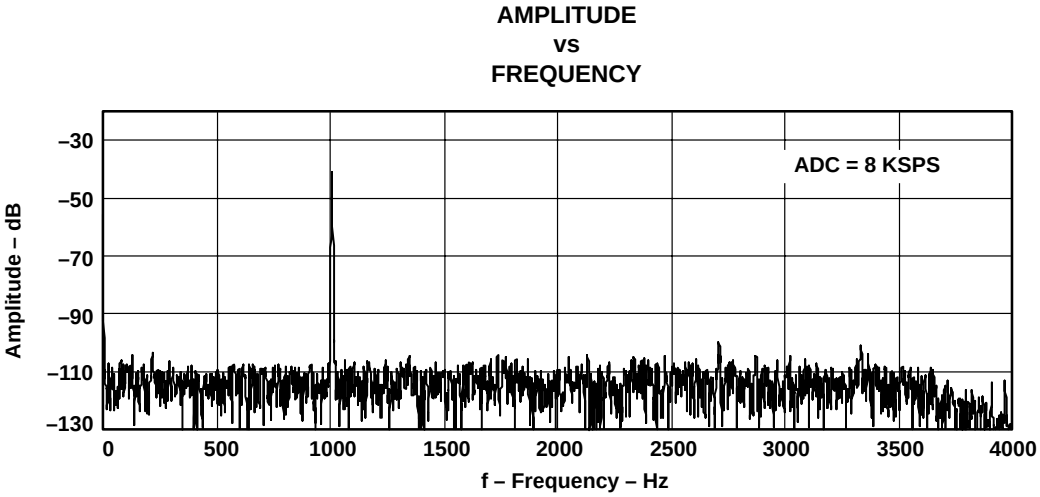


Figure 5–5. FFT—ADC Channel (–40 dB input)

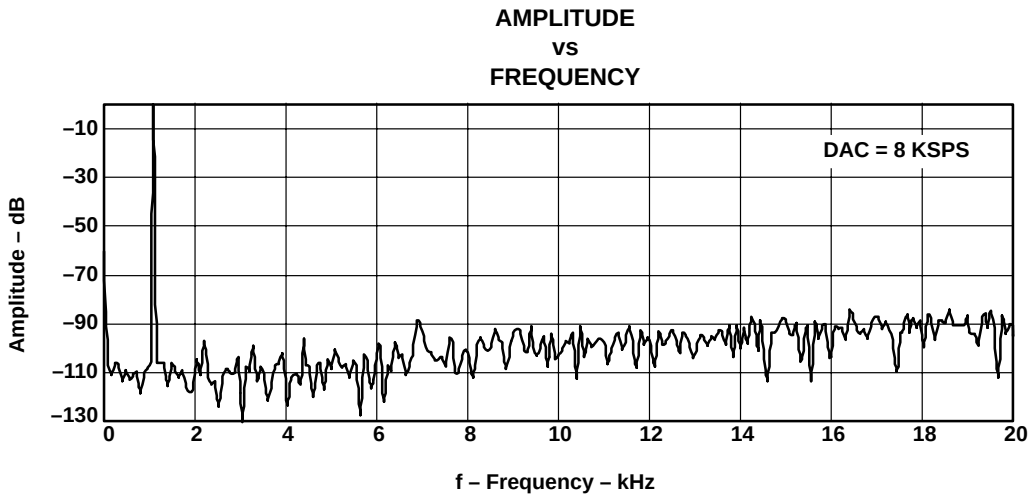


Figure 5–6. FFT—DAC Channel (0 dB input)

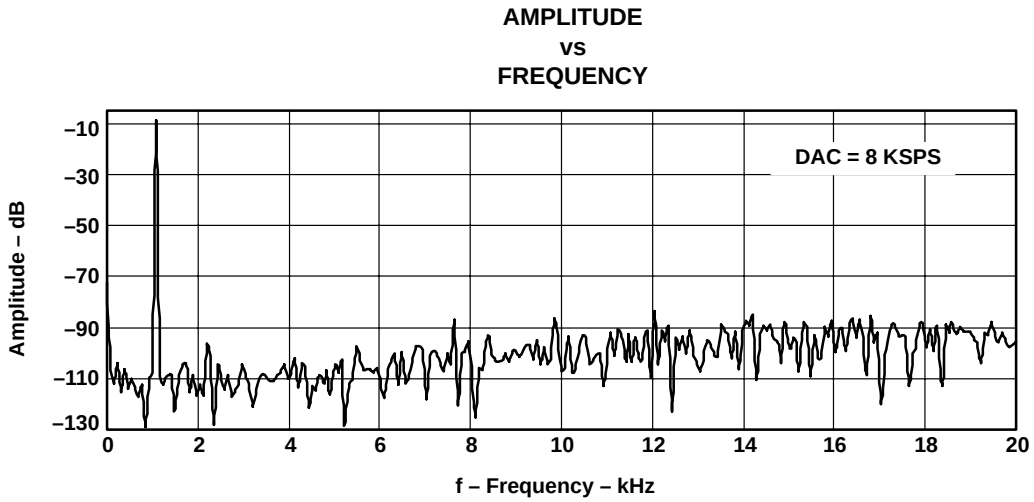


Figure 5–7. FFT—DAC Channel (–9 dB input)

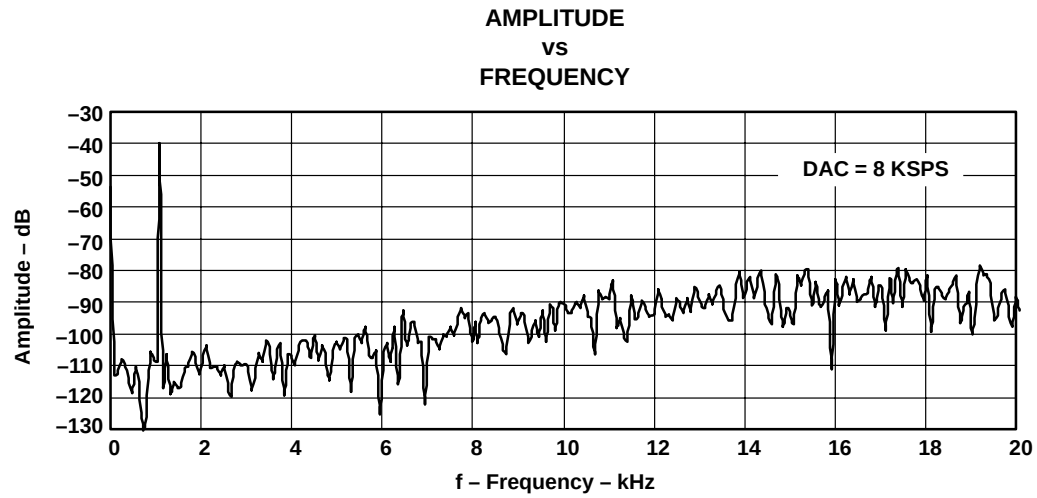


Figure 5–8. FFT—DAC Channel (40 dB input)

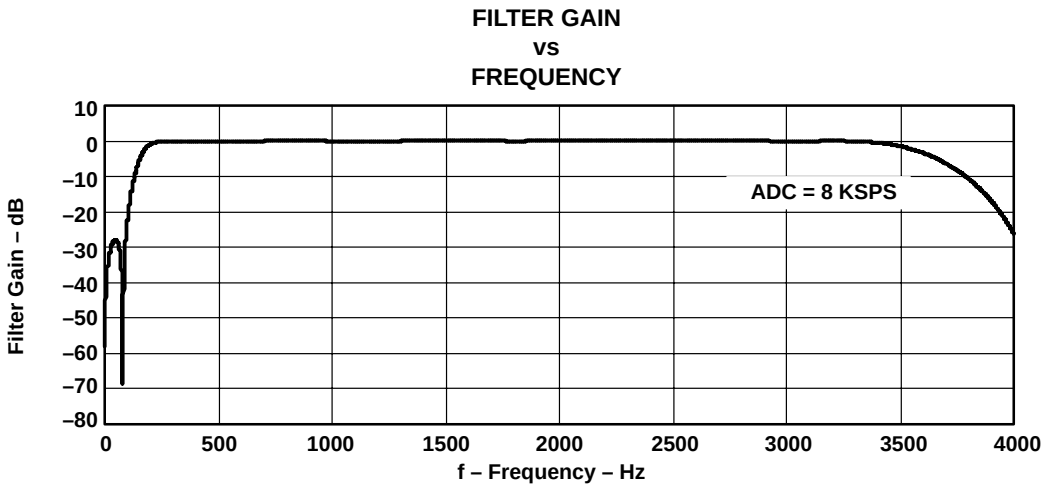


Figure 5–9. ADC FIR Frequency Response – HPF On

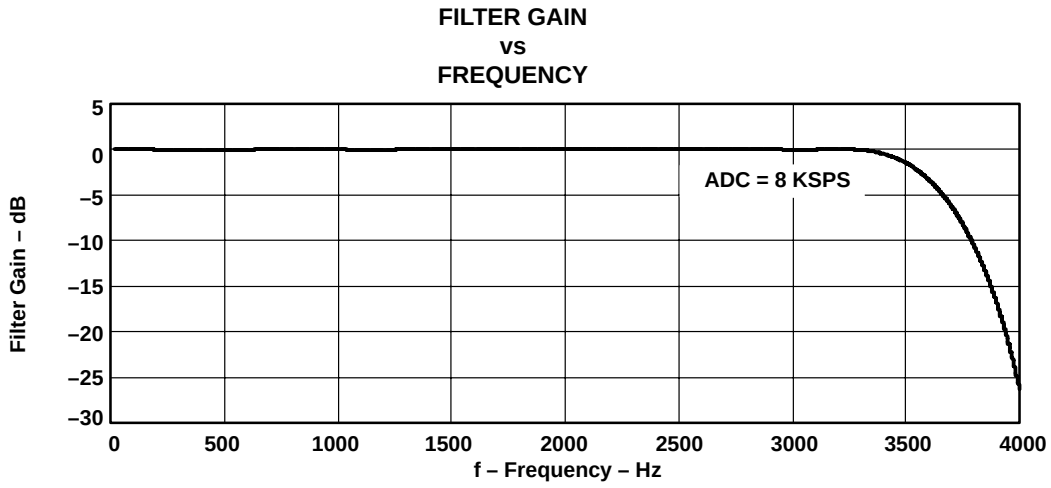


Figure 5–10. ADC FIR Frequency Response – HPF Off

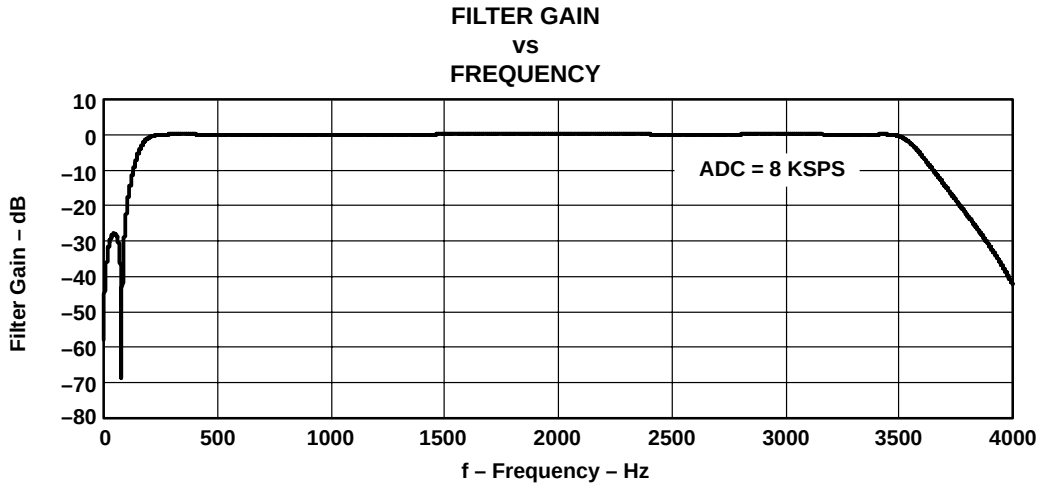


Figure 5–11. ADC IIR Frequency Response –HPF On

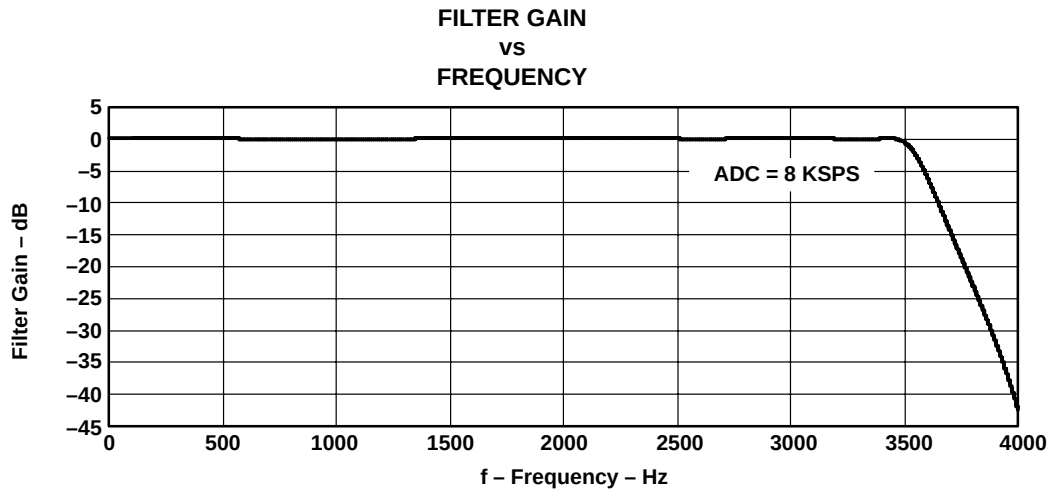


Figure 5–12. ADC IIR Frequency Response – HPF Off

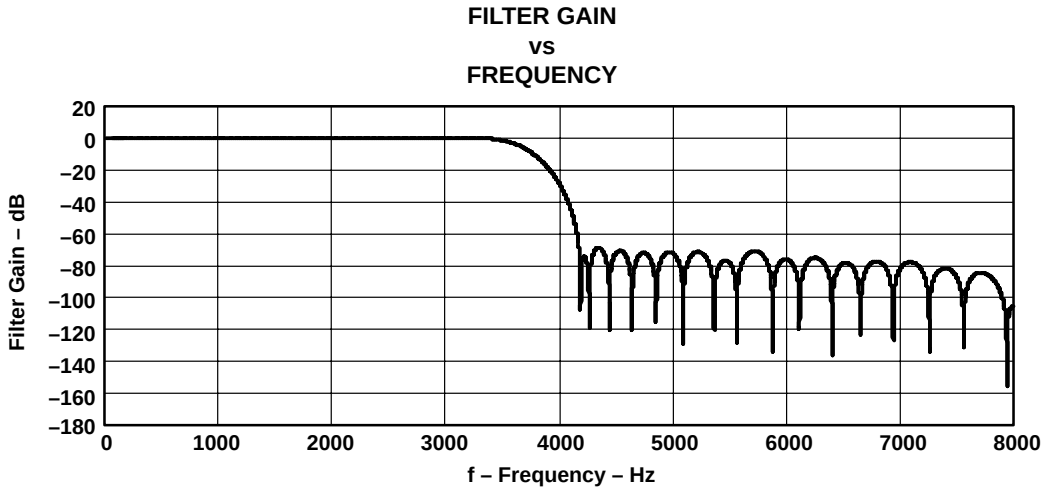


Figure 5–13. DAC FIR Frequency Response (OSR = 128)

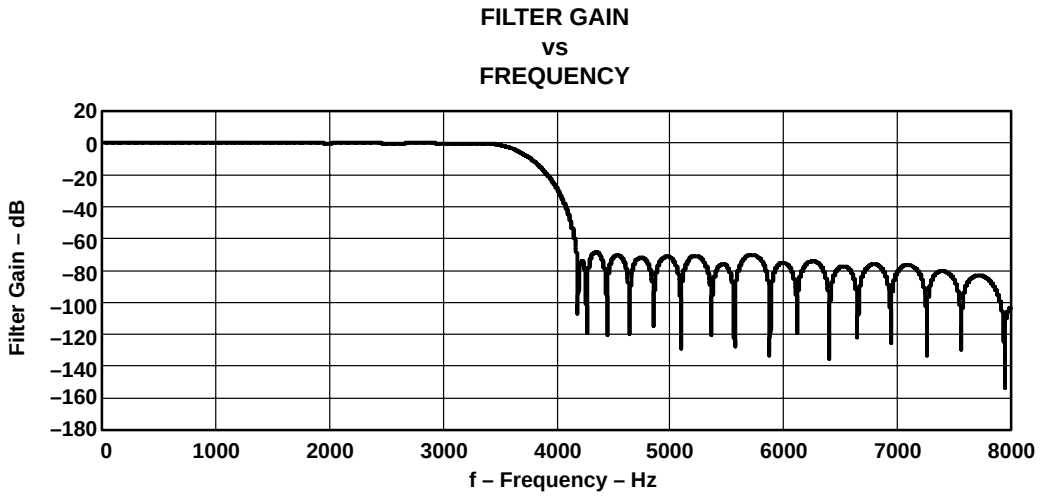


Figure 5–14. DAC FIR Frequency Response (OSR = 256)

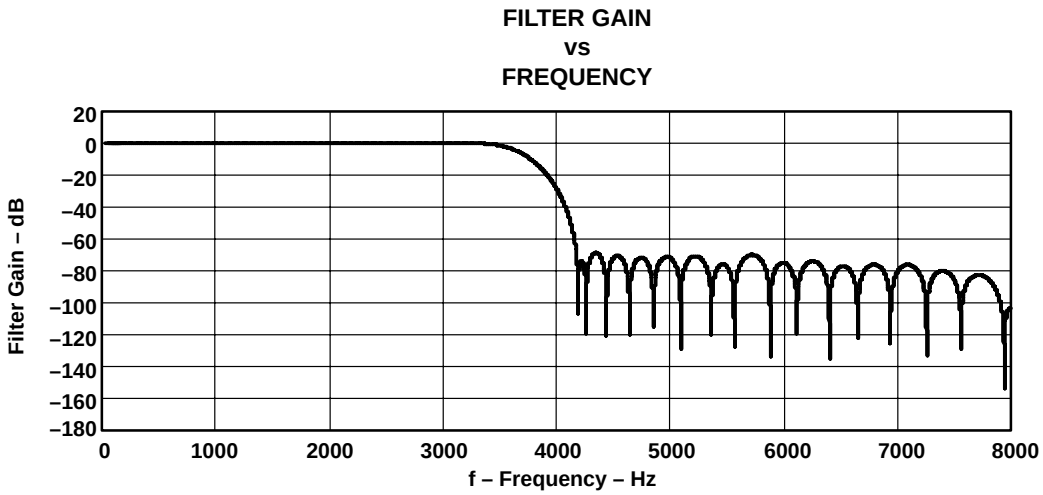


Figure 5–15. DAC FIR Frequency Response (OSR = 512)

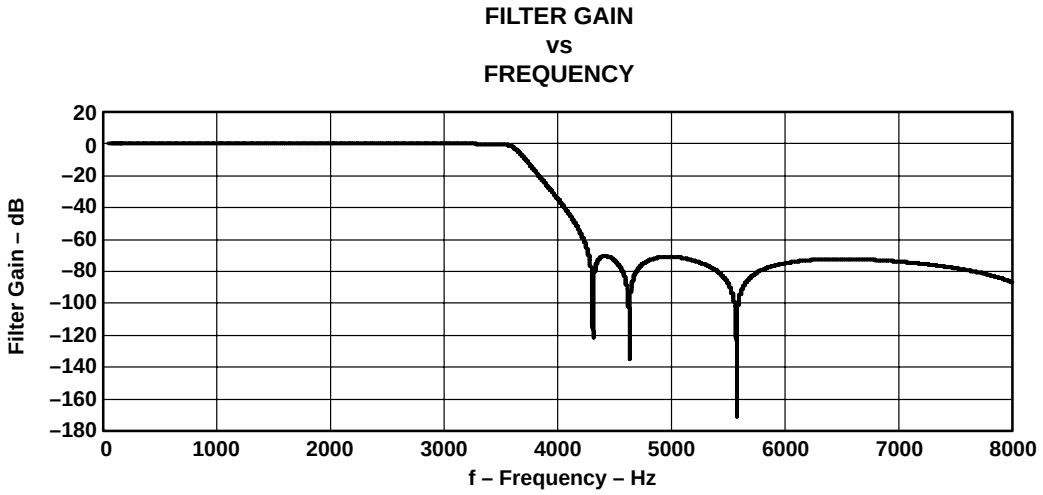


Figure 5–16. DAC IIR Frequency Response (OSR = 128)

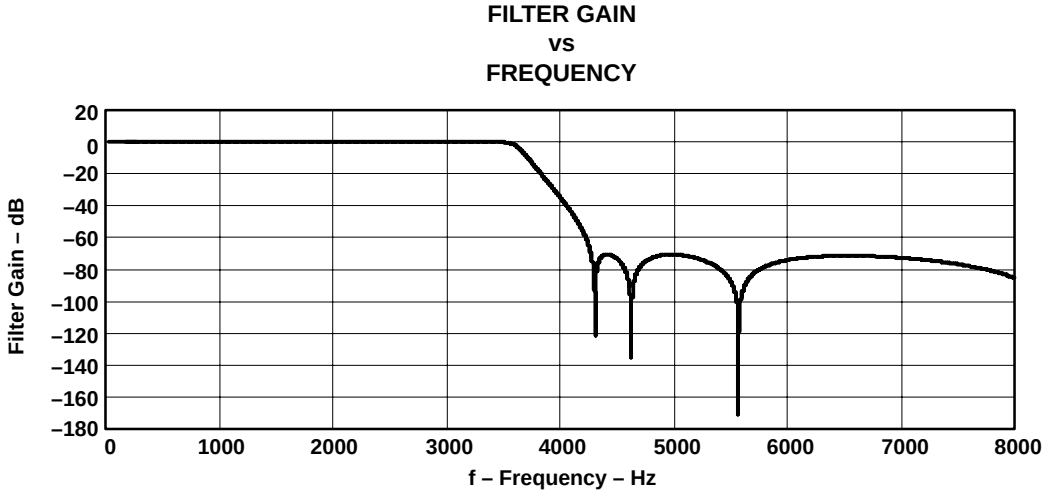


Figure 5–17. DAC IIR Frequency Response (OSR = 256)

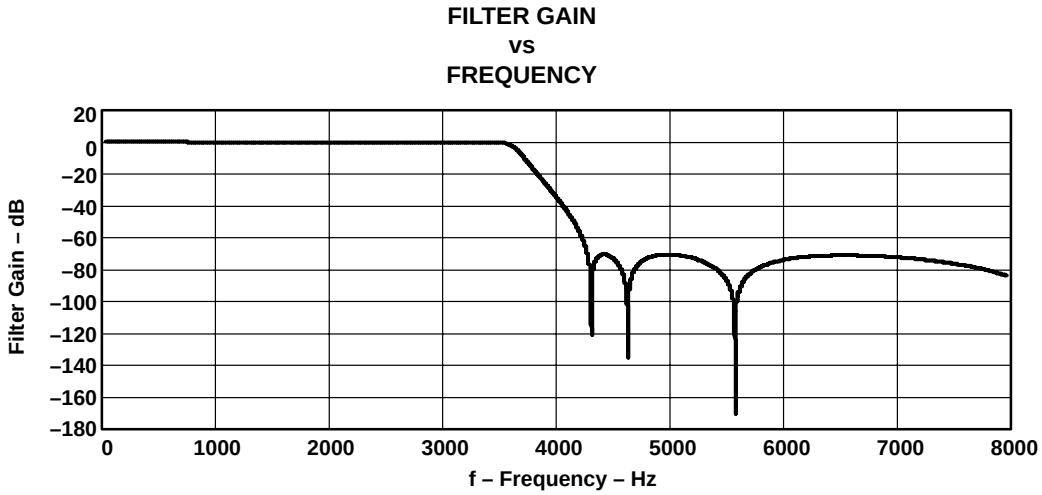


Figure 5–18. DAC IIR Frequency Response (OSR = 512)

5.18 Layout and Grounding Guidelines for TLV320AIC20

TLV320AIC20 has a built-in analog antialias filter, which provides rejection to external noise at high frequencies that may couple into the device. Digital filters with high out-of-band attenuation also reject the external noise. If the differential inputs are used for the ADC channel, then the noise in the common-mode signal is also rejected by the high CMRR of TLV320AIC20. Using external common-mode for microphone inputs also helps reject the external noise. However to extract the best performance from TLV320AIC20, care must be taken in board design and layout to avoid coupling of external noise into the device.

TLV320AIC20 supports clock frequencies as high as 100 MHz. To avoid coupling of fast switching digital signals to analog signals, the digital and analog sections should be separated on the board. In TLV320AIC20 the digital and analog pins are kept separated to aid such a board layout. A separate analog ground plane must be used for the analog section of the board. The analog and digital ground planes should be shorted at only one place as close to TLV320AIC20 as possible. No digital trace should run under TLV320AIC20 to avoid coupling of external digital noise into the device. It is suggested to have the analog ground plane running below the TLV320AIC20. The power-supplies must be decoupled close to the supply pins, preferably, with 0.1 μF ceramic capacitor and 10 μF tantalum capacitor following. The ground pin must be connected to the ground plane as close as possible to the TLV320AIC20, so as to minimize any inductance in the path. Since the MCLK is expected to be a very high frequency signal, it is advisable to shield it with digital ground. For best performance of ADC in differential input mode, the differential signals must be routed close to each other in similar fashion, so that the noise coupling on both the signals is the same and can be rejected by the device.

Extra care has to be taken for the speaker driver outputs, as any trace resistance can cause a reduction in the maximum swing that can be seen at the speaker.

5.19 TLV320AIC20-to-DSP Interface

The TLV320AIC20 interfaces gluelessly to the McBSP port of a C54x or C6x TI DSP. Figure 5–19 shows a single TLV320AIC20 connected to a C54x or C6x TI DSP.

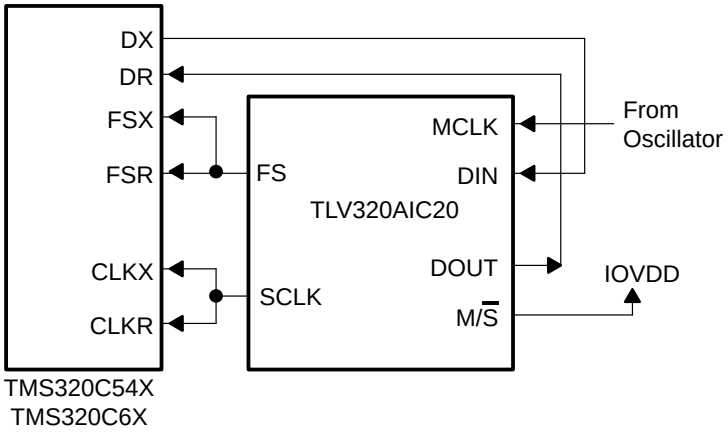


Figure 5–19. TLV320AIC20s Interface to McBSP Port of C54x or C6x DSP

5.20 Hybrid Circuit External Connections

The TLV320AIC20 connected to the telephone line using the LINEI and LINEO hybrid circuit is shown in Figure 5–20.

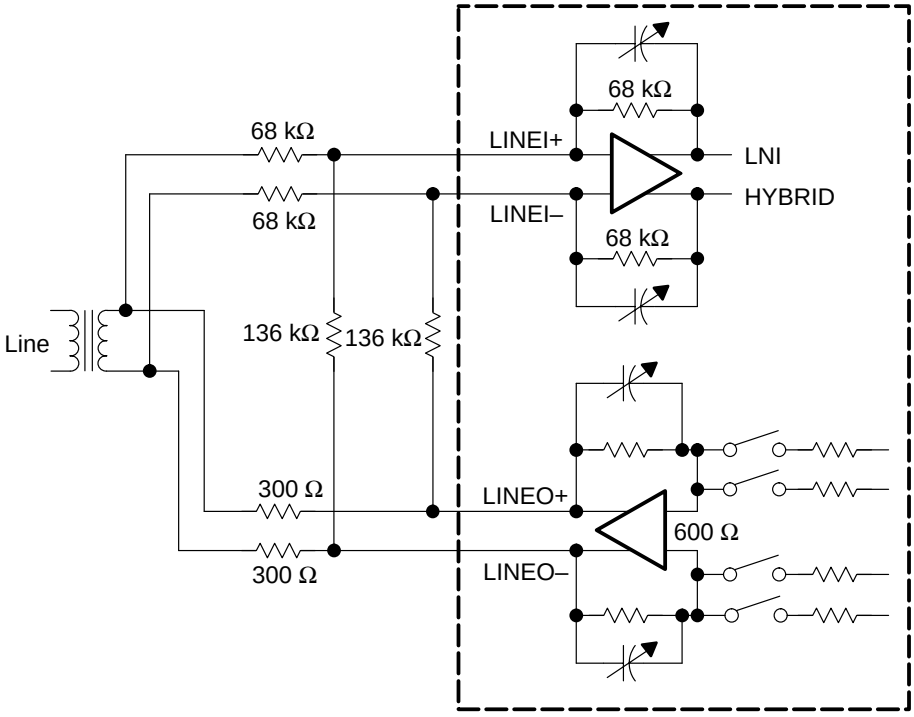


Figure 5–20. Hybrid Circuit External Connections

5.21 Microphone, Handset, and Headset External Connections

The microphone, headset, and handset external connections are shown in Figure 5–21. The suggested discrete components with their values also are included.

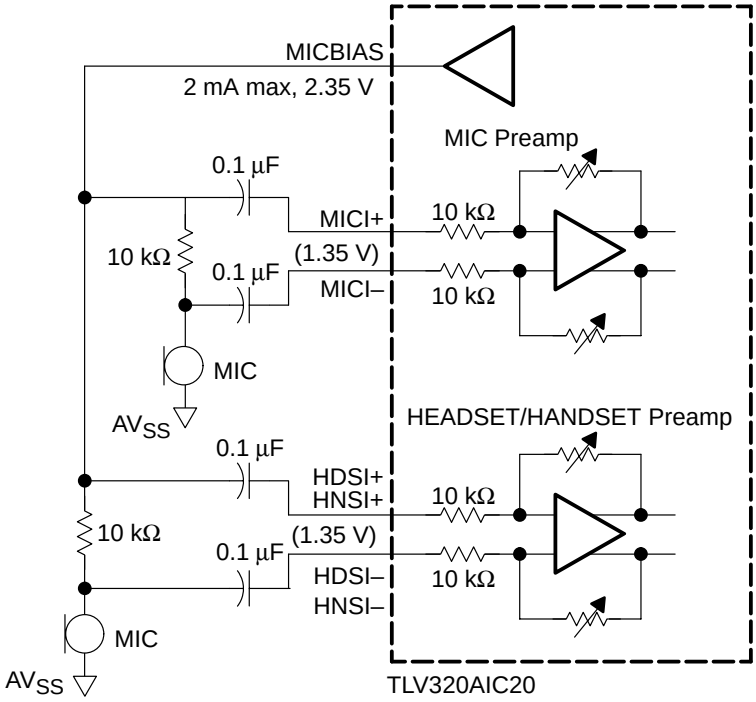


Figure 5–21. MIC/Handset/Headset External Connections

5.22 CallerID Interface

The callerID amplifier interface to the telephone line is shown in Figure 5–22.

The value for Rx is 365 kΩ (E96 series, which has 1% tolerance). Cx is 470 pF (10% tolerance) of high-voltage rating. Voltage rating is decided based on the telecom standards of the country. The typical value is 1 kV. The callerID input can be used as a lower-performance line input. For this application, a larger value capacitor is required for Cx.

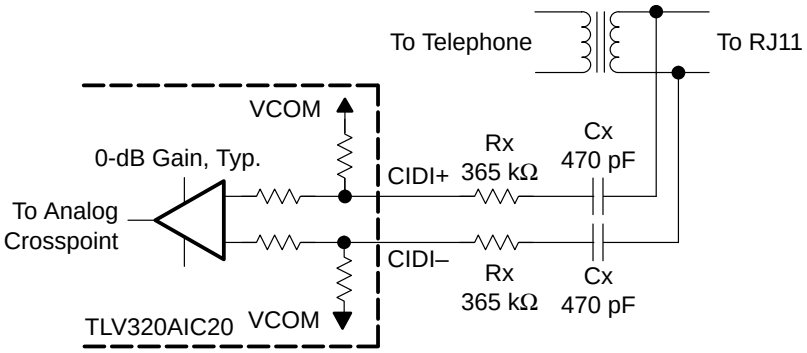
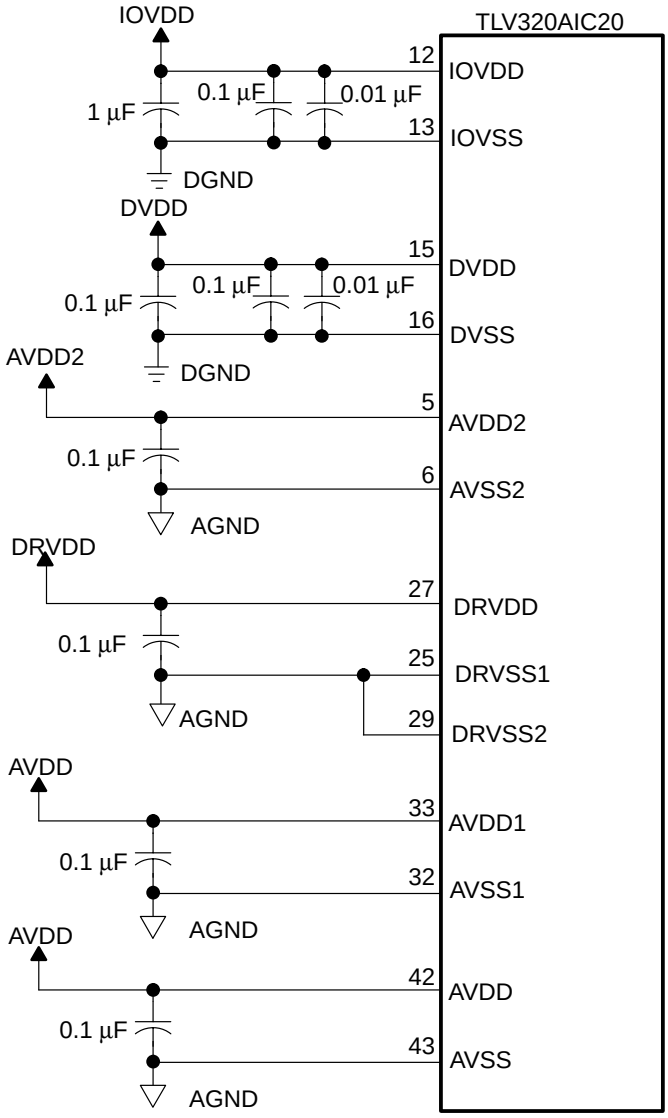


Figure 5–22. Typical Application Circuit for CallerID Amplifiers

5.23 Recommended Power-Supply Decoupling

The recommended power-supply decoupling for the TLV320AIC20 is shown in Figure 5–23. Both high frequency and bulk decoupling capacitors are suggested. The high-frequency capacitors should be X7R type capacitors or better. A 1-μF ceramic capacitor should be used to decouple the digital power supply.



DVDD = Digital Power
DGND = Digital Ground

AVDD/AVDD1/AVDD2= Analog Power
AGND = Analog Ground

DRVDD = Separate Analog Power

Figure 5–23. Recommended Decoupling

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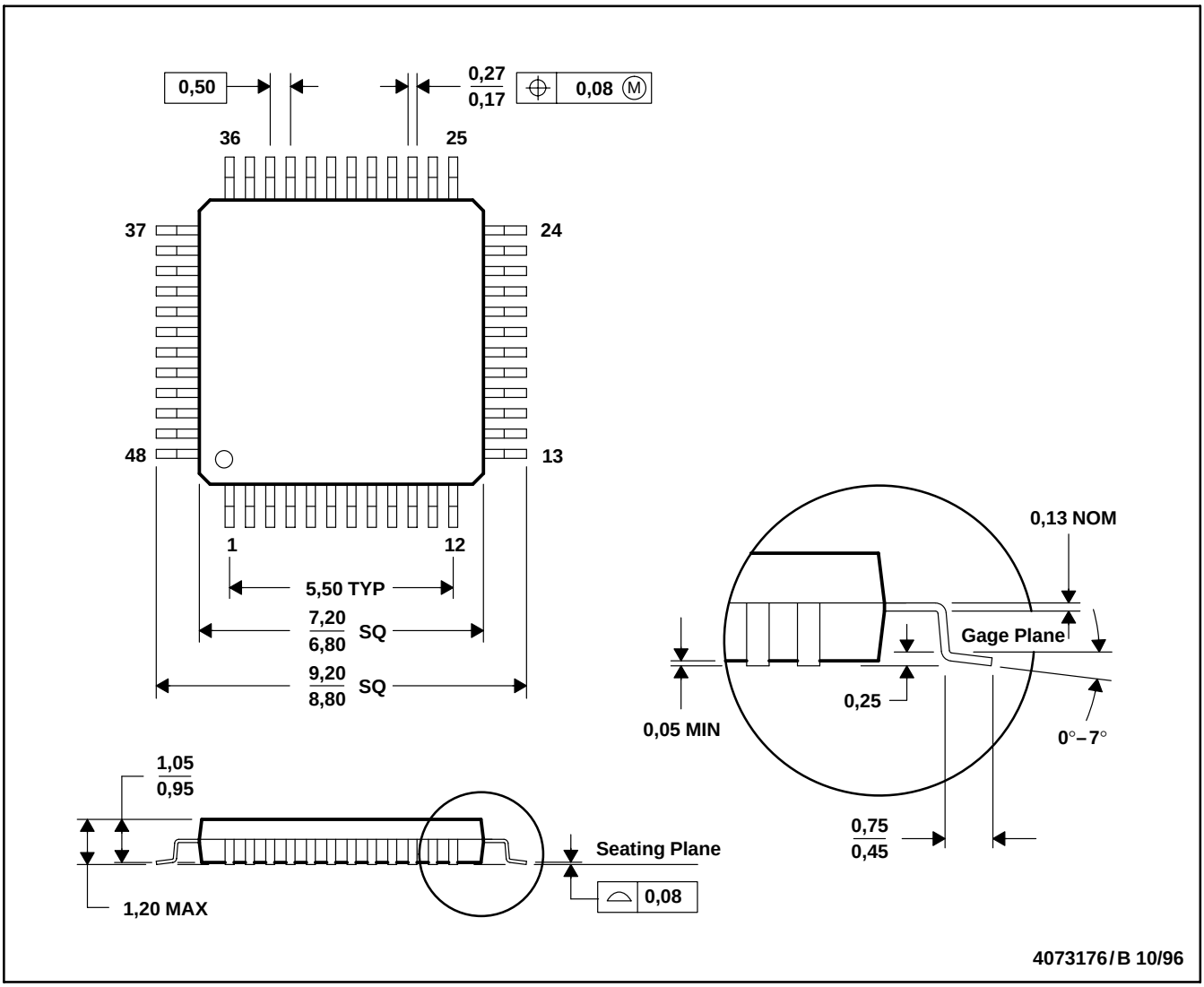
6 Mechanical Information

PFB (S-PQFP-G48) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026