TPS62000, TPS62001, TPS62002, TPS62003
TPS62004, TPS62005, TPS62006, TPS62007, TPS62008
HIGH-EFFICIENCY STEP-DOWN LOW POWER DC-DC CONVERTER

SLVS294C − SEPTEMBER 2000 − REVISED SEPTEMBER 2003

FEATURES

- **High-Efficiency Synchronous Step-Down Converter With Greater Than 95% Efficiency**
- **2 V to 5.5 V Operating Input Voltage Range**
- **Adjustable Output Voltage Range From 0.8 V to V_I**
- **Fixed Output Voltage Options Available in 0.9 V, 1 V, 1.2 V, 1.5 V, 1.8 V, 1.9 V, 2.5 V, and 3.3 V**
- **Synchronizable to External Clock Signal up to 1 MHz**
- **Up to 600 mA Output Current**
- **Pin-Programmable Current Limit**
- **High Efficiency Over a Wide Load Current Range in Power Save Mode**
- **100% Maximum Duty Cycle for Lowest Dropout**
- **Low-Noise Operation Antiringing Switch and PFM/PWM Operation Mode**
- **Internal Softstart**
- **50-µA Quiescent Current (TYP)**
- **Available in the 10-Pin Microsmall Outline Package (MSOP)**
- **Evaluation Module Available**
- **Available in a Ultra-Small, 12-Pin NanoStar™ (Wafer Chip-Scale) Package**

APPLICATIONS

- **Low-Power CPUs and DSPs**
- **Cellular Phones**
- **Organizers, PDAs, and Handheld PCs**
- **MP-3 Portable Audio Players**
- **Digital Cameras**
- **USB-Based DSL Modems and Other Network Interface Cards**

description

The TPS6200x devices are a family of low-noise synchronous step-down dc-dc converters that are ideally suited for systems powered from a 1-cell Li-ion battery or from a 2- to 3-cell NiCd, NiMH, or alkaline battery. The TPS6200x operates typically down to an input voltage of 1.8 V, with a specified minimum input voltage of 2 V.

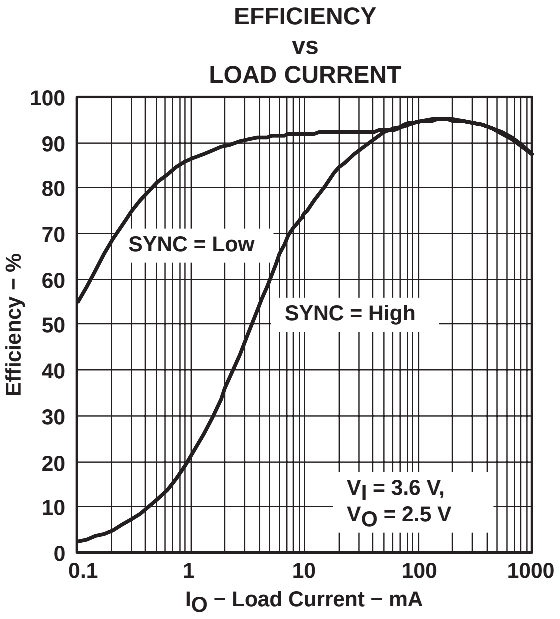
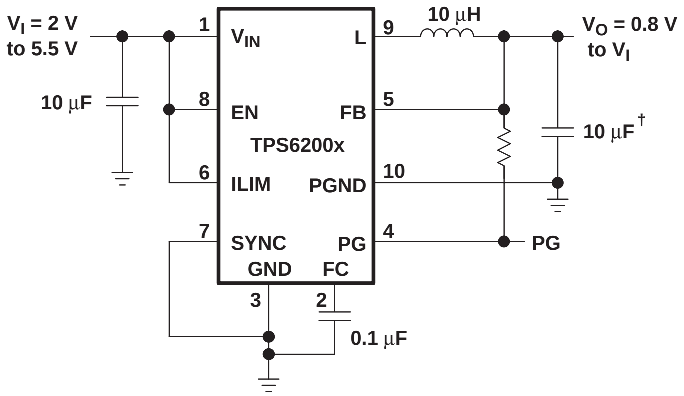


Figure 1



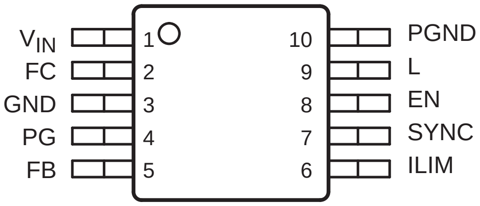
† With $V_O \geq 1.8$ V; C_O = 10 µF, $V_O < 1.8$ V; C_O = 47 µF

Figure 2. Typical Application Circuit for Fixed Output Voltage Option

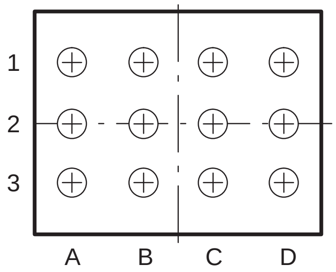
description (continued)

The TPS6200x is a synchronous current-mode PWM converter with integrated N- and P-channel power MOSFET switches. Synchronous rectification is used to increase efficiency and to reduce external component count. To achieve the highest efficiency over a wide load current range, the converter enters a power-saving pulse-frequency modulation (PFM) mode at light load currents. Operating frequency is typically 750 kHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500 kHz to 1 MHz. For low-noise operation, the converter can be operated in the PWM mode and the internal antiringing switch reduces noise and EMI. In the shutdown mode, the current consumption is reduced to less than 1 μA. The TPS6200x is available in the 10-pin (DGS) microsmall outline package (MSOP). The TPS62000 is also available in a 12-pin, 1,85 mm x 1,3 mm NanoStar™ chip scale package (YEG). The devices operate over a free-air temperature range of −40°C to 85°C.

MSOP (DGS) PACKAGE
(TOP VIEW)



YEG PACKAGE
(BOTTOM VIEW)

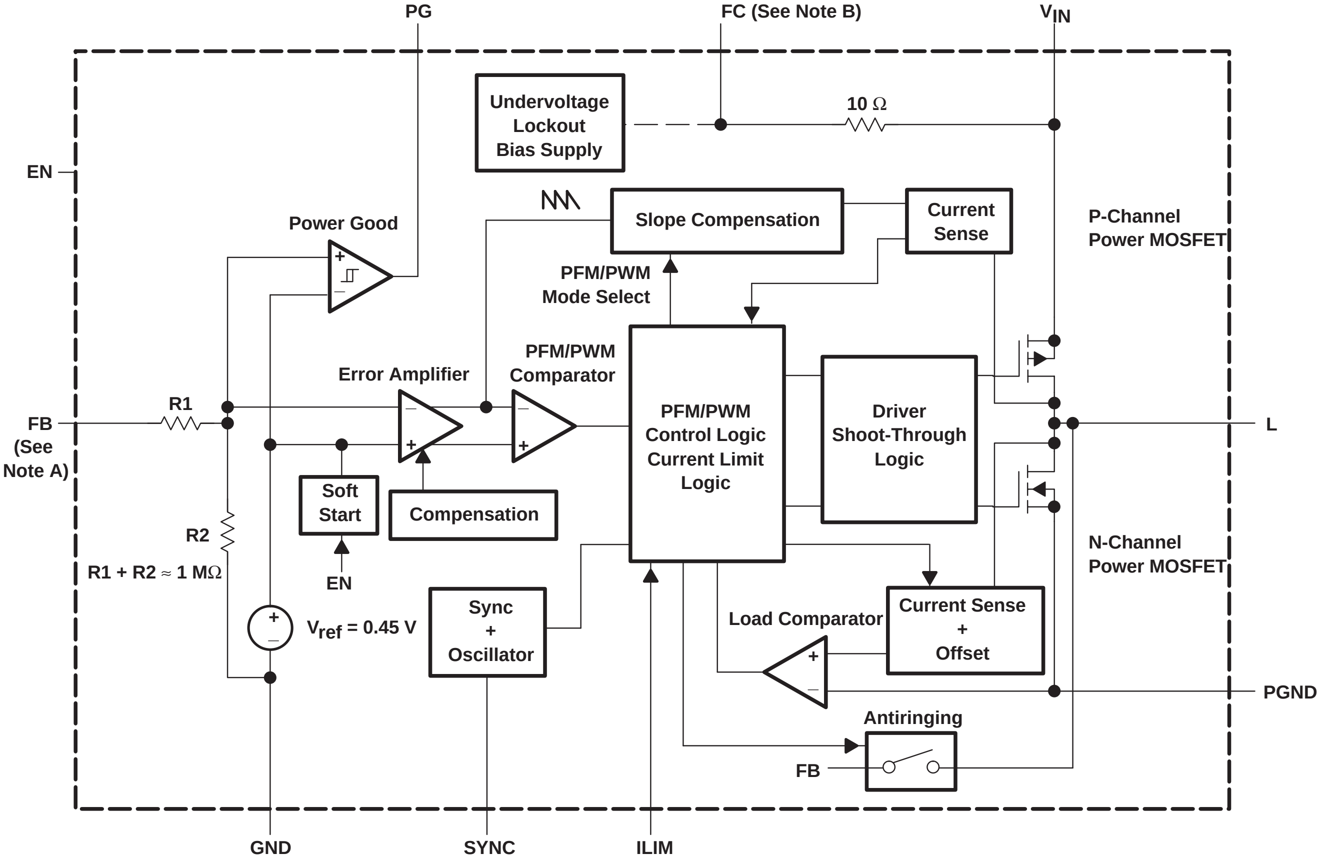


AVAILABLE OPTIONS

T_A	VOLTAGE OPTIONS	PACKAGE		MARKING	
		MSOP[†]	WCSP[‡]	DGS	YEG
−40°C to 85°C	Adjustable	TPS62000DGS	TPS62000YEG	AIH	TPS62000
	0.9 V	TPS62001DGS		AII	
	1 V	TPS62002DGS		AIJ	
	1.2 V	TPS62003DGS		AIK	
	1.5 V	TPS62004DGS		AIL	
	1.8 V	TPS62005DGS		AIM	
	1.9 V	TPS62008DGS		AJI	
	2.5 V	TPS62006DGS		AIN	
	3.3 V	TPS62007DGS		AIO	

[†] Without the suffix indicates deliveries in tubes of 80 units.
[‡] The YEG package is available taped and reeled. Add R suffix to device type (e.g. TPS62000YEGR) to order 3000 devices per reel. Add T sufix to device type (e.g., TPS62000YEGT) to order 250 devices per reel.

functional block diagram



NOTES: A. The adjustable output voltage version does not use the internal feedback resistor divider. The FB pin is directly connected to the error amplifier.

B. Do not connect the FC pin to an external power source

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. DGS	NO. YEG		
EN	8	B3	I	Enable. A logic high enables the converter, logic low forces the device into shutdown mode reducing the supply current to less than 1 µA.
FB	5	A2	I	Feedback pin for the fixed output voltage option. For the adjustable version an external resistive divider is connected to FB. The internal voltage divider is disabled for the adjustable version.
FC	2	C1		Supply bypass pin. A 0.1 µF coupling capacitor should be connected as close as possible to this pin for good high frequency input voltage supply filtering.
GND	3	A1		Ground
ILIM	6	A3	I	Switch current limit. Connect ILIM to GND to set the switch current limit to typically 600 mA, or connect this pin to V_{IN} to set the current limit to typically 1200 mA.
L	9	C2, C3	I/O	Connect the inductor to this pin. L is the switch pin connected to the drain of the internal power MOSFETS.
PG	4	B1	O	Power good comparator output. This is an open-drain output. A pullup resistor should be connected between PG and V_O. The output goes active high when the output voltage is greater than 92% of the nominal value.
PGND	10	D2		Power ground. Connect all power grounds to PGND.
SYNC	7	D3	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level: SYNC = HIGH: Low-noise mode enabled, fixed frequency PWM operation is forced SYNC = LOW (GND): Power save mode enabled, PFM/PWM mode enabled.
V_{IN}	1	D1	I	Supply voltage input
NC		B2		Not connected

detailed description

operation

The TPS6200x is a step down converter operating in a current mode PFM/PWM scheme with a typical switching frequency of 750 kHz.

At moderate to heavy loads, the converter operates in the pulse width modulation (PWM) and at light loads the converter enters a power save mode (pulse frequency modulation) to keep the efficiency high.

In the PWM mode operation, the part operates at a fixed frequency of 750 kHz. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The high side switch is turned off when the sensed current causes the PFM/PWM comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set by ILIM). After a minimum dead time preventing shoot through current, the low side N-channel MOSFET is turned on and the current ramps down again. As the clock cycle is completed, the low side switch is turned off and the next clock cycle starts.

In discontinuous conduction mode (DCM), the inductor current ramps to zero before the end of each clock cycle. In order to increase the efficiency the load comparator turns off the low side MOSFET before the inductor current becomes negative. This prevents reverse current flowing from the output capacitor through the inductor and low side MOSFET to ground that would cause additional losses.

As the load current decreases and the peak inductor current does not reach the power save mode threshold of typically 120 mA for more than 15 clock cycles, the converter enters a pulse frequency modulation (PFM) mode.

operation (continued)

In the PFM mode, the converter operates with:

- Variable frequency
- Constant peak current that reduces switching losses
- Quiescent current at a minimum

Thus maintaining the highest efficiency at light load currents. In this mode, the output voltage is monitored with the error amplifier. As soon as the output voltage falls below the nominal value, the high side switch is turned on and the inductor current ramps up. When the inductor current reaches the peak current of typical: 150 mA + 50 mA/V x ($V_I - V_O$), the high side switch turns off and the low side switch turns on. As the inductor current ramps down, the low side switch is turned off before the inductor current becomes negative which completes the cycle. When the output voltage falls below the nominal voltage again, the next cycle is started.

The converter enters the PWM mode again as soon as the output voltage can not be maintained with the typical peak inductor current in the PFM mode.

The control loop is internally compensated reducing the amount of external components.

The switch current is internally sensed and the maximum current limit can be set to typical 600 mA by connecting ILIM to ground or to typically 1.2 A connecting ILIM to V_{IN}.

100% duty cycle operation

As the input voltage approaches the output voltage and the duty cycle exceeds typical 95%, the converter turns the P-channel high side switch continuously on. In this mode, the output voltage is equal to the input voltage minus the voltage drop across the P-channel MOSFET.

synchronization, power save mode and forced PWM mode

If no clock signal is applied, the converter operates with a typical switching frequency of 750 kHz. It is possible to synchronize the converter to an external clock within a frequency range from 500 kHz to 1000 kHz. The device automatically detects the rising edge of the first clock and is synchronizes immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation without interruption. The switch over is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 8 µs in case the internal clock has a minimum frequency of 500 kHz.

In case the device is synchronized to an external clock, the power save mode is disabled and the device stays in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power save mode. The converter operates in the PWM mode at moderate to heavy loads and in the PFM mode during light loads maintaining high efficiency over a wide load current range.

Connecting the SYNC pin to the V_{IN} pin forces the converter to operate permanently in the PWM mode even at light or no load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads (see Figure 1).

It is possible to switch from forced PWM mode to the power save mode during operation.

The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS6200x to the specific system requirements.

low noise antiringing switch

An *antiringing* switch is implemented in order to reduce the EMI radiated from the converter during discontinuous conduction mode (DCM). In DCM, the inductor current ramps to zero before the end of each switching period. The internal load comparator turns off the low side switch at that instant thus preventing the current flowing backward through the inductance which increases the efficiency. An antiringing switch across the inductor prevents parasitic oscillation caused by the residual energy stored in the inductance (see Figure 12).

NOTE:

The *antiringing* switch is only activated in the fixed output voltage versions. It is not enabled for the adjustable output voltage version TPS62000.

soft start

As the enable pin (EN) goes high, the soft-start function generates an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typical 1 ms (see Figure 13). When the soft-start function is completed, the error amplifier is connected directly to the internal voltage reference.

enable

Logic low on EN forces the TPS6200x into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 1 µA in the shutdown mode.

undervoltage lockout

An undervoltage lockout circuit provides the save operation of the device. It prevents the converter from turning on when the voltage on V_{IN} is less than typically 1.6 V

power good comparator

The power good (PG) comparator has an open drain output capable of sinking typically 10 µA. The PG is only active when the device is enabled (EN = high). When the device is disabled (EN = low), the PG pin is high impedance.

The PG output is only valid after a 100 µs delay after the device is enabled and the supply voltage is greater than 1.2 V. This is only important in cases where the pullup resistor of the PG pin is connected to an external voltage source which might cause an initial spike (false high signal) within the first 100 µs after the input voltage exceeds 1.2 V. This initial spike can be filtered with a small R-C filter to avoid false power good signals during start-up.

If the PG pin is connected to the output of the TPS62000 with a pullup resistor, no initial spike (false high signal) occurs and no precautions have to be taken during start-up.

The PG pin becomes active high when the output voltage exceeds typically 94.5% of its nominal value. Leave the PG pin unconnected when not used.

no load operation

In case the converter operates in the forced PWM mode and there is no load connected to the output, the converter will regulate the output voltage by allowing the inductor current to reverse for a short period of time.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltages on pin V_{IN} and FC (see Note 1)	−0.3 V to 6 V
Voltages on pins EN, ILIM, SYNC, PG, FB, L (see Note 1)	−0.3 V to V_{IN} + 0.3 V
Peak switch current	1.6 A
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
10 pin MSOP	555 mW	5.56 mW/°C	305 mW	221 mW
12 pin YEG	588 mW	5.87 mW/°C	324 mW	235mW

NOTE: The thermal resistance junction to ambient of the 10-pin MSOP is 180°C/W. The thermal resistance junction to ambient of the 12-pin YEG is 170°C/W and $R_{\theta JC}$ = 21°C/W. The device will not run into thermal limitations provided it is operated within the specified range.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_I	2		5.5	V
Output voltage range for adjustable output voltage version, V_O	0.8		V_I	V
Output current for 3-cell operation, I_O ($V_I \ge 2.5$ V; L = 10 µH, f = 750 kHz)			600	mA
Output current for 2-cell operation, I_O ($V_I \ge 2$ V; L = 10 µH, f = 750 kHz)			200	mA
Inductor, L (see Note 2)		10		µH
Input capacitor, C_i (see Note 2)	10			µF
Output capacitor, C_o (see Note 2) $V_O \ge 1.8$ V)	10			µF
Output capacitor, C_o (see Note 2) $V_O < 1.8$ V)	47			µF
Operating ambient temperature, T_A	-40		85	°C
Operating junction temperature, T_J	-40		125	°C

NOTE 2: Refer to application section for further information.

electrical characteristics over recommended operating free-air temperature range, V_I = 3.6 V, V_O = 2.5 V, I_O = 300 mA, EN = V_{IN}, ILIM = V_{IN}, T_A = −40°C to 85°C (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range	I_O = 0 mA to 600 mA	2.5		5.5	V
		I_O = 0 mA to 200 mA	2		5.5	
$I_{(Q)}$	Operating quiescent current	I_O = 0 mA, SYNC = GND (PFM-mode enabled)		50	75	µA
$I_{(SD)}$	Shutdown current	EN = GND		0.1	1	µA

enable

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	EN high-level input voltage		1.3			V
V_{IL}	EN low level input voltage				0.4	V
I_{lkg}	EN input leakage current	EN = GND or V_{IN}		0.01	0.1	µA
$V_{(UVLO)}$	Undervoltage lockout threshold		1.2	1.6	1.95	V

electrical characteristics over recommended operating free-air temperature range, V_I = 3.6 V, V_O = 2.5 V, I_O = 300 mA, EN = V_{IN}, ILIM = V_{IN}, T_A = −40°C to 85°C (unless otherwise noted) (continued)

power switch and current limit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	P-channel MOSFET on-resistance	$V_I = V_{GS}$ = 3.6 V, I = 200 mA	200	280	410	mΩ
		$V_I = V_{GS}$ = 2 V, I = 200 mA		480		
	P-channel leakage current	V_{DS} = 5.5 V			1	μA
	N-channel MOSFET on-resistance	$V_I = V_{GS}$ = 3.6 V, I_O = 200 mA	200	280	410	mΩ
		$V_I = V_{GS}$ = 2 V, I_O = 200 mA		500		
	N-channel leakage current	V_{DS} = 5.5 V			1	μA
$I_{(LIM)}$	P-channel current limit	2.5 V ≤ V_I ≤ 5.5 V, ILIM = V_{IN}	800	1200	1600	mA
		2 V ≤ V_I ≤ 5.5 V, ILIM = GND	390	600	900	
V_{IH}	ILIM high-level input voltage		1.3			V
V_{IL}	ILIM low-level input voltage				0.4	V
I_{lkg}	ILIM input leakage current	ILIM = GND or V_{IN}		0.01	0.1	μA

power good output (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power good threshold	Feedback voltage falling	88% V_O	92% V_O	94% V_O	V
	Power good hysteresis			2.5% V_O		V
V_{OL}	PG output low voltage	$V_{(FB)} = 0.8 \times V_O$ nominal, $I_{(sink)}$ = 10 μA			0.3	V
I_{lkg}	PG output leakage current	$V_{(FB)} = V_O$ nominal		0.01	1	μA
Minimum supply voltage for valid power good signal			1.2			V

NOTE 3: Power good is not valid for the first 100 μs after EN goes high. Please refer to the application section for more information.

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_S	Oscillator frequency		500	750	1000	kHz
$f_{(SYNC)}$	Synchronization range	CMOS-logic clock signal on SYNC pin	500		1000	kHz
V_{IH}	SYNC high level input voltage		1.3			V
V_{IL}	SYNC low level input voltage				0.4	V
I_{lkg}	SYNC input leakage current	SYNC = GND or V_{IN}		0.01	0.1	μA
Duty cycle of external clock signal			20%		60%	

electrical characteristics over recommended operating free-air temperature range, V_I = 3.6 V, V_O = 2.5 V, I_O = 300 mA, EN = V_{IN}, ILIM = V_{IN}, T_A = −40°C to 85°C (unless otherwise noted) (continued)

output

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Adjustable output voltage range	TPS62000		0.8		5.5	V
V_{ref}	Reference voltage	TPS6200x			0.45		V
V_O	Fixed output voltage (see Note 4)	TPS62000 adjustable	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	V
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62001 0.9 V	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62002 1 V	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62003 1.2 V	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62004 1.5 V	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62005 1.8 V	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62008 1.9 V	V_I = 2.5 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62006 2.5 V	V_I = 2.7 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
		TPS62007 3.3 V	V_I = 3.6 V to 5.5 V; 0 mA ≤ I_O ≤ 600 mA	−3%		4%	
			10 mA < I_O ≤ 600 mA	−3%		3%	
Line regulation			V_I = V_O + 0.5 V (min. 2 V) to 5.5 V, I_O = 10 mA		0.05		%/V
Load regulation			V_I = 5.5 V; I_O = 10 mA to 600 mA		0.6%		
η	Efficiency		V_I = 5 V; V_O = 3.3 V; I_O = 300 mA		95%		
			V_I = 3.6 V; V_O = 2.5 V; I_O = 200 mA				
Start-up time			I_O = 0 mA, time from active EN to V_O	0.4		2	ms

NOTE 4: The output voltage accuracy includes line and load regulation over the full temperature range, T_A = −40°C to 85°C.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4, 5
$V_{(drop)}$	Dropout voltage	vs Load current	6
I_Q	Operating quiescent current	vs Input voltage (power save mode)	7
		vs Input voltage (forced PWM)	8
f_{osc}	Oscillator frequency	vs Free-air temperature	9
	Load transient response		10
	Line transient response		11
	Power save mode operation		12
	Start-up	vs Time	13
V_O	Output voltage	vs Load current	14

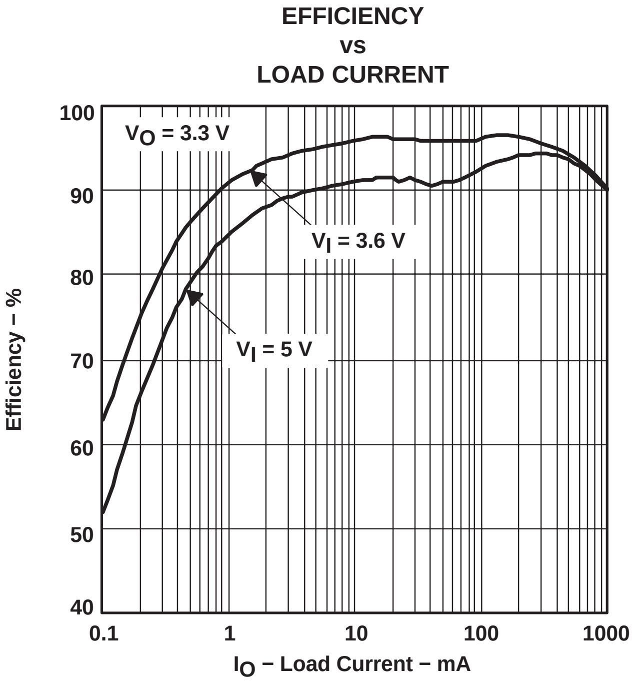


Figure 3

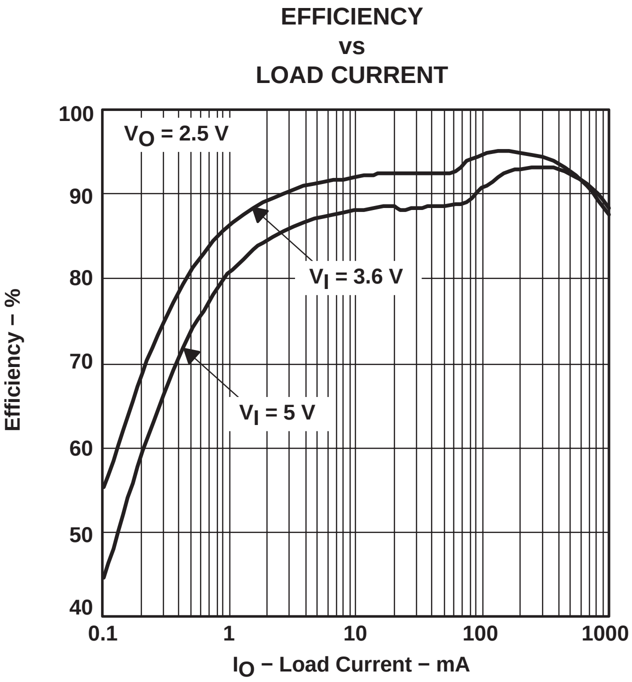


Figure 4

TYPICAL CHARACTERISTICS

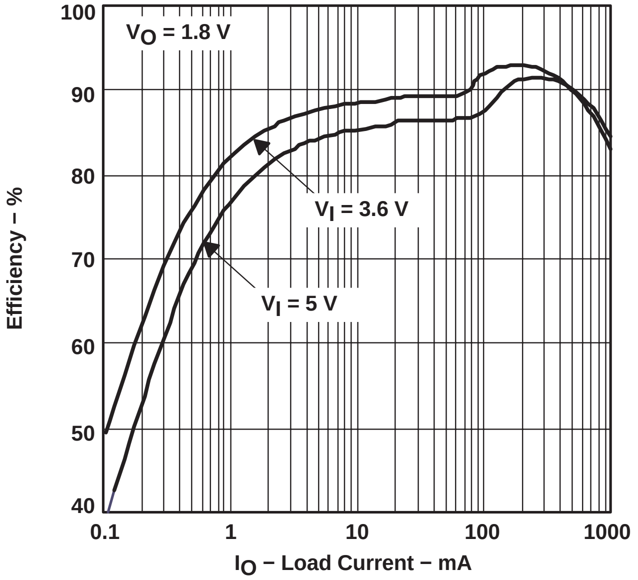

EFFICIENCY vs LOAD CURRENT

Figure 5

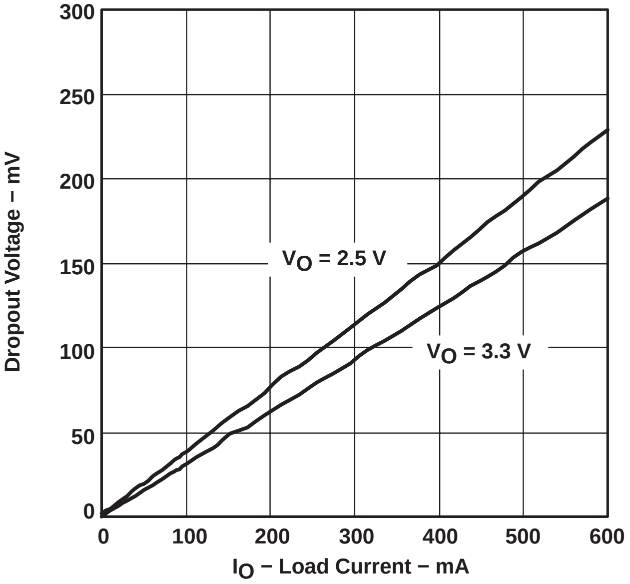

DROPOUT VOLTAGE vs LOAD CURRENT

Figure 6

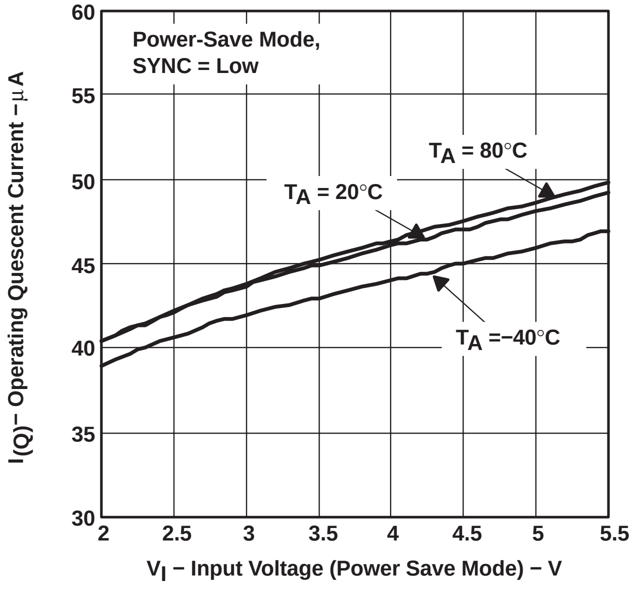

OPERATING QUIESCENT CURRENT vs INPUT VOLTAGE (POWER SAVE MODE)

Figure 7

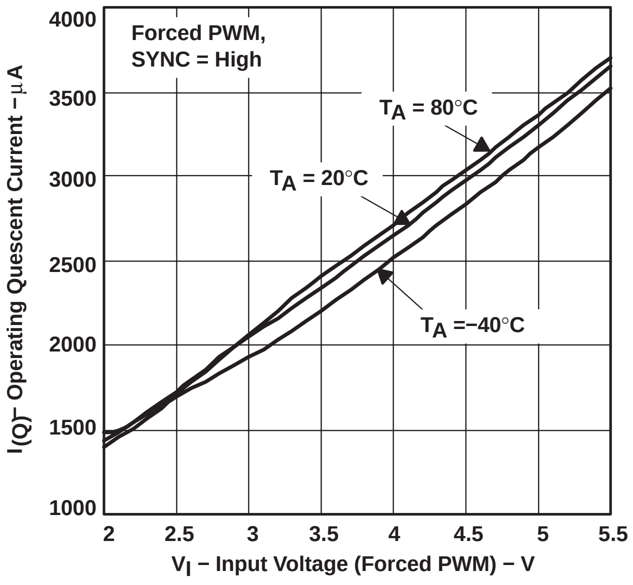

OPERATING QUIESCENT CURRENT vs INPUT VOLTAGE (FORCED PWM)

Figure 8

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

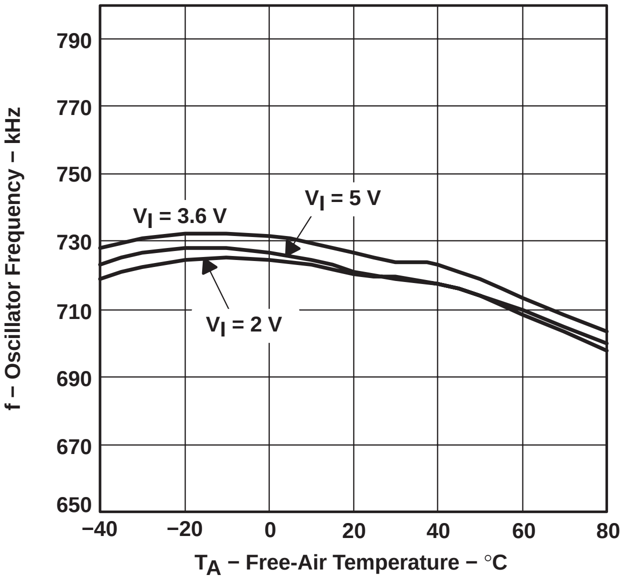


Figure 9

LOAD TRANSIENT RESPONSE

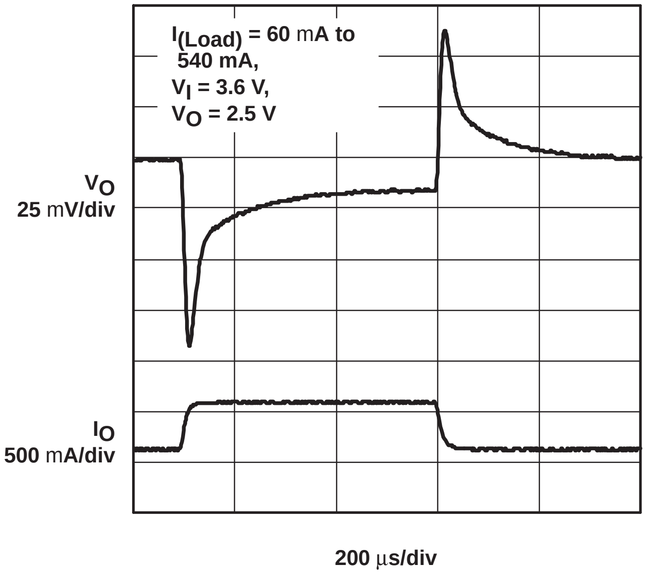


Figure 10

LINE TRANSIENT RESPONSE

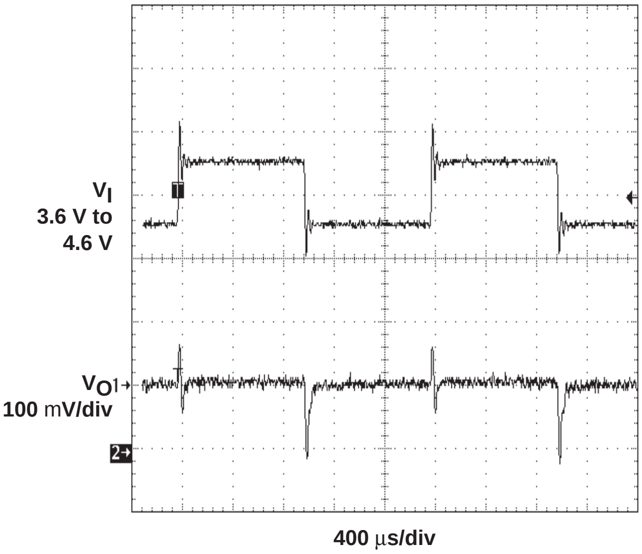


Figure 11

POWER SAVE MODE OPERATION

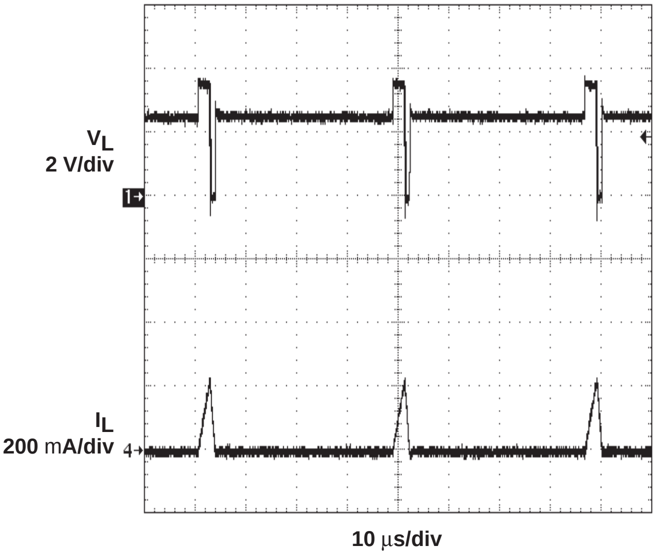


Figure 12

TYPICAL CHARACTERISTICS

START-UP
vs
TIME

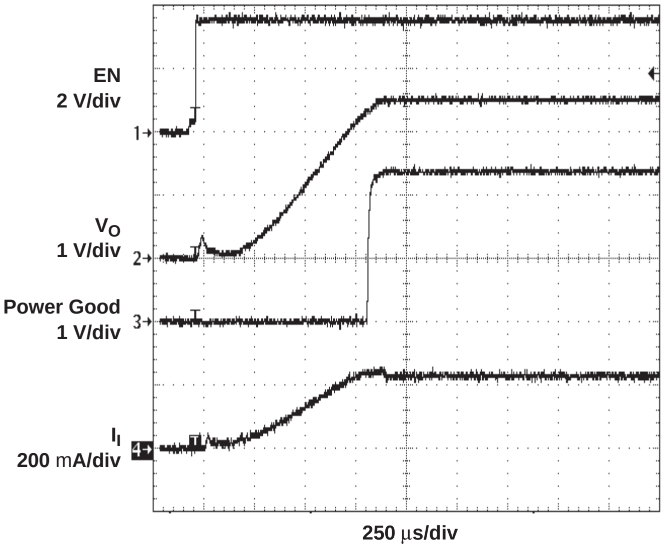


Figure 13

OUTPUT VOLTAGE
vs
LOAD CURRENT

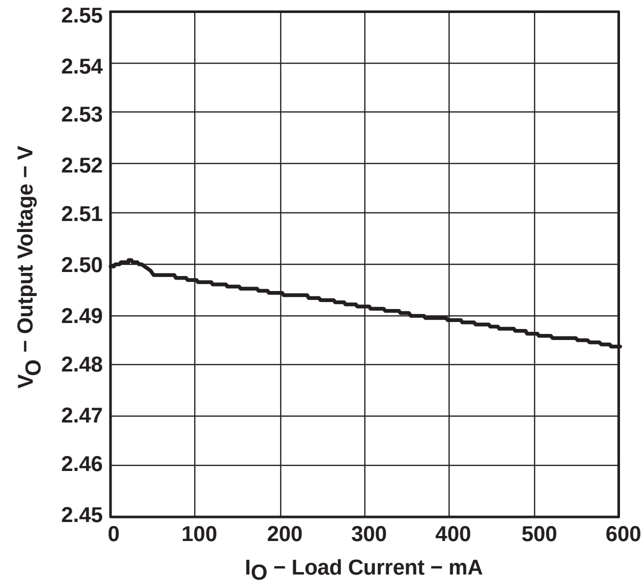


Figure 14

APPLICATION INFORMATION

adjustable output voltage version

When the adjustable output voltage version (TPS62000DGS) is used, the output voltage is set by the external resistor divider (see Figure 15).

The output voltage is calculated as:

$$V_O = 0.45\ V \times \left(1 + \frac{R1}{R2}\right)$$

With $R1 + R2 \le 1\ M\Omega$

$R1 + R2$ should not be greater than $1\ M\Omega$ because of stability reasons.

For stability reasons, a small bypass capacitor (C_{ff}) is required in parallel to the upper feedback resistor, refer to Figure 15. The bypass capacitor value can be calculated as:

$$C_{(ff)} = \frac{1}{2\pi \times 30000 \times R1} \text{ for } C_o < 47\ \mu F$$

$$C_{(ff)} = \frac{1}{2\pi \times 5000 \times R1} \text{ for } C_o \ge 47\ \mu F$$

R1 is the upper resistor of the voltage divider. For $C_{(ff)}$, choose a value which comes closest to the computed result.

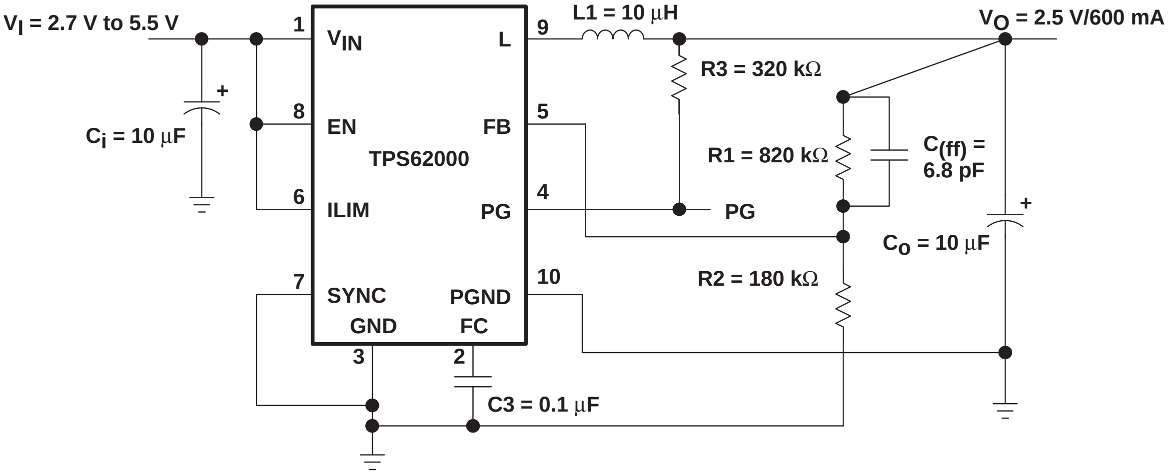


Figure 15. Typical Application Circuit for Adjustable Output Voltage Option

inductor selection

A 10 µH minimum output inductor is used with the TPS6200x. Values larger than 22 µH or smaller than 10 µH may cause stability problems because of the internal compensation of the regulator.

For output voltages greater than 1.8 V, a 22 µH inductance might be used in order to improve the efficiency of the converter.

After choosing the inductor value of typically 10 µH, two additional inductor parameters should be considered: first the current rating of the inductor and second the dc resistance.

The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency.

APPLICATION INFORMATION

inductor selection (continued)

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current which is calculated as:

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2}$$

Where:

f = Switching frequency (750 kHz typical)
L = Inductor value
ΔI_L = Peak-to-peak inductor ripple current
$I_{L(max)}$ = Maximum inductor current

The highest inductor current occurs at maximum V_I.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS6200x which is 1.6 A with ILIM = V_{IN} and 900 mA with ILIM = GND. See table 1 for recommended inductors.

Table 1. Tested Inductors

OUTPUT CURRENT	INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
0 mA to 600 mA	10 µH	Coilcraft DO3316P-103 Coilcraft DT3316P-103 Sumida CDR63B-100 Sumida CDRH5D28-100	High efficiency
		Coilcraft DO1608C-103 Sumida CDRH4D28-100	Smallest solution
0 mA to 300 mA	10 µH	Coilcraft DS1608C-103	High efficiency
		muRata LQH4C100K04	Smallest solution

output capacitor selection

For best performance, a low ESR output capacitor is needed. At output voltages greater than 1.8 V, ceramic output capacitors can be used to show the best performance. Output voltages below 1.8 V require a larger output capacitor and ESR value to improve the performance and stability of the converter.

Capacitor Selection

OUTPUT VOLTAGE RANGE	OUTPUT CAPACITOR	OUTPUT CAPACITOR ESR
$1.8\ V \le V_I \le 5.5\ V$	$C_O \ge 10\ \mu F$	ESR ≤ 120 mΩ
$0.8\ V \le V_I < 1.8\ V$	$C_O \ge 47\ \mu F$	ESR > 50 mΩ

See Table 2 for recommended capacitors.

APPLICATION INFORMATION

output capacitor selection (continued)

If an output capacitor is selected with an ESR value ≤ 120 mΩ, its RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated as:

$$I_{RMS(C_O)} = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR\right)$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

Table 2. Tested Capacitors

CAPACITOR VALUE	ESR/mΩ	COMPONENT SUPPLIER	COMMENTS
10 µF	50	Taiyo Yuden JMK316BJ106KL	Ceramic
47 µF	100	Sanyo 6TPA47M	POSCAP
68 µF	100	Spraque 594D686X0010C2T	Tantalum

input capacitor selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes.

The input capacitor should have a minimum value of 10 µF and can be increased without any limit for better input voltage filtering.

The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_{O(max)} \times \sqrt{\frac{V_O}{V_I} \times \left(1-\frac{V_O}{V_I}\right)}$$

The worst case RMS ripple current occurs at D = 0.5 and is calculated as: $I_{RMS} = \frac{I_O}{2}$.

Ceramic capacitor show a good performance because of their low ESR value, and they are less sensitive against voltage transients compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the IC for best performance.

APPLICATION INFORMATION

layout considerations

As for all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

Therefore, use wide and short traces for the main current paths as indicted in bold in Figure 16. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Place the bypass capacitor, C3, as close as possible to the FC pin. The analog ground, GND, and the power ground, PGND, need to be separated. Use a common ground node as shown in Figure 16 to minimize the effects of ground noise.

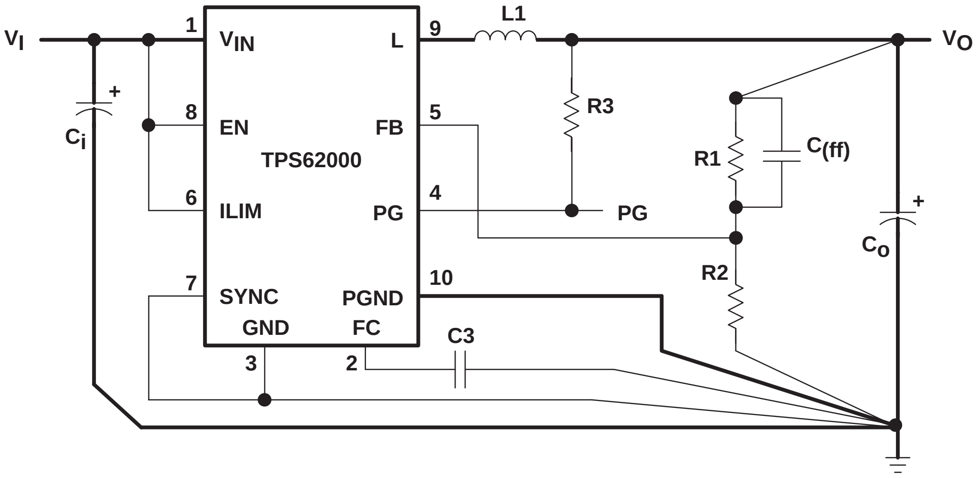
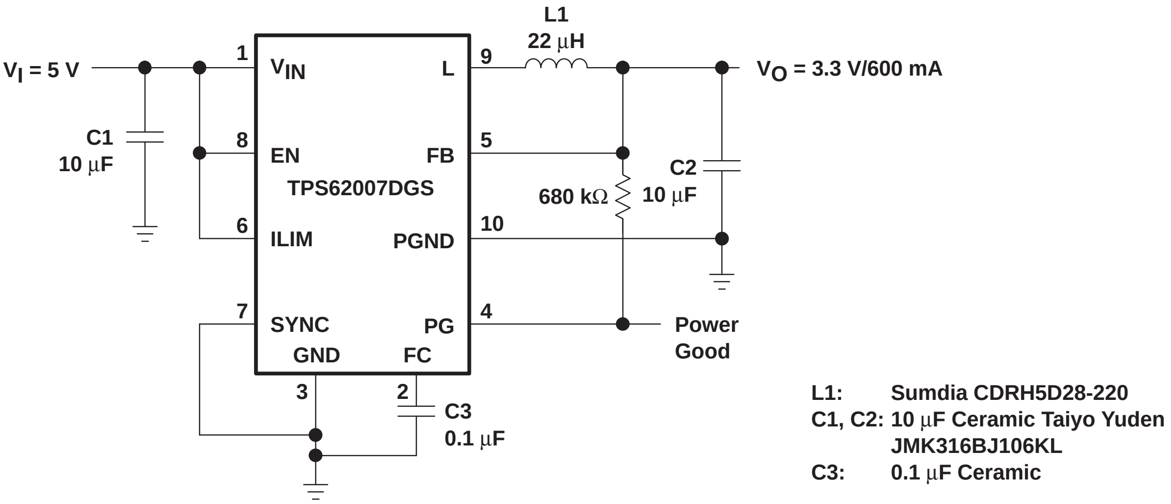


Figure 16. Layout Diagram

typical application

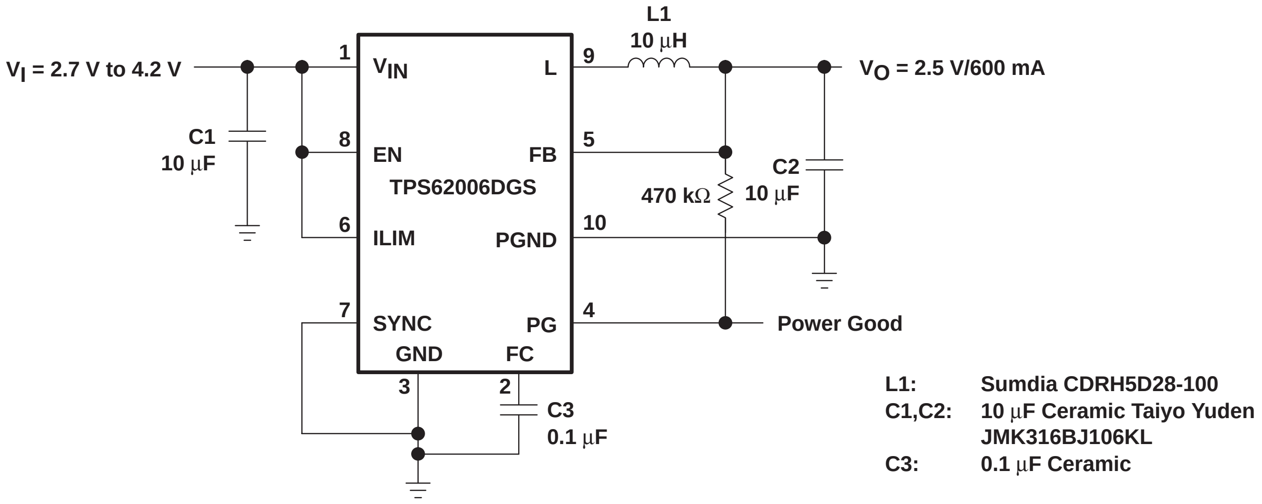


L1:	Sumdia CDRH5D28-220
C1, C2:	10 µF Ceramic Taiyo Yuden JMK316BJ106KL
C3:	0.1 µF Ceramic

Figure 17. Standard 5 V to 3.3 V/600 mA Conversion; High Efficiency

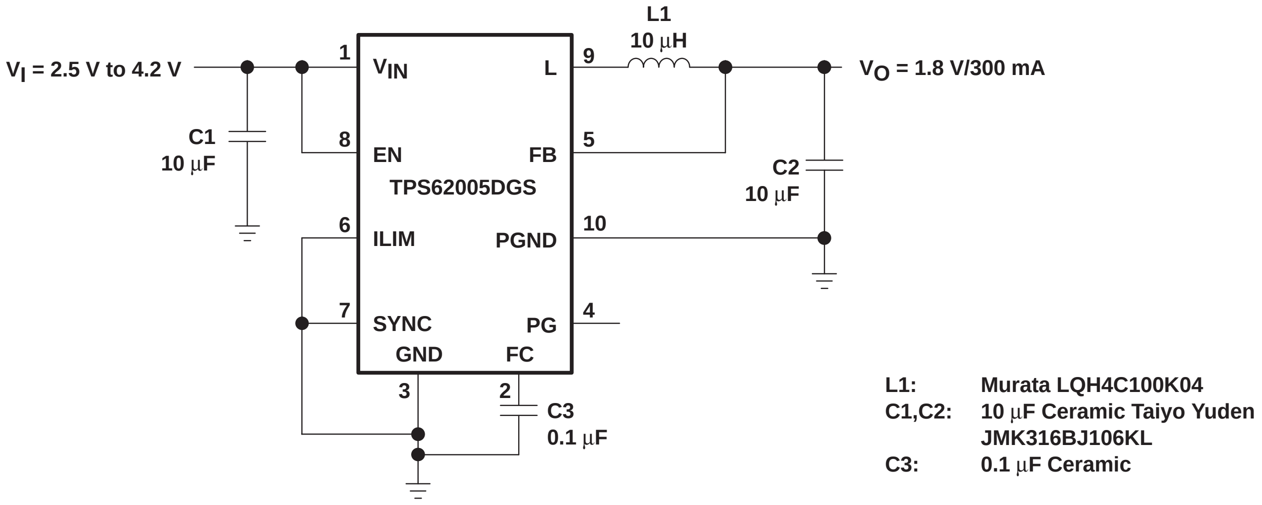
APPLICATION INFORMATION

typical application (continued)



L1: Sumdia CDRH5D28-100
C1,C2: 10 µF Ceramic Taiyo Yuden JMK316BJ106KL
C3: 0.1 µF Ceramic

Figure 18. Single Li-on to 2.5 V/600 mA Using Ceramic Capacitors Only



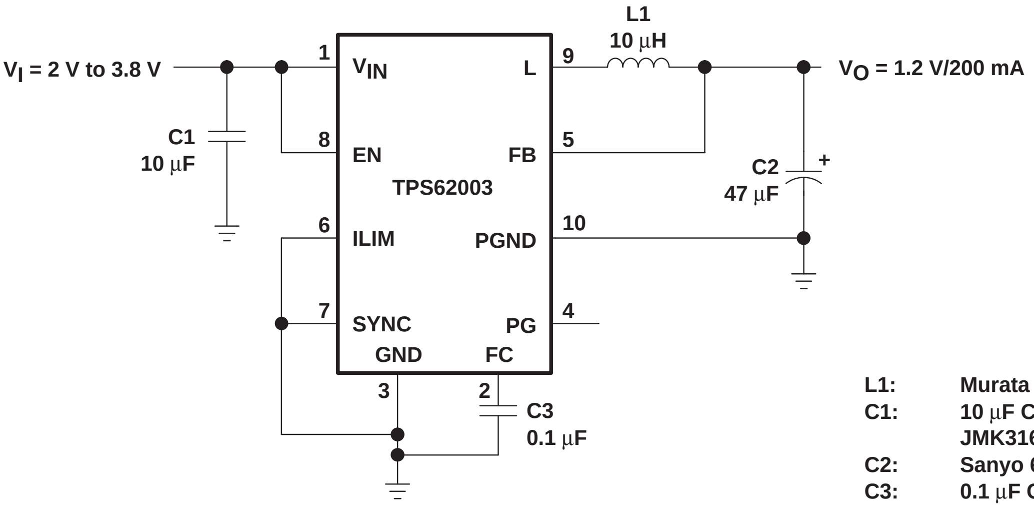
L1: Murata LQH4C100K04
C1,C2: 10 µF Ceramic Taiyo Yuden JMK316BJ106KL
C3: 0.1 µF Ceramic

NOTE: For low noise operation connect SYNC to V_{IN}

Figure 19. Single Li-on to 1.8 V/300 mA; Smallest Solution Size

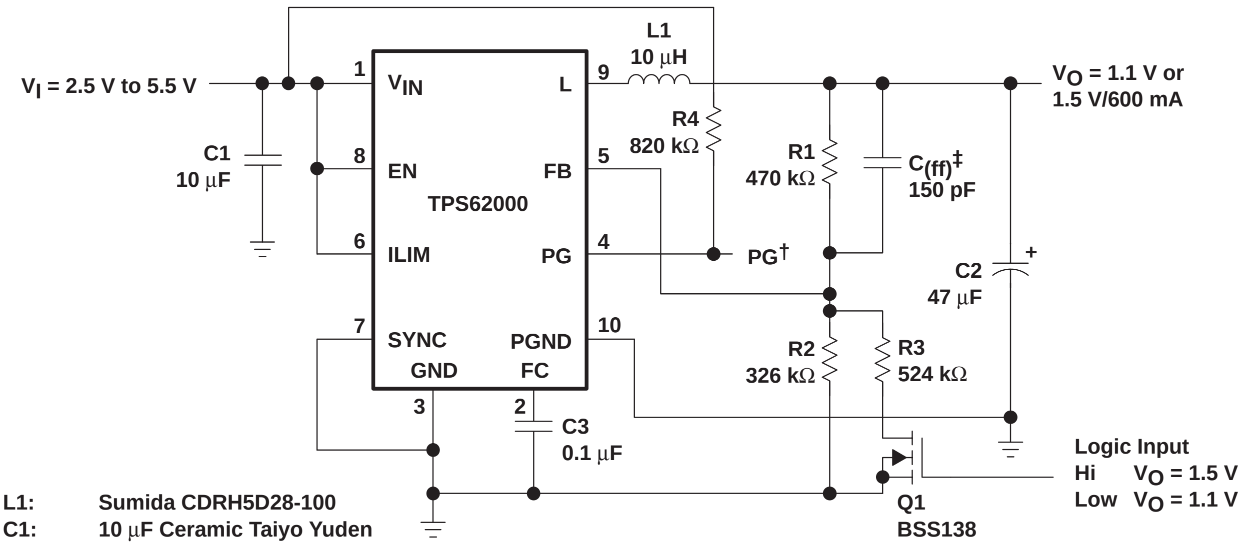
APPLICATION INFORMATION

typical application (continued)



L1: Murata LQH4C100K04
C1: 10 µF Ceramic Taiyo Yuden JMK316BJ106KL
C2: Sanyo 6TPA47M
C3: 0.1 µF Ceramic

Figure 20. Dual Cell NiMH or NiCd to 1.2 V/200 mA; Smallest Solution Size



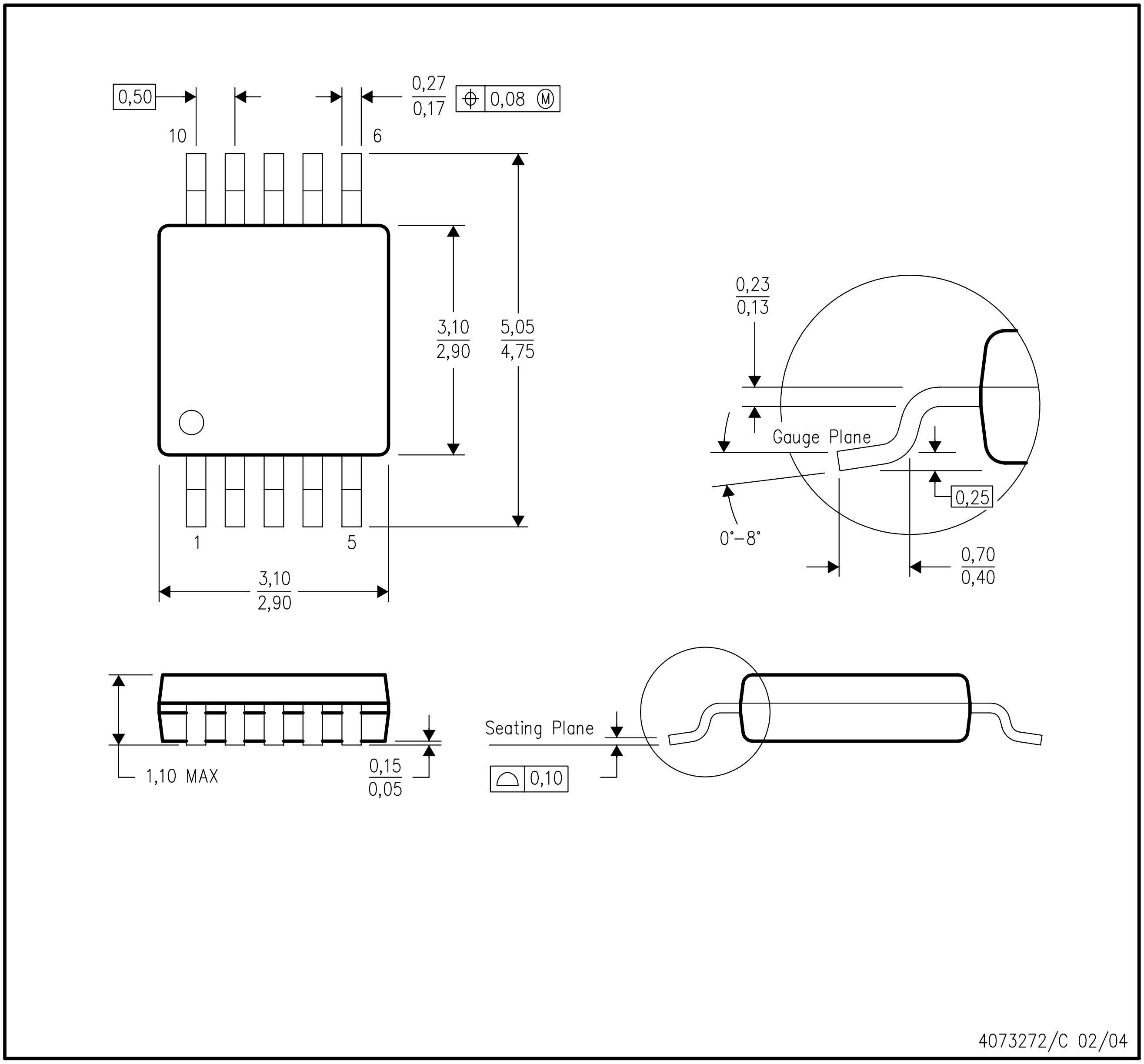
L1: Sumida CDRH5D28-100
C1: 10 µF Ceramic Taiyo Yuden JMK316BJ106KL
C2: Sanyo 6TPA47M
C3: 0.1 µF Ceramic

† Use a small R-C filter to filter wrong reset signals during output voltage transitions.

‡ A large value is used for $C_{(ff)}$ to compensate for the parasitic capacitance introduced into the regulation loop by Q1.

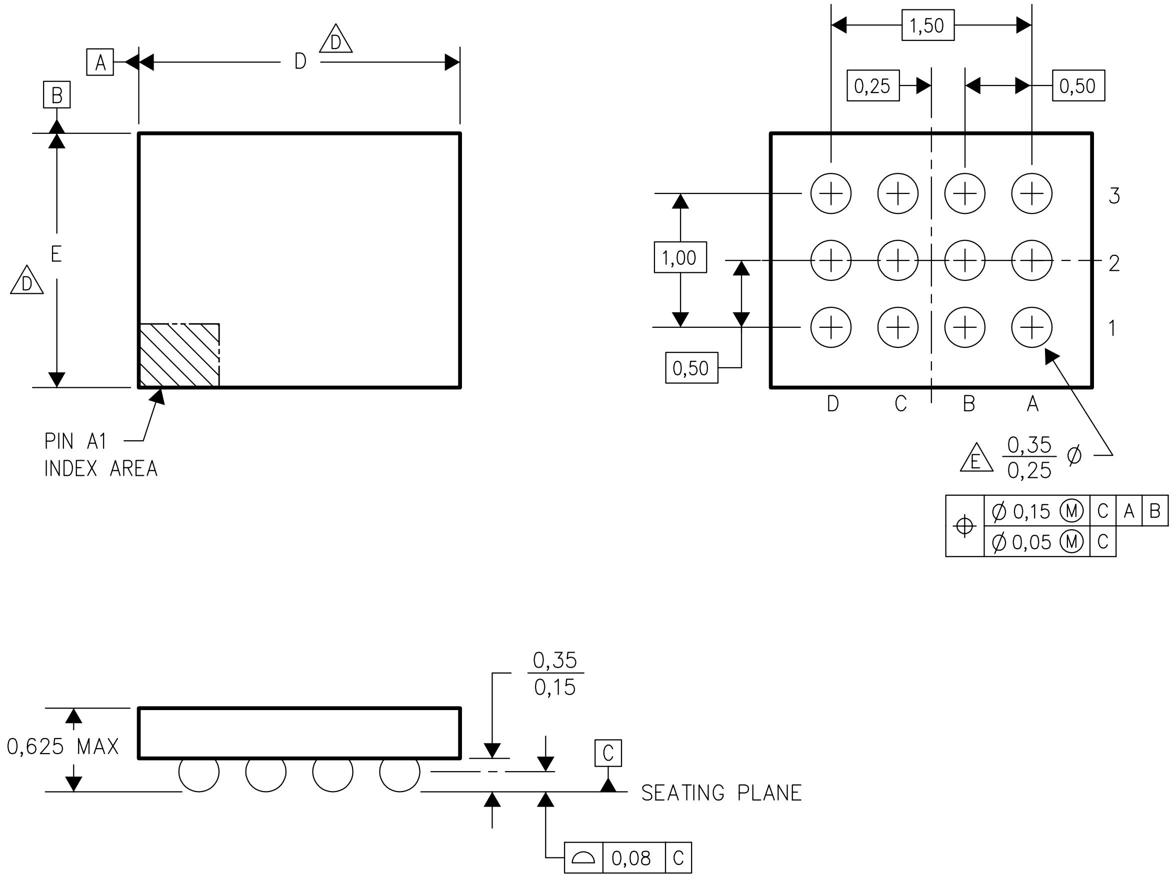
Figure 21. Dynamic Output Voltage Programming As Used in Low Power DSP Applications

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

YEG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



4204182/F 05/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- △D Devices in YEG package can have dimension D ranging from 1.85 to 2.65 mm and dimension E ranging from 1.35 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- △E Reference Product Data Sheet for array population. 4 x 3 matrix pattern is shown for illustration only.
- F. This package contains tin–lead (SnPb) balls. Refer to YZG (Drawing #4205059) for lead–free balls.

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