SPECIFICATION

LIQUID CRYSTAL DISPLAY MODULE

Model No. **UMSH-7295FD-CS**

☐ **CUSTOMER :** **U. R. T. STANDARD**

TENTATIVE

APPROVED SIGNATURE			
VERSION NO. 1			

SAMPLE 1

U.R.T. UNITED RADIANT TECHNOLOGY CORP.

APPROVED BY: _____ **DATE:** _____

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CONTENTS:

Revision record

Module number	Rev mark	Revision description	Rev by	Rev date	Sample No.
UMSH-7295FD-CS	0	1. Tentative without optical characteristics	葉 翊 國 UCSH-E605EN-FS	7/23/02’	0
UMSH-7295FD-CS	1	Add LED backlight cathode pin.	葉 翊 國 UCSH-E605EN-FS	8/19/02’	1

1. Basic Specifications

1-1 Mechanical specifications:

Items	Nominal Dimension	Unit
Dot Matrix	120RGB X 160 DOTS	—
Module Size (W X H X T)	40.1 X 59.15 X 3.9	mm.
Viewing Area (W X H)	28.6 X 37.5	mm.
Active Area (W X H)	26.625 X 35.505	mm.
Dot Size (W X H)	0.207 X 0.207	mm
Dot Pitch (W X H)	0.222 X 0.222	mm.
Driving Method	1/160	Duty
	1/12	Bias
Driving IC Assembly	TAB	—

1-2 Display Specifications:

Display	Descriptions	Note
LCD Type	COLOR STN (4096 color)	
LCD Mode	Negative	
Polarizer Mode	Transflective	
Polarizer UV - Cutting	With	
Polarizer Surface	Anti-glare	
Background Color	Black	
Backlight Type	LED	
Backlight Color	White	
Viewing Angle	6 O‘clock Direction	

＊ Exporse the driver IC under blaze (luminosity over than 1 cd) when using the LCM may cause IC operating failure

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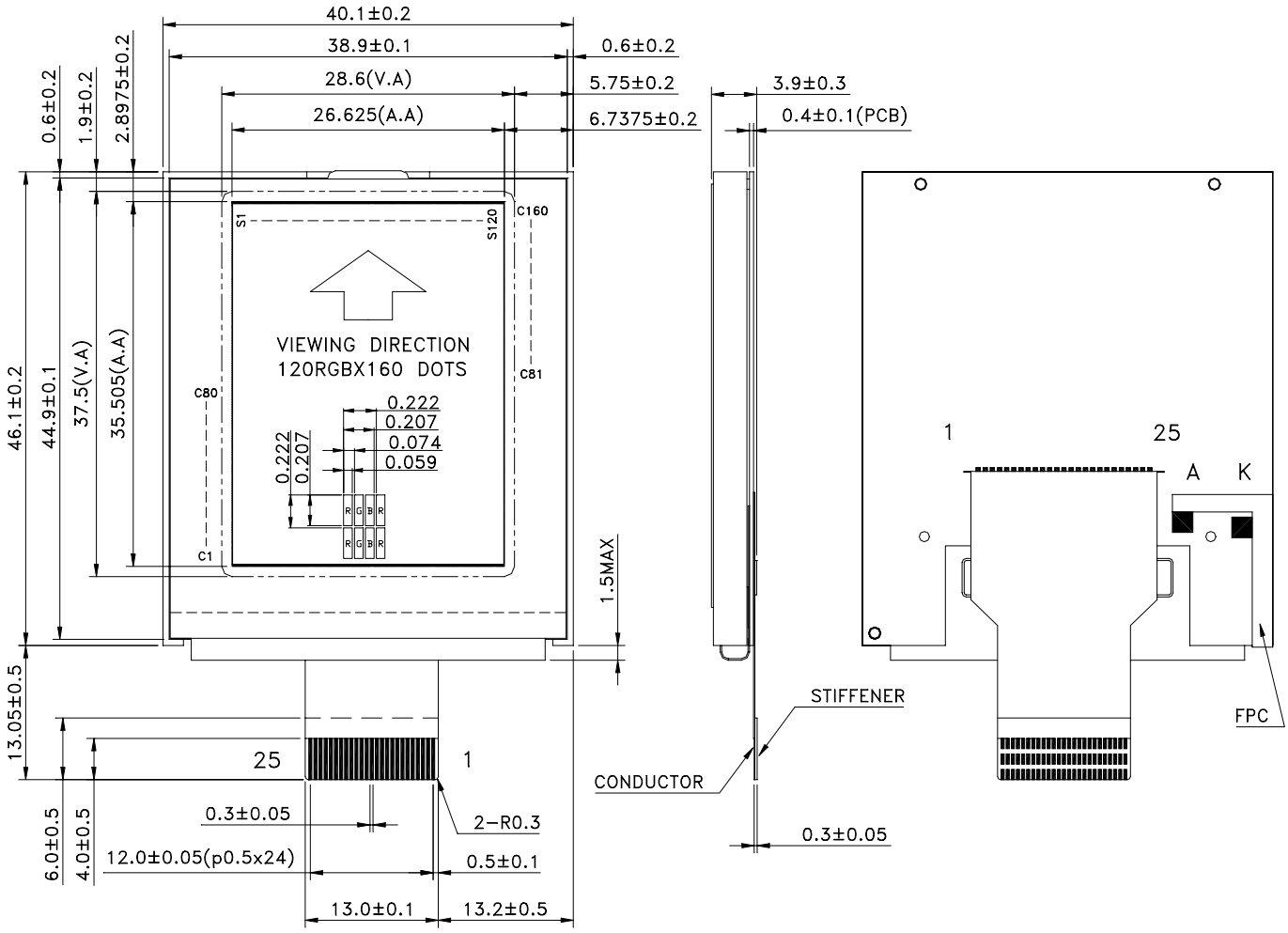
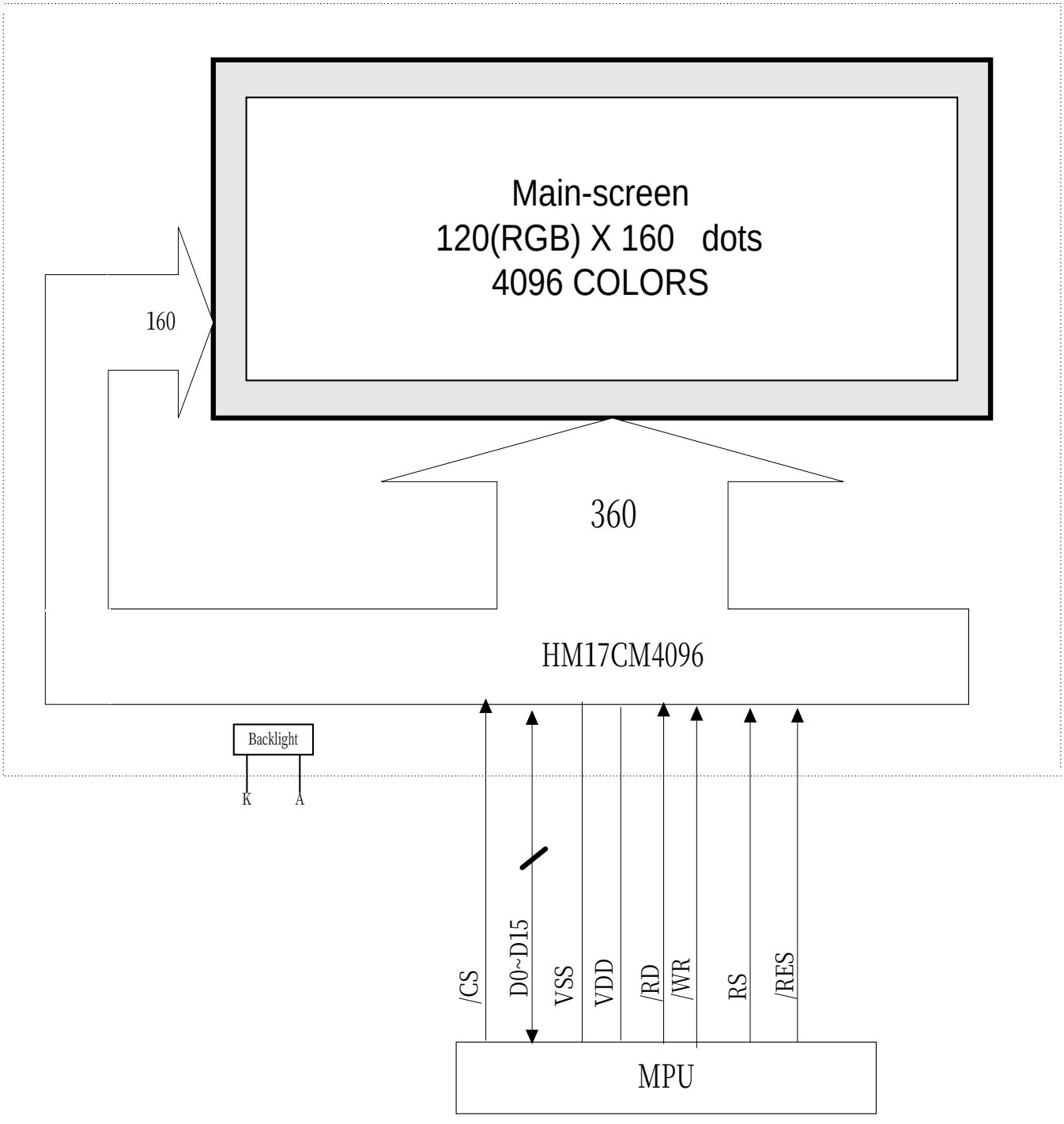
1-3 Outline Dimension



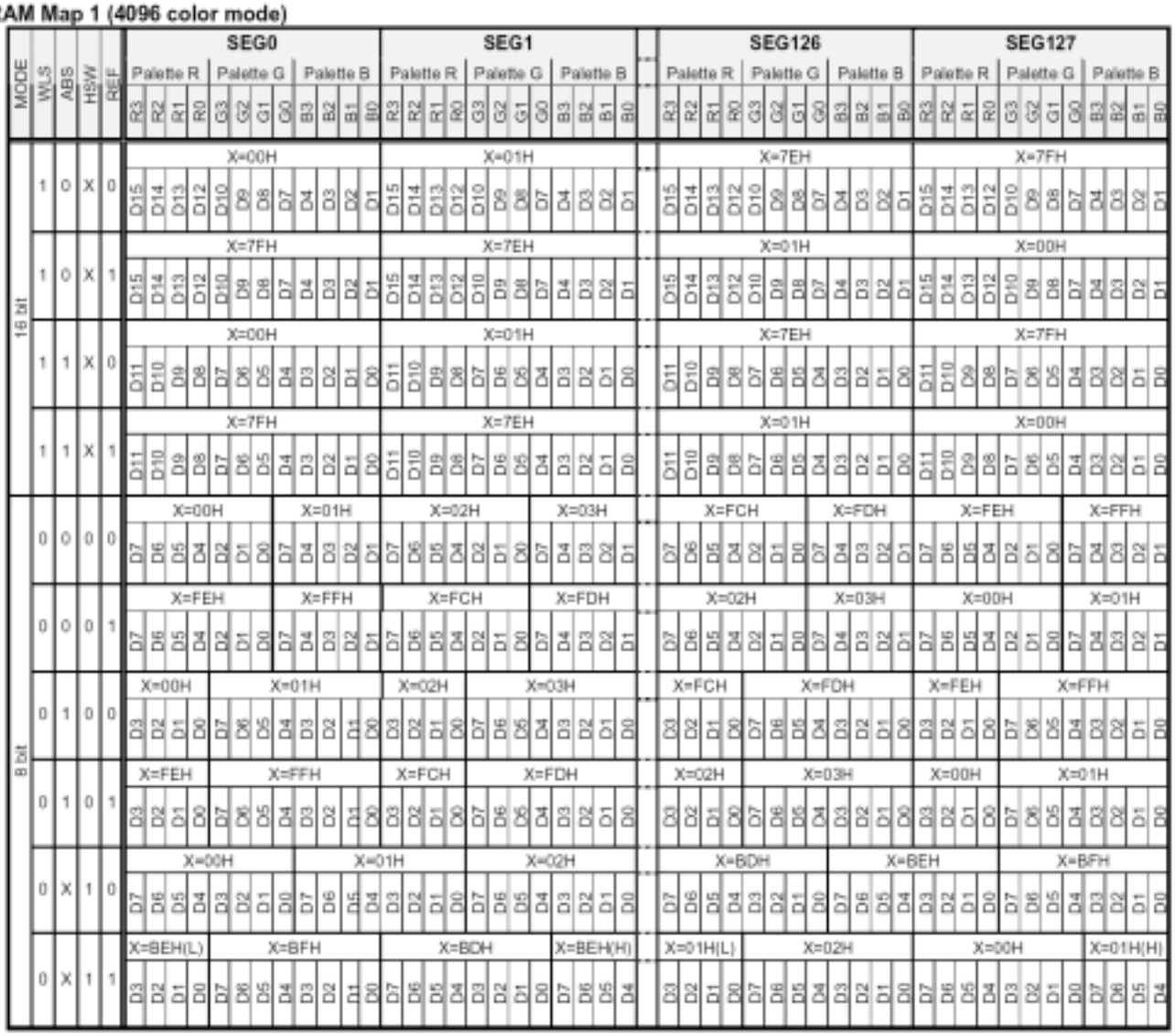
NOTE :
1. LCD : COLOR STN, TRANSFLECTIVE TYPE, NEGATIVE
2. ANTI GLARE TYPE
3. VIEWING DIRECTION : 6 O'CLOCK
4. Top : −20 ~ 70 °C ; Tst : −30 ~ 80 °C
5. VOP : 16.0 V , 1/160 DUTY , 1/12 BIAS
6. IC : HM17CM4096−02M
7. VLED : 5.0 V ; 3 PCS LED CHIP (WHITE)

1-4 Block Diagram

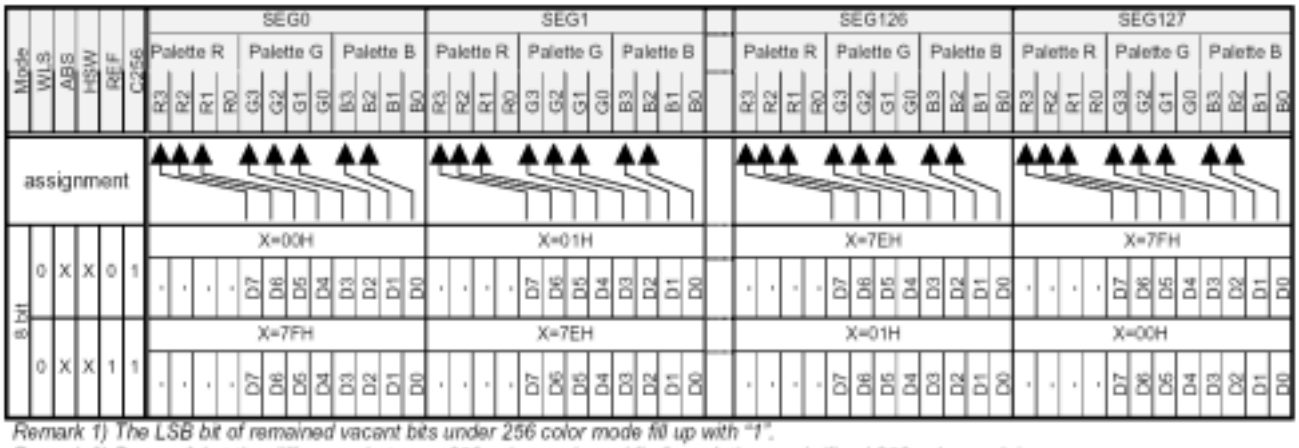


1-5 GRAM Address

RAM Map 1 (4096 color mode)



RAM Map 2 (256 color mode)



Remark 1) The LSB bit of remained vacant bits under 256 color mode fill up with "1".
Remark 2) Be careful at the difference between 256 color mode and fix 8 gradation mode(fixed 256 color mode).
Remark 3) There is no data compatibility between that was written at C256 = "0" and that was done at C256 = "1".
Remark 4) The 16 bit access mode is not available under 256 color mode but only 8 bit access is possible.

1-6 Interface Pin Connection:

Pin No.	Pin Symbol	I/O	Connected to	Description
1	**VDD**	**-**	**Power supply**	**Power supply VDD:3V.**
2	**/RES**	**I**	**MPU**	**Reset pin.**
3	**/CS**	**I**	**MPU**	**Chip select input for color screen.**
4	**RS**	**I**	**MPU**	**Data\command selection.**
5	**VSS**	**-**	**Power supply**	**Power supply GND.**
6	**/WR**	**I**	**MPU**	**Write select input.**
7	**/RD**	**I**	**MPU**	**Read select input**
8	**DB0**	**I/O**	**MPU**	**Data bit0.**
9	**DB1**	**I/O**	**MPU**	**Data bit1.**
10	**DB2**	**I/O**	**MPU**	**Data bit2.**
11	**DB3**	**I/O**	**MPU**	**Data bit3.**
12	**DB4**	**I/O**	**MPU**	**Data bit4.**
13	**DB5**	**I/O**	**MPU**	**Data bit5.**
14	**DB6**	**I/O**	**MPU**	**Data bit6.**
15	**DB7**	**I/O**	**MPU**	**Data bit7.**
16	**DB8**	**I/O**	**MPU**	**Data bit8.**
17	**DB9**	**I/O**	**MPU**	**Data bit9.**
18	**DB10**	**I/O**	**MPU**	**Data bit10.**
19	**DB11**	**I/O**	**MPU**	**Data bit11.**
20	**DB12**	**I/O**	**MPU**	**Data bit12.**
21	**DB13**	**I/O**	**MPU**	**Data bit13.**
22	**DB14**	**I/O**	**MPU**	**Data bit14.**
23	**DB15**	**I/O**	**MPU**	**Data bit15.**
24	**LEDA**	**-**	**LED Power supply**	**LED backlight anode input (+5V).**
25	**LEDK**	**-**	**LED Power supply**	**LED backlight cathode input (0V).**

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

(GND = 0V)

Items	Symbol	Min.	Max.	Unit
Supply voltage for logics	VDD	-0.3	+4.0	V
Supply voltage for driving LCD	V_{LCD}	-0.3	+20	V
Input voltage	V_{IN}	-0.3	VDD+0.3	V
Operating temperature range	T_{OP}	-20	70	℃
Storage temperature range	T_{ST}	-30	80	℃

2.2 DC Characteristics

(VCC=3.0± 0.5V,GND=0V, T_a=25°C)

Items	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage (Logic)	V_{CC}	-	3.0	-	V	
Supply voltage (LCD)	V_{op}	15.7	16.0	16.3	V	*NOTE1
Input high level voltage	V_{IH}	0.8VDD	-	VDD	V	
Input low level voltage	V_{IL}	0	-	0.2VDD	V	
Power supply current (VDD)	I_{CC}	-	4.0	8.0	mA	*NOTE2
Power supply current (LED)	I_{led}	-	35.0	-	mA	*NOTE2

*NOTE1 : Min. and Max. Voltage is specified as the voltage within the condition of operational temperature range -20°C ~ 70°C.

Typ. Voltage is specified as module driving condition: T_a=25°C.

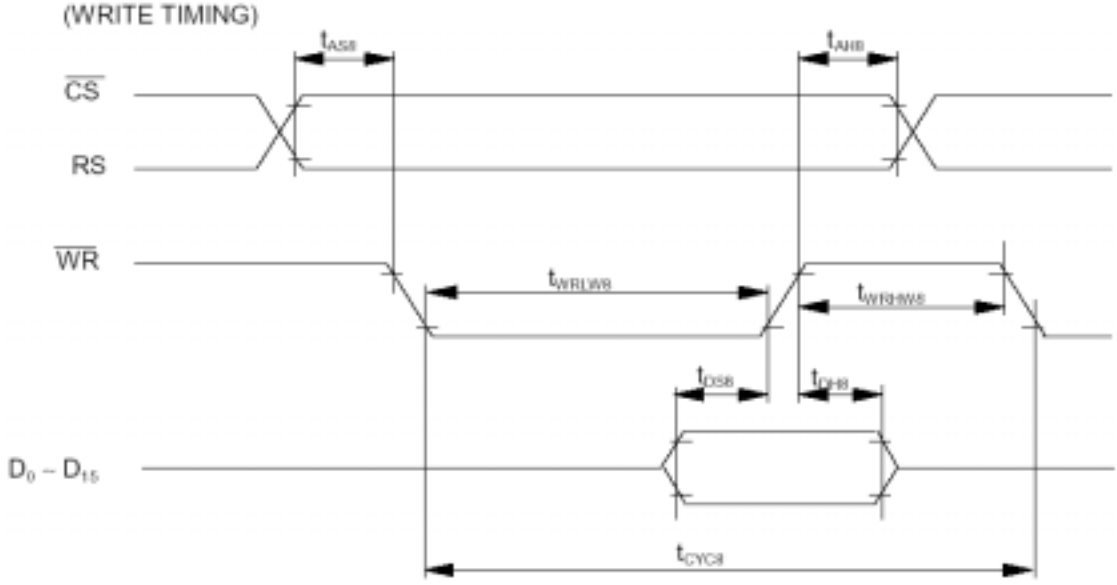
*NOTE2 :
Measuring Condition:
Standard Value MAX.

T_a	= 25°C
VDD-VSS	= 3.0V
V_{1OUT}-VSS	= V_{OP} at optimum contrast
Duty	= 1/160 Duty
Bias	= 1/12 Bias
Display Pattern	= Checkered pattern

2.3 AC Characteristic

SYSTEM BUS READ / WRITE TIMING (80 series CPU interface)

(WRITE TIMING)



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLWR} t_{WRHWR}		90 35 35		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		30 5		ns ns	$D_0 - D_{15}$

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

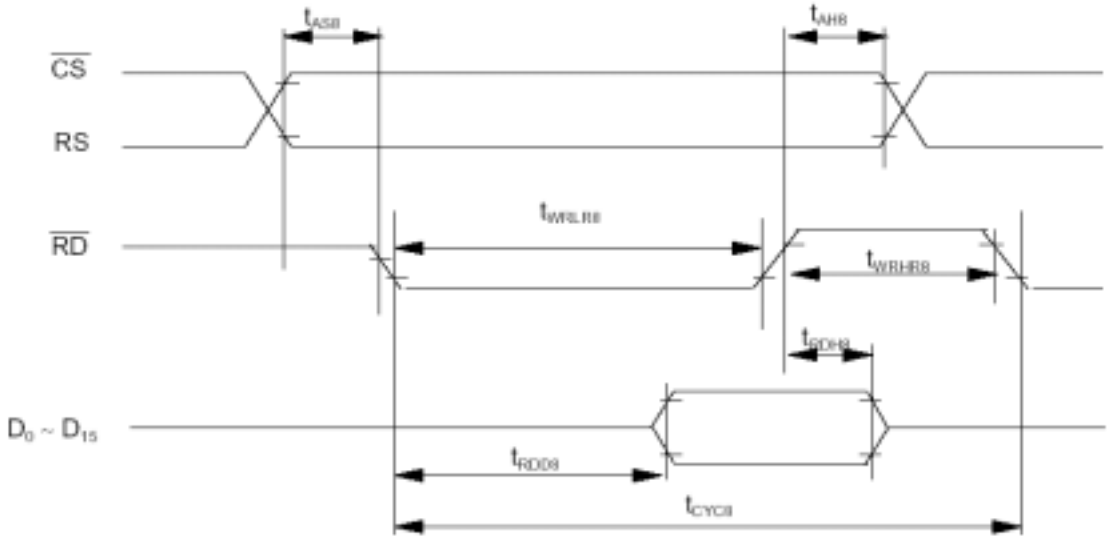
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLWR} t_{WRHWR}		160 70 70		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		40 5		ns ns	$D_0 - D_{15}$

(V_{DD}=1.7~2.2V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing Write "L" pulse width Write "H" pulse width	t_{CYC8} t_{WRLWR} t_{WRHWR}		180 80 80		ns ns ns	$\overline{WR}$
Data setup timing Data hold timing	t_{DS8} t_{DH8}		70 10		ns ns	$D_0 - D_{15}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

(READ TIMING)



(V_{DD}=2.5~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing read "L" pulse width read "H" pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	$\overline{RD}$
read data output delay time read data output hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	$D_0 \sim D_{15}$

(V_{DD}=2.2~2.5V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing read "L" pulse width read "H" pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	$\overline{RD}$
read data output delay time read data output hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	$D_0 \sim D_{15}$

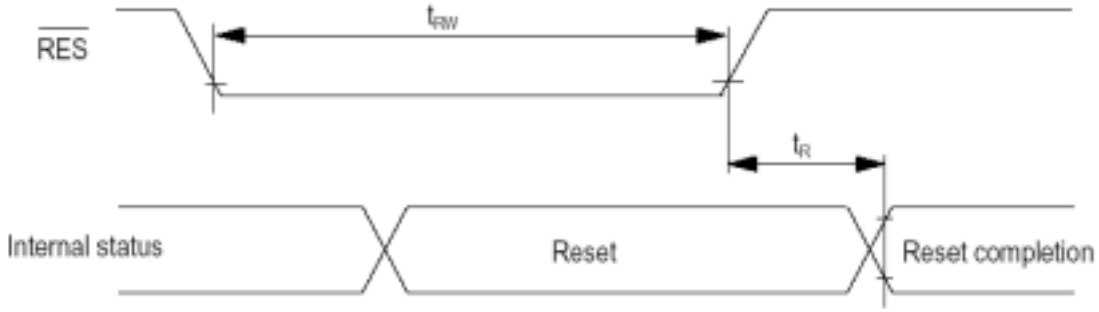
(V_{DD}=1.7~2.2V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing Address setup timing	t_{AH8} t_{AS8}		0 0		ns ns	$\overline{CS}$ RS
System cycle timing read "L" pulse width read "H" pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	$\overline{RD}$
read data output delay time read data output hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	110	ns ns	$D_0 \sim D_{15}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

Reset Timing Characteristics

RESET INPUT TIMING



(V_{DD}=2.4~3.3V, Ta=-30~+85°C)

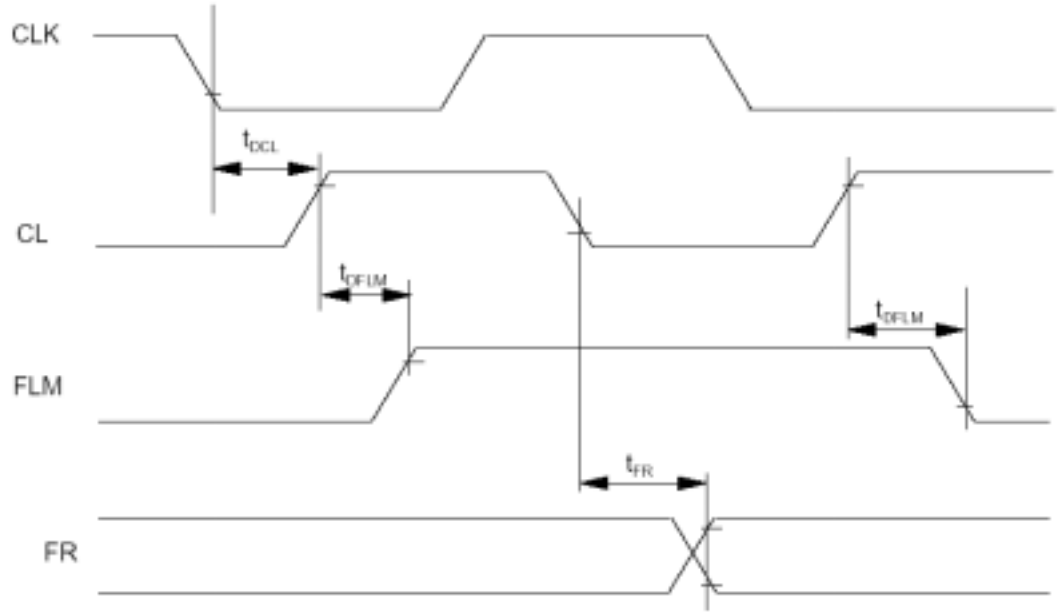
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.0	μs	
$\overline{RES}$ "L" pulse width	t_{RW}		10.0		μs	$\overline{RES}$

(V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.5	μs	
$\overline{RES}$ "L" pulse width	t_{RW}		10.0		μs	$\overline{RES}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

Display Control Timing



OUTPUT TIMING (V_{DD}=2.4~3.3V, Ta=-30~+85°C)

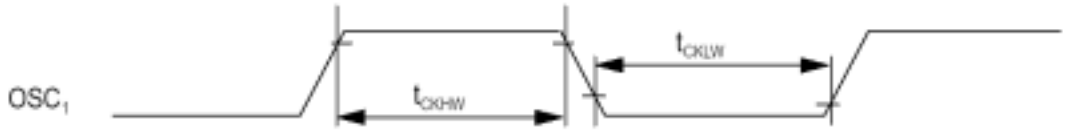
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay timing	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay timing	t_{FR}		0	500	ns	FR
CL delay timing	t_{DCL}		0	200	ns	CL

OUTPUT TIMING (V_{DD}=1.7~2.4V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay timing	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay timing	t_{FR}		0	1000	ns	FR
CL delay timing	t_{DCL}		0	200	ns	CL

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

Source Clock Input timing



(V_{DD}=1.7~3.3V, Ta=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
OSC_1 "H" pulse width (1)	t_{CKHW1}		0.555	0.800	μs	OSC_1
OSC_1 "L" pulse width (1)	t_{CKLW1}		0.555	0.800	μs	*1
OSC_1 "H" pulse width (2)	t_{CKHW2}		2.46	3.54	μs	OSC_1
OSC_1 "L" pulse width (2)	t_{CKLW2}		2.46	3.54	μs	*2
OSC_1 "H" pulse width (3)	t_{CKHW3}		16.9	24.4	μs	OSC_1
OSC_1 "L" pulse width (3)	t_{CKLW3}		16.9	24.4	μs	*3

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

*1. Applicable under gradation display, MON="0", PWM="0"
*2. Applicable under fixed gradation display, MON="0",PWM="1"
*3. Applicable under BW display, MON="1"

3. Optical Characteristics

3.1 Optical Characteristics

Driving Condition

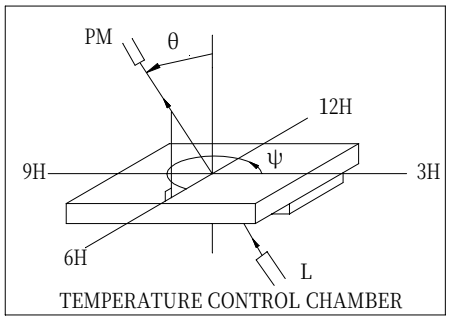
Item	Voltage	Duty	Bias
Valu	16.0	1/160	1/12

Electrical/Optical Characteristics

No	Item		Symbol/Temp.		MIN.	TYP.	MAX.	Unit.	Remarks
1	Vop Voltage		-20℃		-	-	-	V	Note2
			25℃		-	-	-		
			70℃		-	-	-		
2	Response Time		Tr	-20℃	-	-	-	ms	Note4
				25℃	-	-	-		
				70℃	-	-	-		
			Tf	-20℃	-	-	-		
				25℃	-	-	-		
				70℃	-	-	-		
3	Viewing Angle	Front-Rear	Θ1	Φ=270	-	-	-	deg.	Note1
		Left-Right	Θ2		-	-	-		
4	Contrast Ratio		Cr	25℃	-	-	-	-	Note3

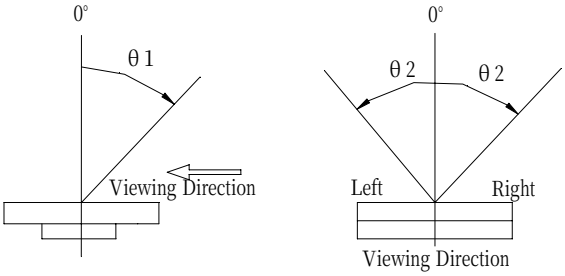
3.2 Definition of Optical Characteristics

Measurement Condition
L: LIGHT SOURCE
PM: LIGHT RECEIVING PHOTOMULTIPLIER TUBE

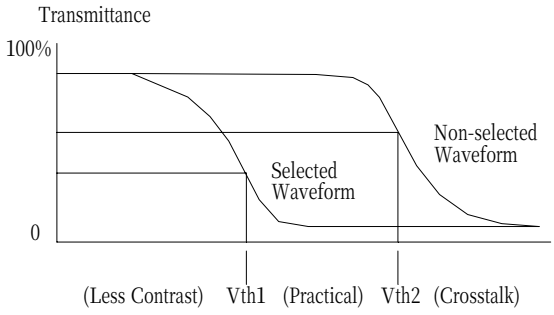


[Note 1] Definition of Viewing Angle

Viewing Direction: ψ=270°

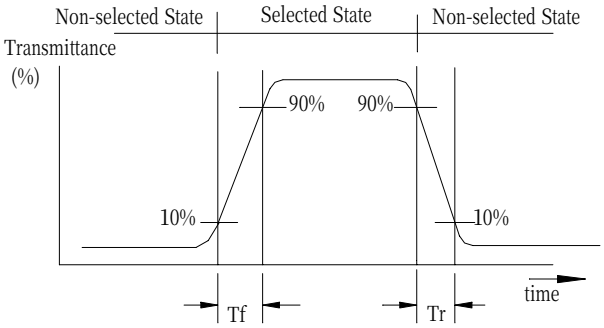


[Note 2] Definition of "Vth"



(a). Vth1: ψ=270°, θ 1=10°, Selected Waveform 50% Transmittance
(b). Vth1: ψ=270°, θ 1=40°, Non-selected Waveform 70% Transmittance

[Note 4] Definition of Response Time



Measurement Condition: Viewing Angle: θ 2=0°, θ 1=0°

[Note 3] Definition of Contrast Ratio

(a). Contrast Ratio= $\frac{\text{Transmittance under Non-selected Waveform}}{\text{Transmittance under Selected Waveform}}$

(b). Measurement Condition: Viewing Angle: θ 2=0°, θ 1=10°

4. Control And Display Command

4-1 Reset Function

HM17CM4096 is initialized as following description when $\overline{RES}$ terminal is set to "L".

INITIAL SETTING CONDITION (default setting)

1. display RAM	: unknown
2. X address	: 00_H set
3. Y address	: 00_H set
4. display start line	:1 line value 0_H
5. display ON/OFF	: display OFF
6. positive/negative	: positive
7. display duty ratio	: 1/163
8. n line inversion	: n inversion disable
9. COM shift direction	: COM0 → COM_{161}
10. increment mode	: increment OFF
11. REF mode	: positive
12. data SWAP mode	: OFF
13. electric volume	: (0, 0, 0, 0, 0, 0, 0)
14. power circuit	: OFF
15. display mode	: gradation display mode
16. bias ratio	: 1/9 bias
17. gradation palette 0	: (0, 0, 0, 0, 0)
18. gradation palette 1	: (0, 0, 0, 1, 1)
19. gradation palette 2	: (0, 0, 1, 0, 1)
20. gradation palette 3	: (0, 0, 1, 1, 1)
21. gradation palette 4	: (0, 1, 0, 0, 1)
22. gradation palette 5	: (0, 1, 0, 1, 1)
23. gradation palette 6	: (0, 1, 1, 0, 1)
24. gradation palette 7	: (0, 1, 1, 1, 1)
25. gradation palette 8	: (1, 0, 0, 0, 1)
26. gradation palette 9	: (1, 0, 0, 1, 1)
27. gradation palette 10	: (1, 0, 1, 0, 1)
28. gradation palette 11	: (1, 0, 1, 1, 1)
29. gradation palette 12	: (1, 1, 0, 0, 1)
30. gradation palette 13	: (1, 1, 0, 1, 1)
31. gradation palette 14	: (1, 1, 1, 0, 1)
32. gradation palette 15	: (1, 1, 1, 1, 1)
33. gradation mode	: variable mode
34. RAM data length	: 8-bit mode
35. discharge register	: "0"

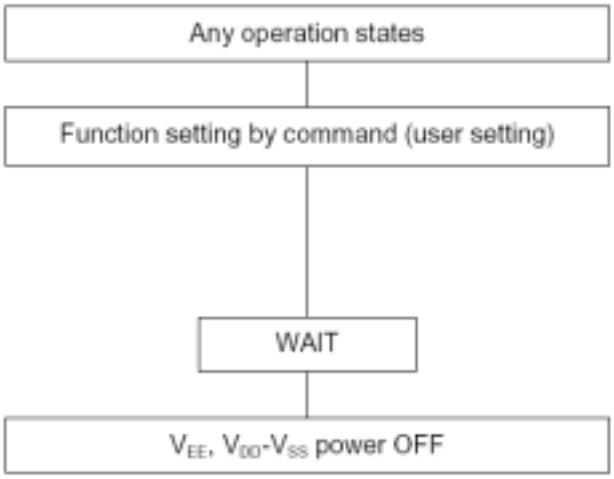
4-1.1 Discharge Circuit

The discharge circuit of voltage (V_{LCD}, V_1~V_4) stabilization capacitor is built in the **HM17CM4096**.

To discharge the capacitors, set the DIS register to "1" or set the $\overline{RES}$ terminal to "L"(discharge when only "L" period). When built-in power supply circuit is used, built-in power supply circuit should be disabled (DCON, AMPON = "0,0") before discharging of the capacitor is executed.

Do not turn on the internal power supply and external power supply (V_{LCD}, V_1~V_4, V_{OUT}) during discharging is executed.

4-1.2 Power Off



- HALT command set or reset operation (All LCD driver output is V_{SS} level)
- Discharge command set (Discharge of V_{LCD}, V_1~V_4 capacitor)

Before turning off the power, be sure to execute HALT or RESET command to make LCD driver output OFF state.

And if the level of V_{EE} and V_{DD} are different (not common but different source), V_{EE} terminal should be turned ON/OFF during V_{DD} terminal voltage maintain voltage level.

4.2 Instruction Table

INSTRUCTION TABLE (1)

INSTRUCTION	CODE (80 series I/F)							code								function
	CS	RS	RD	WR	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display data write in	0	0	1	0	0/1	0/1	0/1	Write Data								Write in to display RAM
Display data read out	0	0	0	1	0/1	0/1	0/1	Read Data								Read out from display RAM
X address (lower) [0_H]	0	1	1	0	0	0	0	0	0	0	0	AX_3	AX_2	AX_1	AX_0	X address setting of display RAM.
X address (upper) [1_H]	0	1	1	0	0	0	0	0	0	0	1	AX_7	AX_6	AX_5	AX_4	X address setting of display RAM.
Y address (lower) [2_H]	0	1	1	0	0	0	0	0	0	1	0	AY_3	AY_2	AY_1	AY_0	Y address setting of display RAM.
Y address (upper) [3_H]	0	1	1	0	0	0	0	0	0	1	1	AY_7	AY_6	AY_5	AY_4	Y address setting of display RAM.
Display start line set (lower) [4_H]	0	1	1	0	0	0	0	0	1	0	0	LA_3	LA_2	LA_1	LA_0	RAM Y address setting corresponds to scan start line of common driver.
Display start line set (upper) [5_H]	0	1	1	0	0	0	0	0	1	0	1	LA_7	LA_6	LA_5	LA_4	RAM Y address setting corresponds to scan start line of common driver.
N line inversion set (lower) [6_H]	0	1	1	0	0	0	0	0	1	1	0	N_3	N_2	N_1	N_0	quantity setting of line inversion
N line inversion set (upper) [7_H]	0	1	1	0	0	0	0	0	1	1	1	N_7	N_6	N_5	N_4	quantity setting of line inversion
Display control(1) [8_H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: common shift direction set, MON: BW/gradation display, ALLON: all on , ON/OFF: display ON/OFF control
Display control(2) [9_H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: display positive / negative , NLIN: n line inversion ON/OFF, SWAP: display data swap , REF: segment positive / negative
Increment control [A_H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: window selection, AIM: increment timing selection, AYI:Y increment, AXI:X increment
Power control [B_H]	0	1	1	0	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: internal OP Amp. ON, HALT: power save DCON: boosting circuit ON, ACL: reset
LCD duty set [C_H]	0	1	1	0	0	0	0	1	1	0	0	DS_3	DS_2	DS_1	DS_0	LCD driver duty ratio set
Boosting coefficient set [D_H]	0	1	1	0	0	0	0	1	1	0	1	*	VU_2	VU_1	VU_0	Boosting times set
bias ratio set [E_H]	0	1	1	0	0	0	0	1	1	1	0	*	B_2	B_1	B_0	LCD drive bias set
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

INSTRUCTION TABLE (2)

INSTRUCTION	CODE (80 series I/F)							code								function
	CS	RS	RD	WR	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette R_0 / R_0 set (lower) $[0_H]$	0	1	1	0	0	0	1	0	0	0	0	PR_{07}/ PR_{03}	PR_{06}/ PR_{02}	PR_{05}/ PR_{01}	PR_{04}/ PR_{00}	Value setting on gradation palette R_0(PS=0) / R_8(PS=1)
Gradation palette R_0 / R_8 set (upper) $[1_H]$	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PR_{04}/ PR_{04}	Value setting on gradation palette R_0 (PS=0) / R_8(PS=1)
Gradation palette R_1 / R_9 set (lower) $[2_H]$	0	1	1	0	0	0	1	0	0	1	0	PR_{17}/ PR_{13}	PR_{16}/ PR_{12}	PR_{15}/ PR_{11}	PR_{14}/ PR_{10}	Value setting on gradation palette R_1(PS=0) / R_9(PS=1)
Gradation palette R_1 / R_9 set (upper) $[3_H]$	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PR_{14}/ PR_{14}	Value setting on gradation palette R_1(PS=0) / R_9(PS=1)
Gradation palette R_2 / R_{10} set (lower) $[4_H]$	0	1	1	0	0	0	1	0	1	0	0	PR_{27}/ PR_{23}	PR_{26}/ PR_{22}	PR_{25}/ PR_{21}	PR_{24}/ PR_{20}	Value setting on gradation palette R_2(PS=0) / R_{10} (PS=1)
Gradation palette R_2 / R_{10} set (upper) $[5_H]$	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PR_{24}/ PR_{24}	Value setting on gradation palette R_2(PS=0) / R_{10} (PS=1)
Gradation palette R_3 / R_{11} set (lower) $[6_H]$	0	1	1	0	0	0	1	0	1	1	0	PR_{37}/ PR_{33}	PR_{36}/ PR_{32}	PR_{35}/ PR_{31}	PR_{34}/ PR_{30}	Value setting on gradation palette R_3(PS=0) / R_{11} (PS=1)
Gradation palette R_3 / R_{11} set (upper) $[7_H]$	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PR_{34}/ PR_{34}	Value setting on gradation palette R_3(PS=0) / R_{11} (PS=1)
Gradation palette R_4 / R_{12} set (lower) $[8_H]$	0	1	1	0	0	0	1	1	0	0	0	PR_{47}/ PR_{43}	PR_{46}/ PR_{42}	PR_{45}/ PR_{41}	PR_{44}/ PR_{40}	Value setting on gradation palette R_4(PS=0) / R_{12} (PS=1)
Gradation palette R_4 / R_{12} set (upper) $[9_H]$	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PR_{44}/ PR_{44}	Value setting on gradation palette R_4(PS=0) / R_{12} (PS=1)
Gradation palette R_5 / R_{13} set (lower) $[A_H]$	0	1	1	0	0	0	1	1	0	1	0	PR_{57}/ PR_{53}	PR_{56}/ PR_{52}	PR_{55}/ PR_{51}	PR_{54}/ PR_{50}	Value setting on gradation palette R_5(PS=0) / R_{13} (PS=1)
Gradation palette R_5 / R_{13} set (upper) $[B_H]$	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PR_{54}/ PR_{54}	Value setting on gradation palette R_5(PS=0) / R_{13} (PS=1)
Gradation palette R_6 / R_{14} set (lower) $[C_H]$	0	1	1	0	0	0	1	1	1	0	0	PR_{67}/ PR_{63}	PR_{66}/ PR_{62}	PR_{65}/ PR_{61}	PR_{64}/ PR_{60}	Value setting on gradation palette R_6(PS=0) / R_{14} (PS=1)
Gradation palette R_6 / R_{14} set (upper) $[D_H]$	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PR_{64}/ PR_{64}	Value setting on gradation palette R_6(PS=0) / R_{14} (PS=1)
RE register set $[F_H]$	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_1	RE_2	RE_1	RE_0	RE flag setting

INSTRUCTION TABLE (3)

INSTRUCTION	CODE (80 series I/F)							code								function
	CS	RS	RD	WR	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette R_7 / R_{15} set (lower) $[0_H]$	0	1	1	0	0	1	0	0	0	0	0	PR_{17}/ PR_{03}	PR_{16}/ PR_{02}	PR_{15}/ PR_{01}	PR_{14}/ PR_{00}	Value setting on gradation palette R_7(PS=0) / R_{15}(PS=1)
Gradation palette R_7 / R_{15} set (upper) $[1_H]$	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PR_{14}/ PR_{04}	Value setting on gradation palette R_7(PS=0) / R_{15}(PS=1)
Gradation palette G_8 / G_8 set (lower) $[2_H]$	0	1	1	0	0	1	0	0	0	1	0	PG_{17}/ PG_{03}	PG_{16}/ PG_{02}	PG_{15}/ PG_{01}	PG_{14}/ PG_{00}	Value setting on gradation palette G_8(PS=0) / G_8(PS=1)
Gradation palette G_8 / G_8 set (upper) $[3_H]$	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PG_{14}/ PG_{04}	Value setting on gradation palette G_8(PS=0) / G_8(PS=1)
Gradation palette G_9 / G_9 set (lower) $[4_H]$	0	1	1	0	0	1	0	0	1	0	0	PG_{17}/ PG_{03}	PG_{16}/ PG_{02}	PG_{15}/ PG_{01}	PG_{14}/ PG_{00}	Value setting on gradation palette G_9(PS=0) / G_9(PS=1)
Gradation palette G_9 / G_9 set (upper) $[5_H]$	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PG_{14}/ PG_{04}	Value setting on gradation palette G_9(PS=0) / G_9(PS=1)
Gradation palette G_{10} / G_{10} set (lower) $[6_H]$	0	1	1	0	0	1	0	0	1	1	0	PG_{17}/ PG_{03}	PG_{16}/ PG_{02}	PG_{15}/ PG_{01}	PG_{14}/ PG_{00}	Value setting on gradation palette G_{10}(PS=0) / G_{10}(PS=1)
Gradation palette G_{10} / G_{10} set (upper) $[7_H]$	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PG_{14}/ PG_{04}	Value setting on gradation palette G_{10}(PS=0) / G_{10}(PS=1)
Gradation palette G_{11} / G_{11} set (lower) $[8_H]$	0	1	1	0	0	1	0	1	0	0	0	PG_{17}/ PG_{03}	PG_{16}/ PG_{02}	PG_{15}/ PG_{01}	PG_{14}/ PG_{00}	Value setting on gradation palette G_{11}(PS=0) / G_{11}(PS=1)
Gradation palette G_{11} / G_{11} set (upper) $[9_H]$	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PA_{14}/ PG_{04}	Value setting on gradation palette G_{11}(PS=0) / G_{11}(PS=1)
Gradation palette G_{12} / G_{12} set (lower) $[A_H]$	0	1	1	0	0	1	0	1	0	1	0	PG_{17}/ PG_{03}	PG_{16}/ PG_{02}	PG_{15}/ PG_{01}	PG_{14}/ PG_{00}	Value setting on gradation palette G_{12}(PS=0) / G_{12}(PS=1)
Gradation palette G_{12} / G_{12} set (upper) $[B_H]$	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PG_{14}/ PG_{04}	Value setting on gradation palette G_{12}(PS=0) / G_{12}(PS=1)
Gradation palette G_{13} / G_{13} set (lower) $[C_H]$	0	1	1	0	0	1	0	1	1	0	0	PG_{17}/ PG_{03}	PG_{16}/ PG_{02}	PG_{15}/ PG_{01}	PG_{14}/ PG_{00}	Value setting on gradation palette G_{13}(PS=0) / G_{13}(PS=1)
Gradation palette G_{13} / G_{13} set (upper) $[D_H]$	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PG_{14}/ PG_{04}	Value setting on gradation palette G_{13}(PS=0) / G_{13}(PS=1)
RE register set $[F_H]$	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag setting

INSTRUCTION TABLE (4)

INSTRUCTION	CODE (80 series I/F)							code								function
	CS	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette G_0 / G_{16} set (lower) [0_H]	0	1	1	0	0	1	1	0	0	0	0	PG_{03}/ PG_{103}	PG_{02}/ PG_{102}	PG_{01}/ PG_{101}	PG_{00}/ PG_{100}	Value setting on gradation palette G_0(PS=0) / G_{16}(PS=1)
Gradation palette G_0 / G_{16} set (upper) [1_H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PG_{04}/ PG_{104}	Value setting on gradation palette G_0(PS=0) / G_{16}(PS=1)
Gradation palette G_1 / G_{17} set (lower) [2_H]	0	1	1	0	0	1	1	0	0	1	0	PG_{13}/ PG_{113}	PG_{12}/ PG_{112}	PG_{11}/ PG_{111}	PG_{10}/ PG_{110}	Value setting on gradation palette G_1(PS=0) / G_{17}(PS=1)
Gradation palette G_1 / G_{17} set (upper) [3_H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PG_{14}/ PG_{114}	Value setting on gradation palette G_1(PS=0) / G_{17}(PS=1)
Gradation palette B_0 / B_8 set (lower) [4_H]	0	1	1	0	0	1	1	0	1	0	0	PB_{03}/ PB_{183}	PB_{02}/ PB_{182}	PB_{01}/ PB_{181}	PB_{00}/ PB_{180}	Value setting on gradation palette B_0(PS=0) / B_8(PS=1)
Gradation palette B_0 / B_8 set (upper) [5_H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PB_{04}/ PB_{184}	Value setting on gradation palette B_0(PS=0) / B_8(PS=1)
Gradation palette B_1 / B_9 set (lower) [6_H]	0	1	1	0	0	1	1	0	1	1	0	PB_{13}/ PB_{193}	PB_{12}/ PB_{192}	PB_{11}/ PB_{191}	PB_{10}/ PB_{190}	Value setting on gradation palette B_1(PS=0) / B_9(PS=1)
Gradation palette B_1 / B_9 set (upper) [7_H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PB_{14}/ PB_{194}	Value setting on gradation palette B_1(PS=0) / B_9(PS=1)
Gradation palette B_2 / B_{10} set (lower) [8_H]	0	1	1	0	0	1	1	1	0	0	0	PB_{23}/ PB_{203}	PB_{22}/ PB_{202}	PB_{21}/ PB_{201}	PB_{20}/ PB_{200}	Value setting on gradation palette B_2(PS=0) / B_{10}(PS=1)
Gradation palette B_2 / B_{10} set (upper) [9_H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PB_{24}/ PB_{204}	Value setting on gradation palette B_2(PS=0) / B_{10}(PS=1)
Gradation palette B_3 / B_{11} set (lower) [A_H]	0	1	1	0	0	1	1	1	0	1	0	PB_{33}/ PB_{213}	PB_{32}/ PB_{212}	PB_{31}/ PB_{211}	PB_{30}/ PB_{210}	Value setting on gradation palette B_3(PS=0) / B_{11}(PS=1)
Gradation palette B_3 / B_{11} set (upper) [B_H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PB_{34}/ PB_{214}	Value setting on gradation palette B_3(PS=0) / B_{11}(PS=1)
Gradation palette B_4 / B_{12} set (lower) [C_H]	0	1	1	0	0	1	1	1	1	0	0	PB_{43}/ PB_{223}	PB_{42}/ PB_{222}	PB_{41}/ PB_{221}	PB_{40}/ PB_{220}	Value setting on gradation palette B_4(PS=0) / B_{12}(PS=1)
Gradation palette B_4 / B_{12} set (upper) [D_H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PB_{44}/ PB_{224}	Value setting on gradation palette B_4(PS=0) / B_{12}(PS=1)
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_1	RE_2	RE_1	RE_0	RE flag setting

INSTRUCTION TABLE (5)

INSTRUCTION	CODE (80 series I/F)							code								function
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette B_0 /B_{13} set (lower) [0_H]	0	1	1	0	1	0	0	0	0	0	0	PB_{07}/ PB_{03}	PB_{06}/ PB_{02}	PB_{05}/ PB_{01}	PB_{04}/ PB_{00}	Value setting on gradation palette B_0(PS=0) / B_{13}(PS=1)
Gradation palette B_1 /B_{13} set (upper) [1_H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PB_{08}/ PB_{04}	Value setting on gradation palette B_1(PS=0) / B_{13}(PS=1)
Gradation palette B_2 /B_{14} set (lower) [2_H]	0	1	1	0	1	0	0	0	0	1	0	PB_{17}/ PB_{13}	PB_{16}/ PB_{12}	PB_{15}/ PB_{11}	PB_{14}/ PB_{10}	Value setting on gradation palette B_2(PS=0) / B_{14}(PS=1)
Gradation palette B_3 /B_{14} set (upper) [3_H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PB_{18}/ PB_{14}	Value setting on gradation palette B_3(PS=0) / B_{14}(PS=1)
Gradation palette B_7 /B_{15} set (lower) [4_H]	0	1	1	0	1	0	0	0	1	0	0	PB_{77}/ PB_{73}	PB_{76}/ PB_{72}	PB_{75}/ PB_{71}	PB_{74}/ PB_{70}	Value setting on gradation palette B_7(PS=0) / B_{15}(PS=1)
Gradation palette B_7 /B_{15} set (upper) [5_H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PB_{78}/ PB_{74}	Value setting on gradation palette B_7(PS=0) / B_{15}(PS=1)
Display start command set [6_H]	0	1	1	0	1	0	0	0	1	1	0	SC_3	SC_2	SC_1	SC_0	Common driver scan start set
Display control signals output enable [7_H]	0	1	1	0	1	0	0	0	1	1	1	*	*	*	SON	Output Enable of CL,FLM,FR,CLK signals
Display selection [8_H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : variable 16 /fixed 9 gray mode selection C256 : 256 color Mode FDC : boost clock control
RAM data length set [9_H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : high speed write in at 8 bit access mode ABS : effective 12 bit RAM selection CKS : oscillator selection WLS : RAM access length 8 /16 bit
Electric volume control (lower) [A_H]	0	1	1	0	1	0	0	1	0	1	0	DV_3	DV_2	DV_1	DV_0	Electric volume level setting (lower)
Electric volume control (upper) [B_H]	0	1	1	0	1	0	0	1	0	1	1	*	DV_6	DV_5	DV_4	Electric volume level setting (upper)
Oscillator Rf control [D_H]	0	1	1	0	1	0	0	1	1	0	1	-	RF_2	RF_1	RF_0	RF: control the feedback resistor of oscillator
discharge [E_H]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	Discharge the Capacitors of the V_{LCD}, V_1~V_4
RE register set [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_1	RE_2	RE_1	RE_0	RE flag setting
Address set for internal register reading [C_H]	0	1	1	0	1	0	0	1	1	0	0	Address for register reading				Address set for internal register reading out.
Internal register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Internal register read out

INSTRUCTION TABLE (6)

INSTRUCTION	CODE (80 series I/F)							code								function
	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Window end X address set (lower) $[0_H]$	0	1	1	0	1	0	1	0	0	0	0	EX_3	EX_2	EX_1	EX_0	X end address under window mode
Window end X address set (upper) $[1_H]$	0	1	1	0	1	0	1	0	0	0	1	EX_7	EX_6	EX_5	EX_4	X end address under window mode
Window end Y address set (lower) $[2_H]$	0	1	1	0	1	0	1	0	0	1	0	EY_3	EY_2	EY_1	EY_0	Y end address under window mode
Window end Y address set (upper) $[3_H]$	0	1	1	0	1	0	1	0	0	1	1	EY_7	EY_6	EY_5	EY_4	Y end address under window mode
Line inversion start address (lower) $[4_H]$	0	1	1	0	1	0	1	0	1	0	0	LS_3	LS_2	LS_1	LS_0	Start line address set under line inversion mode
Line inversion start address (upper) $[5_H]$	0	1	1	0	1	0	1	0	1	0	1	LS_7	LS_6	LS_5	LS_4	Start line address set under line inversion mode
Line inversion end address (lower) $[6_H]$	0	1	1	0	1	0	1	0	1	1	0	LE_3	LE_2	LE_1	LE_0	End line address set under line inversion mode
Line inversion end address (upper) $[7_H]$	0	1	1	0	1	0	1	0	1	1	1	LE_7	LE_6	LE_5	LE_4	End line address set under line inversion mode
Line inversion control $[8_H]$	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LR EV	BT: blink type set LREV: line inversion ON/OFF
Gradation palette setting selection $[9_H]$	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	Upper/lower 8 gradation palette
PWM mode control $[A_H]$	0	1	1	0	1	0	1	1	0	1	0	PW MS	PW MA	PW MB	PW MC	PWM mode selection
RE register set $[F_H]$	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_4	RE_2	RE_1	RE_0	RE flag setting

4.3 Instruction Descriptions

WRITE DIPLAY DATA ON RAM

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display RAM write data							

Writing the 8-bit display RAM data at specified X, Y address.

READ DISPLAY DATA FROM RAM

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display RAM read data							

Reading out the 8-bit display RAM data from specified X, Y address.
One dummy read cycle is needed after X, Y address is set.

X ADDRESS REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX_3	AX_2	AX_1	AX_0

(reset :AX_3~AX_0=0_H, read address:0_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	AX_7	AX_6	AX_5	AX_4

(reset :AX_7~AX_4=0_H, read address:1_H)

Setting the X direction address set. Set the lower 4-bits first and then upper 4-bits later.
Please set from lower bit.

Y ADDRESS REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY_3	AY_2	AY_1	AY_0

(reset:AY_3~AY_0=0_H, read address:2_H)

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	AY_7	AY_6	AY_5	AY_4

(reset:AY_7~AY_4=0_H, read address:3_H)

Setting the Y direction address set. Set the lower 4-bits first and then upper 4-bits later.
Please set from lower bit.

00_H~$A1_H$ is valid range at Y address (AY_7~AY_0). Do not use $A2_H$~FF_H range.

DISPLAY START LINE REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :LA_3~LA_0=0_H, read address:4_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA_3	LA_2	LA_1	LA_0

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :LA_7~LA_4=0_H, read address:5_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	LA_7	LA_6	LA_5	LA_4

Setting the display line address, the address that was stored at the start line register becomes display line at COM_0 line of LCD panel.

The display of LCD panel is done from line address value to the direction of increase.

LA_7	LA_6	LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				⋮				⋮
1	0	1	0	0	0	0	1	161

N-LINE INVERSION REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :N_3~N_0=0_H, read address:6_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N_3	N_2	N_1	N_0

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :N_7~N_4=0_H, read address:7_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	N_7	N_6	N_5	N_4

Setting line number of LCD inversion to register. Setting range is from 2 to 161. N line inversion register can be effective only when N line inversion command ON (NLIN="1").

If N line inversion command OFF (NLIN="0"), the polarity of LCD driving voltage is inverted by every another frame.

N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	Inversion line number
0	0	0	0	0	0	0	0	forbidden *
0	0	0	0	0	0	0	1	2
				:				:
1	0	1	0	0	0	0	0	161

n=N-1

** N_0~N_7="0" is forbidden.*

DISPLAY CONTROL (1) REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF

(reset:{SHIFT, MON, ALLON, ON/OFF}=0_H, read address:8_H)

It's various control setting of display.

a) ON/OFF command
Display ON/OFF control
ON/OFF="0": display OFF (all ports are V_{SS} level)
ON/OFF="1": display ON

b) ALLON command
Setting all display data to "1" with independence of RAM data. This command has higher priority than positive/negative display command. RAM data is not changed.

ALLON="0": normal display state
ALLON="1": turn on all the pixel

c) MON command
BW display / gradation display selection
MON="0": gradation display mode
MON="1": BW display mode

d) SHIFT command
Selection command of the scan data shift direction at common driver output.
SHIFT="0":$COM_0 \rightarrow COM_{161}$ shift
SHIFT="1":$COM_{161} \rightarrow COM_0$ shift

DISPLAY CONTROL (2) REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

(reset:{REV, NLIN, SWAP, REF}=0_H, read address:9_H)
It's various control setting of display.

a) REF command

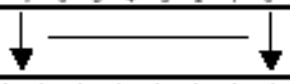
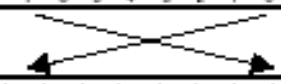
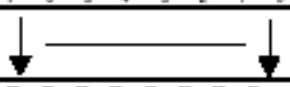
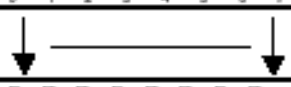
When CPU tries to access display RAM, the relation between X address and write data is changed by command, normal or headfirst.

The output sequence of display data to segment driver can be controlled by register setting. The IC can be placed in panel with less constraint at application.

b) SWAP command

When CPU tries to access display RAM, the display data to be written can be swapped.

SWAP="0": Normal state, D_7--D_0 or D_{15}--D_0 are written to the RAM as it is.
SWAP="1": SWAP mode ON state. The swapped data of D_7--D_0 or D_{15}--D_0 are written to the RAM

	SWAP="0"	SWAP="1"
Write data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
		
Internal data	d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	d_0 d_1 d_2 d_3 d_4 d_5 d_6 d_7
		
Read data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

c) NLIN command

n line inversion ON/OFF control command

NLIN="0": n line inversion OFF. Polarity signal, FR is inverted every other frame.
NLIN="1": n line inversion ON. The n lines are inverted according to the contents of n line inversion register.

d) REV command

The reverse turn control between RAM data and display data is defined by this command.

REV="0": The display data are reflected the RAM data as it is.
REV="1": The display data are reflected the reverse turned data of RAM data

INCREMENT CONTROL REGISTER SET

$\overline{CS}$	$\overline{RS}$	$\overline{RD}$	WR	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	WIN	AIM	AYI	AXI

(reset :{WIN,AIM,AYI,AXI}=0_H, read address :A_H)

Sets the increment mode when RAM data is accessed.

Per RAM write or read access, the increment or non-increment settings of X and Y address counter are possible by AIM, AYI, AXI register setting. By this register setting. when accessing consecutive RAM areas by read or write, the address increment operation is possible without setting the read or write address case by case.

After setting the auto increment register, the X, Y address should be set lower bits first.

Please revise X, Y addresses register after increment register setting.

When WIN register is set to "1", the CPU accesses specified area of display RAM. In this case X, Y address should be used with auto increment mode set (AXI="1", AYI="1").

The window area setting is not valid without X,Y address auto increment mode.

WIN="0": normal display RAM access
WIN="1": window area access at display RAM

The window area of RAM to be accessed is defined by setting the start X, Y address and end X, Y address.

When accessing display with window area mode, please set WIN command (WIN="1") first, and then X, Y start address and then X, Y window end address.

The relationship between AIM, AYI, AXI register and X, Y address increment mode is as follow.

AIM	Increment timing selection	Remark
0	Both case of writing in and read out display RAM data	①
1	Only when writing in display RAM (read modify)	②

notice①) This mode is valid when read or write is performed on consecutive RAM location.

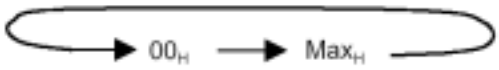
notice②) This mode is valid when read out consecutive data and modifying the data and then write them in again or read → write per access.

AYI	AXI	Increment timing selection	Remark
0	0	No increment	①
0	1	X address auto increment	②
1	0	Y address auto increment	③
1	1	X, Y address auto increment	④

notice①) Regardless of AIM setting, no auto increment for X and Y address

notice②) According to AIM setting, auto increment only for X address.

And X address is increased as followed loop according to REF register(SEG output direction setting register) value.



※) Please refer to 「RAM address bitmap」 in 「(10) relation between display RAM and address」

notice③) According to AIM setting, auto increment only for Y address.
Y address is increased as followed loop regardless of REF register.

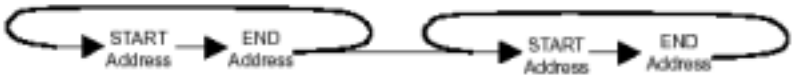
notice④) According to AIM setting, auto increment for X and Y address
X address is increased to Max_H first and then Y address is increased later.

X address Y address

*) Please refer to 「RAM address bitmap」 in 「(10) relation between display RAM and address」

When AYI and AXI were set as "1", the address should be set X address and then Y address later, anything else setting is forbidden.

And when X, Y auto increment mode operating, window access is possible. When window mode is selected (WIN ="1"), address is increased as following loop.



X address Y address

a) 8 bit access mode
The increment operating is as above description.

b) 16 bit access mode
Address is increased after access.
X address is increased as (00_H, 01_H,……$7E_H$, $7F_H$) sequence.

POWER CONTROL REGISTER SET

(32-10) POWER CONTROL REGISTER SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

(reset : {AMPON,HALT,DCON,ACL} = 0_H, read address : B_H)

a) ACL COMMAND

This command initializes internal circuit.

ACL="0": normal state

ACL="1": initialization ON

Just after the execution of ACL command (ACL="1"), the value of D_0 (ACL) bit is set to "1". But as the initialization process goes on internally, D_0 is reset to "0".

When ACL command is executed, using internal display clock (clock from internal oscillator or from external resistor oscillation mode) produces the internal reset signal.

So, after ACL command is executed, it needs to WAIT at least 2 period of the oscillation clock for next process beginning.

b) DCON COMMAND

ON/OFF the internal voltage boosting circuit.

DCON="0": boosting circuit OFF

DCON="1": boosting circuit ON

c) HALT COMMAND

Power save mode ON/OFF control

HALT="0": normal state

HALT="1": power save state

The power consumption is decreased near static current at power save mode.

States of each sub-block in power save mode are as follow.

- Oscillator, built-in power supply block stop.
- Stop driving LCD panel and the drive ports of segment and common are all set to V_{SS} level.
- Clock input from OSC_1 port is disabled.
- Display RAM data are conserved.
- Operational modes are preserved as those before power save command was executed.
- V_{LCD}, $V_1 \sim V_4$ become high impedance state.

Make display OFF state before power save mode by HALT command.

And when returning from power save mode, you should display ON after oscillator, power circuit is activated stable.

After display OFF and HALT command, if the display is turned ON before oscillator and power circuit is not activated stable, wrong display can be appeared.

d) AMPON COMMAND

ON/OFF the internal OP. amplifier circuit of power block (voltage regulator block, electric volume, voltage converting circuit).

AMPON="0" : internal power circuit OP. Amplifier OFF

AMPON="1" : internal power circuit OP. Amplifier ON

LCD DUTY SET

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	DS_3	DS_2	DS_1	DS_0

(reset :{ DS_3,DS_2,DS_1,DS_0}=0_H, read address :C_H)

LCD display duty setting

DS_3	DS_2	DS_1	DS_0	duty
0	0	0	0	Y direction 162 dot width display, 1/163 duty
0	0	0	1	Y direction 160 dot width display, 1/160 duty
0	0	1	0	Y direction 144 dot width display, 1/144 duty
0	0	1	1	Y direction 133 dot width display, 1/133 duty
0	1	0	0	Y direction 128 dot width display, 1/128 duty
0	1	0	1	Y direction 112 dot width display, 1/112 duty
0	1	1	0	Y direction 96 dot width display, 1/96 duty
0	1	1	1	Y direction 80 dot width display, 1/80 duty
1	0	0	0	Y direction 72 dot width display, 1/72 duty
1	0	0	1	Y direction 64 dot width display, 1/64 duty
1	0	1	0	Y direction 56 dot width display, 1/56 duty
1	0	1	1	Y direction 48 dot width display, 1/48 duty
1	1	0	0	Y direction 40 dot width display, 1/40 duty
1	1	0	1	Y direction 32 dot width display, 1/32 duty
1	1	1	0	Y direction 24 dot width display, 1/24 duty
1	1	1	1	Y direction 16 dot width display, 1/16 duty

※ The 163'rd status of COM and SEG port under 1/163 duty
COM: all output non-display state
SEG: the same data with 162'nd line data

Partial display is possible by setting duty with discretion.

BOOSTING COEFFICIENT SETTING

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :{VU_2~VU_0}=0_H, read address :D_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

coefficient setting of boosting circuit

VU_2	VU_1	VU_0	Boosting multiple
0	0	0	No boosting *
0	0	1	2 times boosting operation
0	1	0	3 times boosting operation
0	1	1	4 times boosting operation
1	0	0	5 times boosting operation
1	0	1	6 times boosting operation
1	1	0	7 times boosting operation
1	1	1	forbidden

*V_{REG} amplifier gain is "1".

BIAS REGISTER SETTING

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :{B_2~B_0}=0_H, read address :E_H) * : "Don't care."

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

This register controls the bias ratio. From 1/12 to 1/5 biases can be selected by B_2, B_1 and B_0 register.

B_2	B_1	B_0	bias
0	0	0	Operating under 1/9 bias
0	0	1	Operating under 1/8 bias
0	1	0	Operating under 1/7 bias
0	1	1	Operating under 1/6 bias
1	0	0	Operating under 1/5 bias
1	0	1	Operating under 1/10 bias
1	1	0	Operating under 1/11 bias
1	1	1	Operating under 1/12 bias

REFLAG STATE REGISTER SETTING

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST_0	RE_2	RE_1	RE_0

(reset :{TST_0,RE_2,RE_1,RE_0}=0_H, read address : F_H)

Setting the register of command extension registers (RE_2, RE_1 and RE0). When accessing each command register, the extension register, RE corresponding flag should be set first, and then access it. The TST_0 register is that for test, and so please set to "0".

DISPLAY START COMMAND SET

$\overline{CS}$	$\overline{RS}$	RD	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	SC_3	SC_2	SC_1	SC_0

(reset :{ SC_3, SC_2, SC_1, SC_0}=0_H, read address :6_H)

Setting the scan start output of common driver.

SC_3	SC_2	SC_1	SC_0	SHIFT=0 starting point of COM.	SHIFT=1 starting point of COM.
0	0	0	0	COM_0~	COM_{161}~
0	0	0	1	COM_1~	COM_{160}~
0	0	1	0	COM_9~	COM_{152}~
0	0	1	1	COM_{14}~	COM_{146}~
0	1	0	0	COM_{17}~	COM_{144}~
0	1	0	1	COM_{25}~	COM_{136}~
0	1	1	0	COM_{33}~	COM_{128}~
0	1	1	1	COM_{41}~	COM_{120}~
1	0	0	0	COM_{49}~	COM_{112}~
1	0	0	1	COM_{57}~	COM_{104}~
1	0	1	0	COM_{65}~	COM_{96}~
1	0	1	1	COM_{73}~	COM_{88}~
1	1	0	0	COM_{122}~	COM_{39}~
1	1	0	1	COM_{130}~	COM_{31}~
1	1	1	0	COM_{138}~	COM_{23}~
1	1	1	1	COM_{146}~	COM_{15}~

SHIFT=0:COM increasing direction scanning
SHIFT=1:COM decreasing direction scanning

DISPLAY SELECTION CONTROL

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	C256	FDC1	FDC2

(reset :{PWM,C256,FDC1,FDC2}=0_H, read address :8_H) * : "Don't care"

a) PWM COMMAND

Selection gradation display mode.
PWM="0": Gradation mode is selected variable 16 gradation among 32 levels (defaults).
PWM="1": Fixed 8 gradation display mode.

b) C256 COMMAND

8 bit mode (256 color) selection command.
C256="0": Variable 16 gradation selection among 32 gray level (default).
C256="1": Variable 256 color mode. 8 gradation (Palette B is only 4 gradation) selection among 32 gray level.

c) FDC1, FDC2 COMMAND

Boosting clock setting commands.

FDC1	FDC2	Boosting clock
0	0	1 times
0	1	2 times
1	0	4 times
1	1	1/2 times

RAM DATA LENGTH SETTING

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	HSW	ABS	CKS	WLS

(reset :{HSW,ABS,CKS,WLS}=0_H, read address :9_H)

HSW COMMAND:

High speed write in mode selection under 8 bit RAM access mode.

HSW="0": Write in mode with high speed OFF (default).
HSW="1": Write in mode with high speed ON.

ABS COMMAND:

Effective RAM data selection of 12 bit .
ABS="0": Normal mode (defaults).
ABS="1": ABS mode.

WLS: Selection 8 bit access or 16-bit access at RAM access. Access with 16-bit data length is effective only at RAM access. The other accesses are 8 bits access (command access).
WLS="0": RAM access is done by 8-bit data length (default).
WLS="1": RAM access is done by 16-bit data length.

CKS: Selection the oscillator.
CKS="0": internal oscillation mode (default).
CKS="1": external oscillation mode.

External oscillation mode should be used under the condition of clock input by OSC_1 port or resistor connection between OSS1 and OSC2 port. Please open OSC2 port when the source clock forced through OSC2 port.

ELECTRIC VOLUMN REGISTER SETTING

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

(read address :A_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV_0

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

(read address :B_H) *: "Don't care"
(reset :DV_6~DV_0=00_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV_6	DV_5	DV_4

Setting the electric volume code.
The voltage range is divided into 127 levels by this register.

DV_6	DV_5	DV_4	DV_3	DV_2	DV_1	DV_0	Output voltage
0	0	0	0	0	0	0	low
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	high

The output voltage of V_{REG} is determined by Eq. ①.

$$V_{REG} = V_{REF} \times N \cdots\cdots ①$$

(N: booster coefficient)
N=1 under the condition of boosting operation is not valid (booster coefficient register, VU=0_H).

The LCD driving voltage V_{LCD} is decided by V_{REG} level or electric volume value (Eq. ②).

$$V_{LCD} = 0.5 \times V_{REG} + M \times (V_{REG} - 0.5V_{REG}) / 127 \cdots\cdots ②$$

(M: DV_6~DV_0 register value)

To prevent over voltage from being generated by electric volume setting, when the register value is set to upper side of electric volume, voltage level is not changed immediately.
When the register value is set to lower side of electric volume, the voltage level is changed instantly.

OSCILLATOR CIRCUIT RF CONTROL

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

(reset :{Rf_2,Rf_1,Rf_0}=0_H, read address : D_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	Rf_2	Rf_1	Rf_0

Setting this register can change the feedback resistance of oscillator circuit.
The frame frequency is changed according to the frequency of oscillator, and the oscillation frequency is determined by the resistor value.
When you set the frame rate, please check the state of LCD display quality.

Rf_2	Rf_1	Rf_0	Feedback resistor size
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	forbidden
1	1	0	forbidden
1	1	1	forbidden

DISCHARGE CONTROL

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	*	DIS

(reset :{DIS}=0_H, read address : E_H) * : "Don't care"

The capacitors connected between V_{LCD}~V_4 and V_{SS} can be discharged by this control.
Meaningless display can be prevented when power OFF time.
Please refer to capacitor setting example.

DIS="0": discharge disable
DIS="1": starts discharge

SET READ ADDRESS OF INTERNAL REGISTER

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA_3	RA_2	RA_1	RA_0

(reset :{RA_3, RA_2, RA_1, RA_0}=B_H)

Before executing the internal register data read command the address of register to be read should be specified first. For example, when display control (1) is being read out, {RA_3, RA_2, RA_1 and RA_0} = 8_H should be specified first.

And, because selected register is corresponded with RE flag, please set RE flag first and then read out the register.

Refer to the command function description and the lists of commands for the address of each register.

INTERNAL REGISTER DATA READ

$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	RE_2	RE_1	RE_0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data read			

*: "Don't care"

This command is used to read out internal register data. Before executing this command, RE flag and the address for internal register to read should be set first.

5. Reliability

5.1 Environmental Test

Item No	Items	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200 Hrs	
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200Hrs	
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time	70°C 200Hrs (*1)	
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200Hrs (*1)	
5	High temperature / humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C 90% RH 200Hrs	
6	Temperature cycle	Endurance test applying the low and high temperature cycles. -30°C ⟷ 80°C (30min.) (30min.) 1 Cycle	10 Cycle.	
7	Vibration test	10 → 55 → 10 Hz, within 1 minute amplitude 1.5mm .	15 minutes for each direction(X,Y,Z)	
8	Drop test	Packed, 100CM free fall, (6 sides, 1corner, 3edges)		

***1) : Driving condition for operation test:**

Power supply voltage for logic system =＋3.0V

Power supply voltage for LCD system = Getting Optimum Contrast at 25°C

6. HANDLING INSTRUCTION

☐ PRECAUTION IN USE OF LCD

- Do not contact or scratch the front surface and the contact pads of an LCD panel with hard materials such as metal or glass or with one‘s nail.
- To clean the surface,wipe it gently with soft cloth dampened alcohol.
- Do not attempt to wiped off the contact pads.
- Keep LCD panels away from direct sunlight,also avoid storing them in a high-temperature&high humidity environment for a long period.
- Do not drive LCD panels by DC voltage.
- Do not expose LCD panels to organic solvent.
- Liquid in LCD is hazardous substance, any contacts with liquid crystal materials ,wash it off immediately with soap and water.
- The polarizer is easily damaged and should be handle with special care.Do‘nt press or rub it with hard objects.

☐ PRECAUTION FOR HANDLING LCM

- The LCD module contains a C-MOS LSI.To avoid damage to the LSI from static electricity generated while working,Ground your body,work/assembly areas and assembly equipment to protect the module against STATIC ELECTRICITY.
- Do not input any signal before power is turned on.
- Do not take LCM from it‘s packaging bag until it is assembled.
- Peel off the LCM protective film slowly since static electricity may be generated.
- Pay attention to the humidity of the work shop,50~60%RH is satisfactory.
- Use a non-leak iron for soldering LCM.
- Do not touch the display surface or connection terminals area with bare hands.Smudges on the display surface reduce the insulation between terminals.
- Cautions for soldering to LCM:
  Conditions for soldering I/O terminals:
  Temperature at iron tip: 280℃± 10℃.
  Soldering time : 3~4 sec./ terminal.
  Type of solder : Eutectic solder(rosin flux filled).

☐ PRECAUTION FOR STORING LCM

- To avoid degradation of the device,do not store the module under the con itions of direct sunlight,high temperature or high humidity.Keep the module in bags designed to prevent static electricity charging under low temperature / normal humidity conditions(avoid high temperature / high humidity and low temperature below 0 ℃).

☐ PRODUCTION NO. DEFINITION