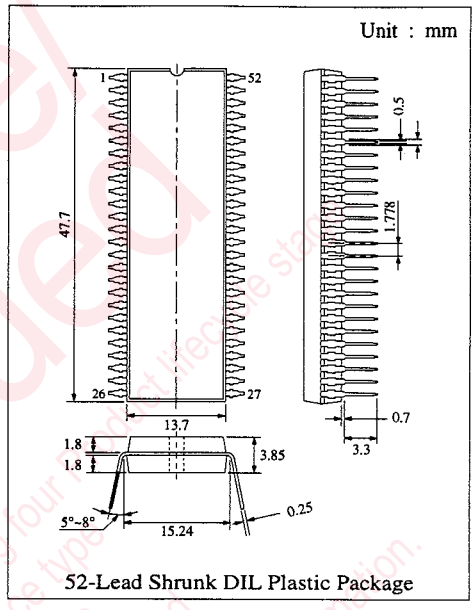
AN5607NK

PAL/NTSC Video, Chrominance, and Deflection Signal Processing IC with I²C Bus Interface



52-Lead Shrunk DIL Plastic Package

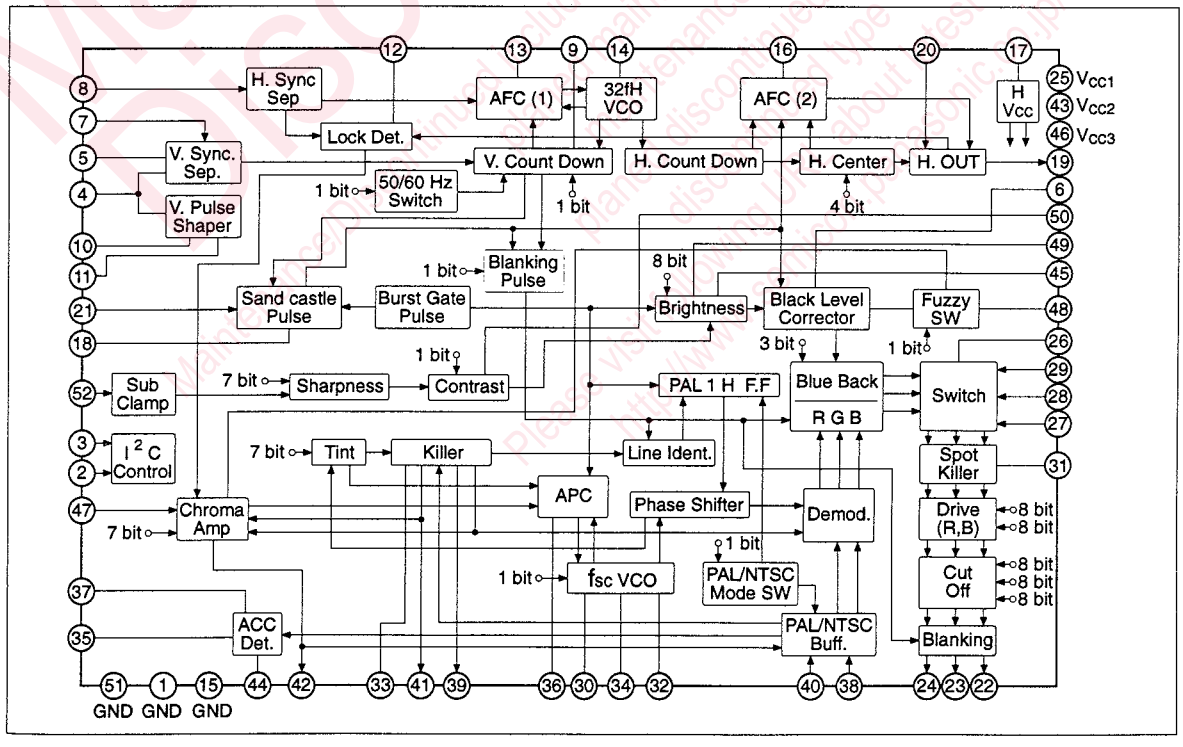
■ Description

The AN5607NK is an integrated circuit consisting of a Video, Chroma, and Synchronous Signal Processing (with I²C Bus) for use in the PAL/NTSC Colour TV.

■ Features

- PAL/NTSC Signal Processing
- External R G B Signal Input
- Can be easily combined with SECAM Decoder IC (AN5636K)
- I²C bus control for the following 11 DAC Inputs (including Sub-level Adjusts) :
  Colour, Tint (NTSC Only), Brightness, Contrast, Sharpness, H-center, RB-Drives, & RGB Cut-off
- I²C bus control for the following 8 switches : PAL/NTSC Mode Switch, 50/60Hz Switch, RGB Back Mode Switch, R-Back ON/OFF, G-Back ON/OFF, B-Back ON/OFF, Blanking Switch, 3.58/4.43MHz VCO Switch
- Built-in Y-Delay (Luminance Delay), Black-Level Expander, X-ray Protection, ACL, ABL, Colour-Killer, Spot Killer functions & Fuzzy Switch

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating			Unit
Supply Voltage	V_{CC}	V_{CC1} = 9.8	V_{CC2} = 5.5	V_{CC3} = 6.8	V
Supply Current	I_{CC}	I_{CC1} = 59	I_{CC2} = 90	I_{CC3} = 18	mA
Power Dissipation (Ta = 70°C)*refer to "Ta-P_D curve"	P_D	1480			mW
Operating Ambient Temperature	Topr	-20 ~ +70			°C
Storage Temperature	Tstg	-55 ~ +150			°C

■ Recommended Operating Range (Ta=25°C)

Item		Symbol	Range
Operating Supply Voltage Range	$V_{25-1,15,51}$	V_{CC1}	8.3V ~ 9.7V
	$V_{43-1,15,51}$	V_{CC2}	4.6V ~ 5.4V
	$V_{46-1,15,51}$	V_{CC3}	5.7V ~ 6.7V
Operating Supply Current Range		I_{17}	13mA ~ 25mA

■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test cct.	Condition	min.	typ.	max.	Unit
Circuit Current 1	I_{CC1}	1	V_{CC1}=9V, V_{CC2}=5V, Sync. input, V_{CC3}=6.2V	34.0	44.0	54.0	mA
Circuit Current 2	I_{CC2}	1	V_{CC1}=9V, V_{CC2}=5V, Sync. input, V_{CC3}=6.2V	56.0	68.0	82.0	mA
Circuit Current 3	I_{CC3}	1	V_{CC1}=9V, V_{CC2}=5V, Sync. input, V_{CC3}=6.2V	8.0	12.0	16.0	mA
Circuit Voltage	V_{17}	1	I_{17}=12mA	5.8	6.3	6.9	V
Constant Voltage Operating Resistance	R_{17}	1	V_{CC1}=9V, V_{CC2}=5V, I_{17}=12~30mA			30	Ω
Pin 47 Voltage	V_{47-51}	1	V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V	1.7	2.0	2.3	V
Pin 52 Voltage	V_{52-51}	1	V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V	2.7	3.0	3.3	V
Pin 38 Voltage	$V_{38-51(PAL)}$	1	V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V (PAL MODE)	1.9	2.2	2.5	V
Pin 40 Voltage	$V_{40-51(PAL)}$	1	V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V (PAL MODE)	1.9	2.2	2.5	V
[I^2C • DAC]							
ACK Suction Current	V_{ACK}	1	I_3=2mA			0.5	V
SCL-SDA Signal Input LOW Level	V_{LOW}	1				0.9	V
SCL-SDA Signal Input HIGH Level	V_{HIGH}	1		4.0			V
Input Signal Frequency	f_{in}	1				100	k bit/s
(1) Y-Signal Processing							
Video Input Pin Voltage	V_{52}	1	V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V, I_{17}=15mA	2.7	3.0	3.3	V
Pedestal Variation with Drive	Y_{PL-D}	1	No input, Drive : MIN/MAX, Cutoff : "18", Brightness : TYP	-400	0	400	mV
RGB Output Pedestal Level	Y_{PL}	1	No input, Drive : TYP, Cutoff : "18", Brightness : TYP	1.7	2.4	3.1	V
RGB Output Pedestal Difference Voltage (1)	$Y_{PL(B-G)}$	1	B-G	-250	0	+250	mV
RGB Output Pedestal Difference Voltage (2)	$Y_{PL(R-G)}$	1	R-G	-250	0	+250	mV
Video Voltage Gain	A_V	1	Input 0.4Vpp, Contrast : TYP, Sharpness : MIN, Brightness : TYP	4.7	5.5	6.7	Times
Video Voltage Gain Relative Ratio (1)	$A_{VB/G}$	1	Input 0.4Vpp, Contrast : TYP, Sharpness : MIN, Brightness : TYP	0.85	1.0	1.15	Times
Video Voltage Gain Relative Ratio (2)	$A_{VR/G}$	1	Input 0.4Vpp, Contrast : TYP, Sharpness : MIN, Brightness : TYP	0.85	1.0	1.15	Times

■ Electrical Characteristics (Ta=25°C) (Continue)

Item	Symbol	Test cct	Condition	min.	typ.	max.	Unit
Video Frequency Characteristics	f_{YC}	1	Attenuation at input f = 5MHz to output level at input f = 2MHz.	-7	-3		dB
Picture Quality Variable Range (1)	A_{STYP} A_{SMIN}	1	Input sine wave 0.1Vpp, f = 3.3MHz, Brightness : "B0", Sharpness = TYP/MIN	4.0	7.0	10.0	dB
Black Level Variation with Aperture Control Change	Y_{PL-S}	1	No input, pedestal measurement. Sharpness = MAX/MIN	-50		50	mV
Contrast Ratio	e_{MAX} e_{MIN}	1	Input sine wave 0.2Vpp, f = 2MHz, Brightness : "B0", Contrast = MAX/MIN	18	21.5	29	dB
RGB Output Tracking (1)	$e_{OT(1)}$	1	Contrast = 20→60	7	10	13	dB
RGB Output Tracking (2)	$e_{OT(2)}$	1	R/B	0.96	1.0	1.04	Times
RGB Output Tracking (3)	$e_{OT(3)}$	1	G/B	0.96	1.0	1.04	Times
Brightness Variable Range	B	1	Input 0.4Vpp, Brightness = MIN~MAX, Measure pedestal level.	2.1	2.6	3.1	V
Brightness Control Sensitivity	B_G	1	Brightness = 5F→9F	0.55	0.85	1.15	V
Brightness Relative Control Sensitivity (1)	$B_{R/G}$	1	Brightness = 5F→9F R/G	0.85	1.0	1.15	Times
Brightness Relative Control Sensitivity (2)	$B_{B/G}$	1	Brightness = 5F→9F B/G	0.85	1.0	1.15	Times
DC Restoration Rate	T_{DC}	1	Input 0.4Vpp, Contrast = TYP, Sharpness : MIN, APL 10 ~ 90%	91	95	105	%
RGB Output BLK Level	Y_{BL}	1	V_{CC1}=9V, V_{CC2}=5V, H,VBLK level when V_{CC3}=6.2V, I_{17}=15mA	0.5	1.0	1.5	V
Black Level Correction							
Correction Quantity (Amplitude Variable) (1)	V_{BL} (b)-(a)	1	Input signal : All black, (a) Pin 48 : External RC, (b) Pin 48 : 9V	-100	0	100	mV
Correction Quantity (Amplitude Variable) (2)	V_{BL} (a)-(c)	1	Input signal : All black, (c) Pin 48 : 3V, R = 220k	0.45	0.75	1.05	V
Correction Quantity (Amplitude Variable) (3)	V_{BL} (b)-(a)	1	Adjust output amplitude to 0.6$V_{OP.}$, R = 220k	100	300	500	mV
Correction Quantity (Amplitude Variable) (4)	V_{BL} (b)-(a)	1	Adjust output amplitude to 1.5$V_{OP.}$, R = 220k	-100	0	150	mV
Y-Signal Delay Time	τ_D	1	Input stair step 0.4Vpp.	150	220	270	nsec
ACL Characteristic	ACL	1	Input stair step, Pin 50 = 3.0 ~ 3.4V.	6.5	8.5	10.5	dB/V
ABL Characteristic	ABL	1	Pedestal level variation with Pin 49 = 3.0 ~ 3.4V.	0.9	1.4	1.9	V/V
(2) ON Screen Circuit							
Ys Threshold	e_{STH}	1	Switch level of Pin 26.	0.45	0.7	0.95	V
External RGB Frequency Characteristic	e_{fRGB}	1	Input sine wave 0.2Vpp, Y_S = 1V, f = 2MHz ~ 5MHz	-4	-2		dB
External RGB Output DC Voltage	E_{OEXT}	1	Input/No input Y_S = 1V, Cutoff ="18", Measure B	1.45	2.15	2.85	V
External RGB Output DC Difference Voltage (1)	E_{OEXT} (R-B)	1	Input/No input Y_S = 1V, Cutoff ="18", Measure B, R-B.	-250	0	250	mV
External RGB Output DC Difference Voltage (2)	E_{OEXT} (G-B)	1	Input/No input Y_S = 1V, Cutoff ="18", Measure B, G-B.	-250	0	250	mV
Internal/External Pedestal Difference Voltage	E_{OYS}	1	Measure pedestal level (Inside-Outside) difference at Y_S = 0.4(OFF)/1.2V(ON).	-50	300	600	mV
External RGB Output Signal Level	e_{EXT}	1	Input sine wave 0.2Vpp f = 2MHz, Contrast = MAX, Measure B.	4.6	6.6	8.6	dB
External RGB Relative Output Signal Level (1)	e_{EXT} G/B	1	Input sine wave 0.2Vpp f = 2MHz, Contrast = MAX, Measure B, G/B.	0.9	1	1.1	Times
External RGB Relative Output Signal Level (2)	e_{EXT} R/B	1	Input sine wave 0.2Vpp f = 2MHz, Contrast = MAX, Measure B, G/B.	0.9	1	1.1	Times
Internal/External Crosstalk	e_{CT}	1	Input sine wave Y_S = 1.2V, 0.4Vpp, f = 1MHz, External/Internal crosstalk			-45	dB
External RGB Frequency Charateristic Ratio (1)	e_{fRGB} R/B	1	Input sine wave 0.2Vpp f = 5MHz, Measure B.	0.9	1	1.1	Times

■ Electrical Characteristics (Ta=25°C) (Continue)

Item	Symbol	Test cct	Condition	min.	typ.	max.	Unit
External RGB Frequency Charateristic Ratio (2)	$e_{fRGB\ G/B}$	1	Input sine wave 0.2Vpp, f = 5MHz, Measure B, R/B, G/B.	0.9	1	1.1	Times
External RGB Output Blanking Voltage	$Y_{BLK\ (RGB)}$	1	No input when V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V, I_{17}=15mA	0.5	1.0	1.5	V
External RGB Contrast Control Characteristic	e_{EXT-C}	1	Input 2Vpp. Output ratio when Contrast = MAX/MIN	9.5	12.5	15.5	mV
(3) Colour Signal Processing Circuit							
PAL Colour Difference Output (B-Y) (1)	e_{O1}	1	Colour bar signal, Burst 150mVpp, Contrast : Colour : TYP, Brightness : "B0"	2.0	2.6	3.2	Vpp
PAL Colour Difference Output (B-Y) (2)	e_{O2}	1	Colour bar signal, Burst 150mVpp, Contrast : TYP, Colour : MAX, Brightness : "E6"	4.1	5.2	6.3	Vpp
PAL Colour Difference Output (Residual Colour) (3)	e_{O3}	1	Colour bar signal, Burst 150mVpp, Contrast : MAX, Colour : MIN			80	mVpp
PAL ACC Characteristic (1)	A_{CC1}	1	Colour bar signal, Burst 300mVpp(+6dB)	0.8	1.0	1.2	Times
PAL ACC Characteristic (2)	A_{CC2}	1	Colour bar signal, Burst 30mVpp(-14dB)	0.7	0.9	1.1	Times
PAL Demodulation Output Ratio (1)	R/B	1	Colour bar signal, Burst 150mVpp, Contrast : Colour : TYP	0.67	0.78	0.88	Times
PAL Demodulation Output Ratio (2)	G/B	1	Colour bar signal, Burst 150mVpp, Contrast : Colour : TYP	0.31	0.36	0.41	Times
PAL Demodulation Angle R	$\angle R$	1	Colour bar signal, Burst 150mVpp, Contrast : Colour : TYP	84	90	96	deg
PAL Demodulation Angle G	$\angle G$	1	Colour bar signal, Burst 150mVpp, Contrast : Colour : TYP	228	235	242	deg
PAL Demodulation Output Residual Carrier	e_{car}	1	No signal input. 4.43MHz component of each output pin			90	mVpp
Contrast Slope	Δe_{typ}	1	Colour bar signal, Burst 150mVpp, Contrast : 20→60, Colour : TYP	8	10.5	14	dB
NTSC Tint Center	T_C	1	Colour bar signal, Burst 150mVpp, Measure phase displacement at tint data 37	-7	0	+7	deg
NTSC Tint Variable Range	$\Delta\theta_T$	1	Colour bar signal, Burst 150mVpp, Measure phase displacement at tint data 37. Tint : MIN ~ MAX	70	90	120	deg
PAL Colour Variable	Δe_{O-COL}	1	Colour bar signal, Burst 150mVpp, Contrast : TYP, Colour : Variation at 10→7F	17	20	25	dB
PAL APC Pull-in Range	f_{PCP}	1	Burst frequency is variable.	±450	±500		Hz
NTSC APC Pull-in Range	f_{PCN}	1	Burst frequency is variable.	±450	±500		Hz
PAL VCO Free-run Frequency	f_{COP}	1	No signal, A_{CC} : OFF	-200	0	+200	Hz
NTSC VCO Free-run Frequency	f_{CON}	1	No signal, A_{CC} : OFF	-200	0	+200	Hz
PAL fCO Dependency with Supply Voltage	Δf_{COP-V}	1	V_{CC2}=5V±10% variable variation to V_{CC2}=5V	-120	0	+120	Hz
NTSC fCO Dependency with Supply Voltage	Δf_{CON-V}	1	V_{CC2}=5V±10% variable variation to V_{CC2}=5V	-120	0	+120	Hz
PAL VCO Output Level	e_{CW-P}	1	Pin 30 output level when V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V, I_{17}=15mA	0.3	0.4	0.5	Vpp
NTSC VCO Output Level	e_{CW-N}	1	Pin 30 output level when V_{CC1}=9V, V_{CC2}=5V, V_{CC3}=6.2V, I_{17}=15mA	0.3	0.4	0.5	Vpp
PAL Colour Killer Tolerance	e_{KP}	1	Colour bar signal, Burst 150mVpp=0dB, Colour : Contrast : MAX	-30	-36	-41	dB
NTSC Colour Killer Tolerance	e_{KN}	1	Colour bar signal, Burst 150mVpp=0dB, Colour : Contrast : MAX	-37	-42	-48	dB
Colour Killer Leak	e_{CK}	1	Input sine wave 150mVpp, f = 2MHz(4.43-2)MHz component, Colour : Contrast : MAX			30	mVpp
Colour Killer Detection Output Voltage (Colour)	V_{41-C}	1	Measure Pin 41. Burst signal exists.	4.5	5.0	5.5	V
Colour Killer Detection Output Voltage (Black and White)	$V_{41-B/W}$	1	No burst signal.		0.06	0.5	V
Chroma Input Pin Voltage	V_{47}	1	Pin 47 open voltage	1.7	2.0	2.3	V

■ Electrical Characteristics (Ta=25°C) (Continue)

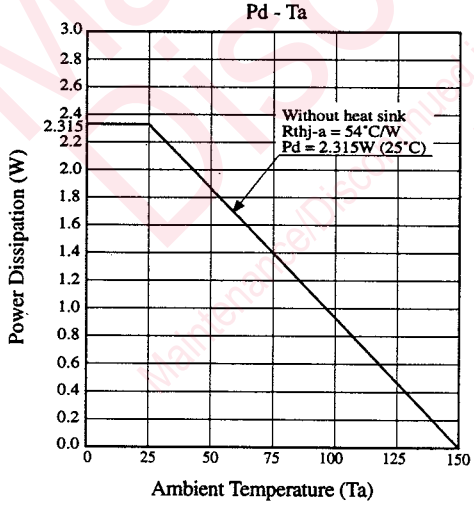
Item	Symbol	Test cct	Condition	min.	typ.	max.	Unit
PAL/SECAM Changeover Voltage	$V_{47\text{-}P/S}$	1	Pin 47 PAL/SECAM changeover threshold	2.35	2.5	2.65	V
Colour Difference Output (B-Y) when Lock Det. Pin is Low	e_{04}	1	Colour bar signal, Pin 12 = 0V, Burst 150mVpp, Colour : Contrast : MAX		200	600	mVpp
(4) RGB Output Circuit							
Drive Adjustment Range	A_{VD}	1	External input 0.2Vpp input, YS = 1V, Drive : MIN ~ MAX, R, B output	3	6	9	dB
Cutoff adjustment Range (1 step)	V_{CUT1}	1	No input. Pedestal level variation with cutoff : MIN ~ MAX when DAC SW is out of use	1.0	1.3	1.6	V
Cutoff adjustment Range (2 step)	V_{CUT2}	1	No input pedestal level variation with cutoff : MIN ~ MAX when DAC SW is in use	1.6	2.25	2.9	V
(5) Deflection Signal Processing							
Horizontal Free-run Oscillation Frequency	f_{HO}	1	No input, Pin 19 output frequency	15.45	15.75	16.05	kHz
Horizontal Free-run Oscillation Frequency Dependency with Supply Voltage	$\frac{\Delta f_{HO}}{V_{CC3}}$	1	$f_{HO}(I_{17}=30mA)$ $f_{HO}(I_{17}=15mA)$	-100	0	100	Hz
Horizontal Oscillation Starting Voltage	$V_{fH(S)}$	1	Horizontal oscillation output is 1Vpp or more and f=10k ~ 20kHz			5.2	V
Horizontal Oscillation Pulse Duty Ratio	τ_{HO}	1	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=5V I_{17}=15mA	35.0	38.0	41.0	%
Horizontal Pull-in Range	f_{PH}	1	f_{HO} = 15.75kHz	±400			Hz
H Pulse Output Voltage	V_{19}	1	V_{CC} : TYP	2.3	2.8	3.3	V
High-tension Detection Circuit Operating Voltage (Shutdown)	V_{sth}	1	I_{20} = 50µA	0.7	0.83	0.95	V
Shutdown Leakage Current	I_{sth}	1	Measure 120 when Pin 20 = 0V			5.0	µA
AFC1 Pin Operating Voltage	V_{13}	1	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=5V I_{17}=15mA	3.8	4.2	4.6	V
(6) Vertical Signal Processing							
PAL Vertical Free-run Oscillation Frequency	$f_{VO\text{-}P}$	1	$\left(\frac{2}{625} f_{H\text{-}P}\right)$	48.5	50	51.5	Hz
NTSC Vertical Free-run Oscillation Frequency	$f_{VO\text{-}N}$	1	$\left(\frac{2}{525} f_{H\text{-}N}\right)$	58.5	60	61.5	Hz
Vertical Free-run Oscillation Pulse Width	τ_{VO}	1	PAL : f_H = 15.625kHz NTSC : f_H = 15.75kHz	9.5	10.0	10.5	1/f_H
PAL Vertical Pull-in Enable Frequency	$f_{PV\text{-}P}$	1	$f_{V\text{-}P}$ = 50Hz	46	50	54	Hz
NTSC Vertical Pull-in Enable Frequency	$f_{PV\text{-}N}$	1	$f_{V\text{-}N}$ = 60Hz	56	60	64	Hz
Vout Output Voltage	V_9	1	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=5V I_{17}=15mA	0	0.2	0.5	Hz
V-Pulse Shaper Output Pulse Width	τ_{10}	1		1.4	2.2	3.0	msec
(7) Sand Castle Pulse							
PAL Burst Gate Pulse Width	$\tau_{BGP\text{-}P}$	1	Pin 18 PAL Burst gate pulse width	3.4	4.0	4.6	µsec
NTSC Burst Gate Pulse Width	$\tau_{BGP\text{-}N}$	1	Pin 18 NTSC Burst gate pulse width	2.5	3.0	3.5	µsec
PAL V-Blanking Width	$\tau_{VBLK}^{\text{-P}}$	1	Pin 18 PAL Blanking pulse width (22±1.5)H	1.31	1.41	1.51	msec
NTSC V-Blanking Width	$\tau_{VBLK}^{\text{-N}}$	1	Pin 18 NTSC Blanking pulse width (17.5±1.5)H	1.01	1.11	1.21	msec
Burst Gate Pulse Output Voltage	V_{BGP}	1	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=5V I_{17}=15mA	3.6	4.0	4.5	V
H-Blanking Pulse Output Voltage	V_{HBLK}	1	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=5V I_{17}=15mA	2.5	2.9	3.4	V
V-Blanking Pulse Output Voltage	V_{VBLK}	1	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=5V I_{17}=15mA	1.0	1.5	2.0	V

■ Electrical Characteristics (Ta=25°C) (Continue)

Item	Symbol	Test cct	Condition	min.	typ.	max.	Unit
(8) H Center Circuit							
H Center Variable Range (1)	$\tau_{DH(1)}$	1	H center : TYP→MIN, Hsync rise and HBLK delay	-2.2	-1.6	-1.3	µsec
H Center Variable Range (2)	$\tau_{DH(2)}$	1	H center : TYP→MAX, Hsync rise and HBLK delay	1.3	1.6	2.2	µsec
(9) Lock Detector Circuit							
Lock Detector Output Voltage (Hi)	$V_{12\text{-}HI}$	1	In Hor. Loop ON state, Pin 12 voltage at input of horizontal sync. signal.	7.9	8.5	9.0	V
Lock Detector Output Voltage (Lo)	$V_{12\text{-}LO}$	1	In Hor. Loop ON state, Pin 12 voltage at no input.		0.2	0.5	V
(10) Service Switch Circuit							
Service Switch Threshold	V_{sth}	1		0.35	0.65	1.10	V
Service SW Operation	e_{ser}	1	Input : stair step 0.4Vpp Measure amplitude at Pin 50 (ACL)=0V			150	mVpp
(11) Spot Killer							
Spot Killer Operation	K_{SP}	1	Measure each output pedestal level when the current of 1mA is applied to Pin 31.	6.8	7.5	8.2	V
(12) Other							
Video Circuit D Range	Y_D	1	0.6Vpp (0.429Vop) input, Brightness :7F, Contrast : 7F, Cutoff : 7F	3.8			Vop

■ Characteristics Curve Diagrams

NFS - 52D Package Power Dissipation
Pd - Ta



■ Supplementary Explanation

● Electrical Characteristics Design Reference Values (Ta=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
(1) Y-Signal Processing Circuit						
Y-Signal Input	e_Y	Input : Pin 52, Positive polarity		0.6Vpp ± 3dB		
Picture Quality Variable Range (2)	$\frac{A_{SMAX}}{A_{SMIN}}$	Input sine wave 0.2Vpp, f = 3.3MHz, Brightness : "B0", Sharpness = MAX/MIN	8	11	14	dB
Video Output (Eo) DC Dependency with Supply Voltage	$\frac{\Delta E_O}{\Delta V}$	Pedestal change rate of video output in V_{CC} changing ±5%.			400	mV/V
Eo Dependency with Ambient Temperature	$\frac{\Delta E_O}{\Delta T}$	V_{CC1}=9V, VCC2=5V, Change rate of pedestal level in Ta = -20~70°C		-1.8		mV/°C
Contrast Variation with Aperture Control Change	V_{CA}	Video input, Step wave 0.4Vpp, Contrast : TYP, Sharpness : MIN/MAX			150	mVpp
Black Level Variation Voltage with Contrast Change	V_{BAC}	Sharpness : MIN Contrast : MIN /MAX			200	mV
Black Level Variation Difference Voltage with Contrast Change	ΔV_{BAC}	Sharpness : MIN Contrast : MIN /MAX	-20	0	20	mV
Delay Line Dynamic Range	V_{DDR}			1.1		Vpp
Peak Clamp Input Pin Flow-in Current	I_{IN52}	Current flowing in when 5V is applied to Pin 52.		55		µA
Video Signal Output Dependency with Supply Voltage	$\frac{\Delta e_O}{\Delta V}$	Input signal 0.4Vpp, Stair step, Change rate of output amplitude at V_{CC} =±5%	0.15	0.2	0.25	Vpp/V
eo Dependency with Ambient Temperature	$\frac{\Delta e_O}{\Delta T}$	V_{CC1}=9V, V_{CC2}=5V, Change rate of output amplitude in Ta = -20~70°C		11		%
C-Y/Y Ratio	C-Y/Y	Colour bar input, Colour : MAX Contrast : TYP	1.0	1.15	1.5	Times
Delay Line Group Delay	D_{FL}	Flat		3		MHz
Video Signal Output	E_{OD}	Input 0.4Vpp, Stair step, Contrast : MAX		4		Vpp
Video Output DC DifferenceVoltage Dependency with Supply Voltage	$\frac{\Delta E_O}{\Delta V}$	V_{CC1}=9V ± 10% V_{CC2}=5V	250	0	250	mV/V
Differential Gain	DG	APL 10~90%			5.0	%
Temperature Variation to each Output	$\frac{\Delta E_{RGB}}{\Delta T}$	Relative variation for each RGB output			±35	mV
Y Noise Level	Y_{NL}	No input, 1~4MHz component			50	mV
Y S/N	$Y_{S/N}$	Input 600mV, Sharpness : MIN, Set output at 3.3V, then measure with a noise meter.		53		dB
(2) ON Screen Circuit						
Changeover Speed	T_{SW}		7			MHz
Ext. RGB Input Dynamic Range	V_{DREXT}			2.4		Vpp
(3) Colour Signal Processing Circuit						
PAL/NTSC Ratio	P/N	Measure demodulation output ratio at PAL/NTSC.	0.7	1.0	1.3	Times
Max. Colour Difference Output	e_{OM}	Colour bar signal, Burst 150mVpp, Contrast: Colour : MAX	3.8	4.7	5.4	V_{OP}
Colour Difference Output Dependency with Supply Voltage	Δe_{O-VCC}	V_{CC2}=5V ±10% Variation width to V_{CC1}=9V			1.3	Vpp/V
Colour Difference Output Dependency with Ambient Temperature	Δe_{O-T}	Ta = -20~70°C Center : Ta = 25°C		18		%
Demodulation Output 1H Changeover DC Step Voltage	ΔE_{PAL}			0	40	mV
f_O Dependency with Ambient Temperature PAL	Δf_{COP-T}	Ta = -20~70°C Colour signal no input		-2		Hz/°C
VCO Control Sensitivity PAL	β_P			3.3		Hz/mV
APC Phase Detection Sensitivity PAL	μ_P	Killer : OFF		30		$\frac{mV}{deg}$
Phase Hold Characteristic PAL	$\Delta\phi_P$	$\frac{1}{\mu \times \beta}$ x 100		1.33		$\frac{deg}{100Hz}$

Note) The above characteristic is a design reference value, not a guarantee value.

■ Supplementary Explanation

● Electrical Characteristics Design Reference Values (Ta=25°C) (Continue)

Item	Symbol	Condition	min.	typ.	max.	Unit
f_O Dependency with Ambient Temperature NTSC	Δf_{CON-T}	Ta = -20~70°C Colour signal no input		-2		Hz/°C
VCO Control Sensitivity NTSC	β_N	Burst Gate : OFF		2.3		Hz/mV
APC Phase Detection Sensitivity NTSC	μ_N	Killer : OFF		30		$\frac{mV}{deg}$
Phase Hold Charactersitic NTSC	$\Delta\phi_N$	$\frac{1}{\mu \cdot \beta}$ x 100		1.45		$\frac{deg}{100Hz}$
Carrier Filter Frequency Characteristic	e_{ef}	Frequency at which output pin showns -3dB.		1.1		MHz
E_C Variation with Colour	$\Delta E_{R(C)}$ $\Delta E_{G(C)}$ $\Delta E_{B(C)}$	Colour : MIN→MAX Contrast : MAX, A_{CC}=5V			50	mV
E_C Variation with ACC	$\Delta E_{R(A)}$ $\Delta E_{G(A)}$ $\Delta E_{B(A)}$	E_C variation with A_{CC} voltage change Colour : Contrast : MAX			20	mV/V
Colour/Black & White DC Difference Voltage	$\Delta E_{C/BW}$	Measure pedestal variation when killer pin=H/L.		0	60	mV
Line Crawling	Δe_{OPAL}				50	mV
Demodulation Output Frequency Characteristic	f_{C-Y}			1.1		MHz
Colour Difference Output Contrast Ratio	Δe_{OC}	Coloiur bar signal, Burst 150mVpp, Contrast : MIN→MAX, Colour : TYP	20	26	33	dB
NTSC Tint Control Sensitivity	θ_T	Colour bar signal, Burst 150mVpp, Phase variation at tint : 20→60	30	40	50	deg
(3) Deflection Processing Circuit						
Sync. Separable Input	V_{in}	APL : 50%	1.0	2.0	2.8	Vpp
f_{HO} Dependency with Ambient Temperature	$\frac{\Delta f_{HO}}{Ta}$	Ta = -20~70°C		5.5		Hz/°C
Phase Detection Sensitivity	μ	V_{CC1}=9V, V_{CC2}=5V		31		μA/μs
Horizontal Oscillation Frequency Control Sensitivity	β			-1.6		Hz/mV
Vertical Free-run Oscillation Frequency Dependency with Supply Voltage	Δf_{VO}	V_{CC1}=9V V_{CC3}=6.2V V_{CC2}=4.5~5.5V I_{17}=15mA	-0.8	0	0.8	Hz
FBP Slice Level (Blanking)	V_{FBP-1}	FBP input level at which blanking works on RGB outputs	0.3	0.75	1.1	V
(5) RGB Back						
RGB Back Output Level	E_{RGB-B}	No input DC variation in RGB Back operating.	2.3	2.75	3.2	V
(6) Sand Castle Pulse						
Burst Gate Pulse Position	P_{BGP}	From back edge of horizontal sync. signal to front edge of burst gate pulse.		0.1		μs
(7) H-Center Circuit						
FBP Delay Time Allowable Range	T_{H-FBP}	Range within which center position of screen changes by ±1.3μs or more when delay time is changed from Hout rise to FBP center.	12		19	μs
FBP Slice Level (AFC2)	V_{FBP-2}	FBP input level at which AFC2 operates	1.5	2.0	3.0	V
(8) I^2C • DAC						
4 Bit DAC DNLE	L_1	1 LSB = {DATA(MAX)-DATA(MIN)}/15	0.5	1	1.5	$\frac{LSB}{STEP}$
7 Bit DAC DNLE	L_2	1 LSB = {DATA(MAX)-DATA(MIN)}/127	0.1	1	1.9	$\frac{LSB}{STEP}$
8 Bit DAC DNLE (Except 40.80.CO)	L_{3-1}	1 LSB = {DATA(MAX)-DATA(MIN)}/255	0.1	1	1.9	$\frac{LSB}{STEP}$
8 Bit DAC DNLE (Only for 40.80.CO)	L_{3-2}	1 LSB = {DATA(MAX)-DATA(MIN)}/255	-2	1	4	$\frac{LSB}{STEP}$

Note) The above characteristic is a design reference value, not a guarantee value.

■ Supplementary Explanation

● Electrical Characteristics Design Reference Values (Ta=25°C) (Continue)

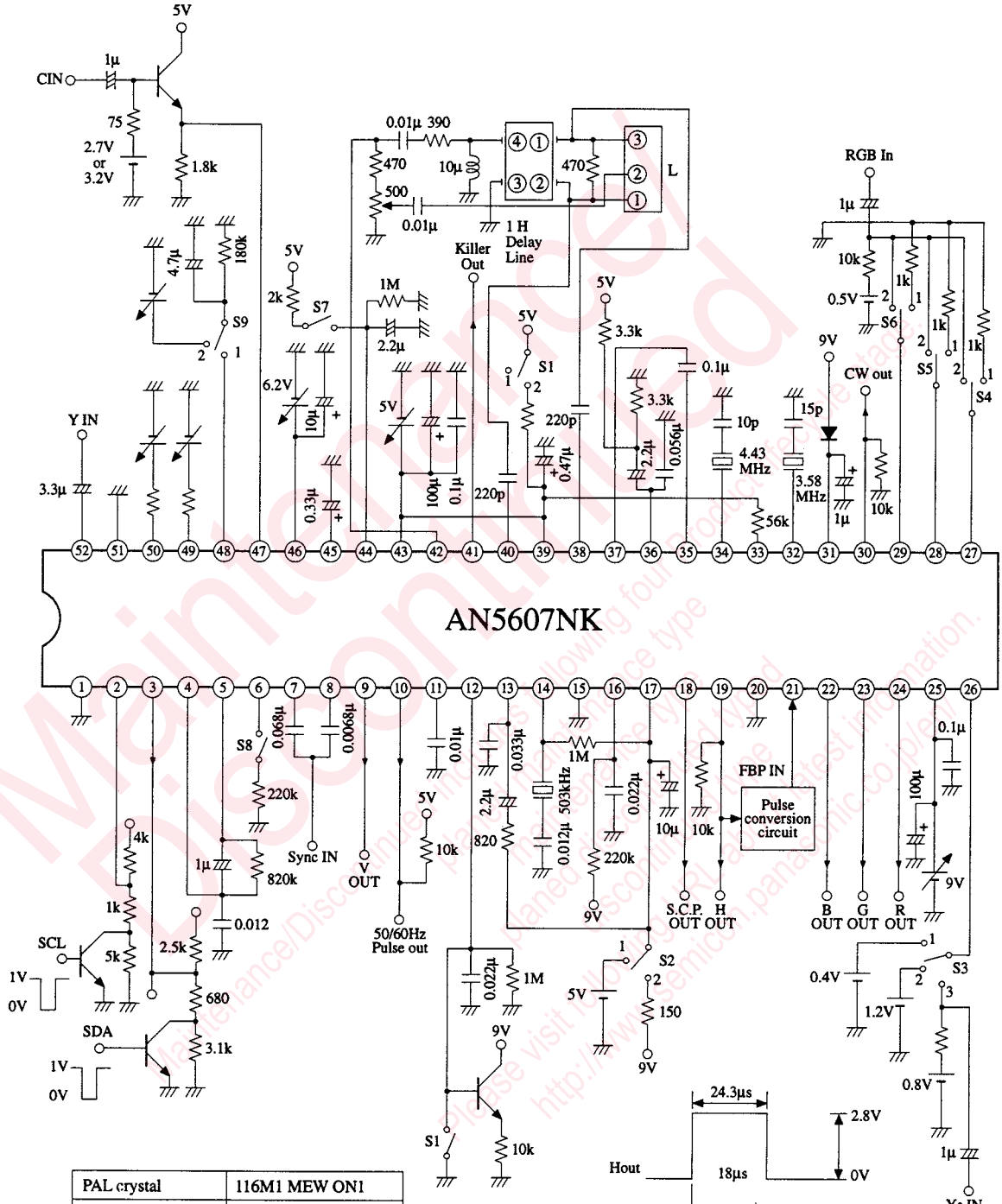
Item	Symbol	Condition	min.	typ.	max.	Unit
t_{BUF}			4.0			µs
$t_{SU \cdot STA}$			4.0			µs
$t_{HD \cdot STA}$			4.0			µs
t_{HI}			4.0			µs
t_{LO}			4.0			µs
t_R					1.0	µs
t_F					0.35	µs
$t_{SU \cdot DAT}$			0.25			µs
$t_{HD \cdot DAT}$			0			µs
$t_{SU \cdot STO}$			4.0			µs

Note) The above characteristic is a design reference value, not a guarantee value.

■ Pin Descriptions

Pin No.	Pin Name	Pin No.	Pin Name
1	GND (I^2C)	27	B Input
2	SCL Input	28	G Input
3	SDA Input	29	R Input
4	Vertical Integration Filter	30	CW Output
5	Vertical Sync. Separation Input	31	Spot Killer Input
6	Black Level Correction Starting Point Adjustment	32	3.58MHz Oscillation
7	Vertical Sync. Input	33	Killer Bypass
8	Horizontal Sync. Input	34	4.43MHz Oscillation
9	Vertical Output	35	ACC Filter 1
10	50/60Hz Pulse Output	36	APC Filter
11	50/60Hz Shaper	37	ACC Filter 2
12	Horizontal Sync. Detection Filter	38	R-Y Input
13	Horizontal AFC 1 Filter	39	Killer Filter
14	503kHz (32fH) Oscillation	40	B-Y Input
15	GND (Vertical)	41	Killer Output
16	Horizontal AFC 2 Filter	42	Chroma Signal Output
17	Supply Voltage 4 (Horizontal)	43	Supply Voltage 2 (Chroma)
18	Sand Castle Pulse Output	44	ACC Detection Filter
19	Horizontal Drive Pulse Output	45	Y Clamp Capacitor
20	High tension Detection (Shutdown) Input	46	Supply Voltage 3 (Video)
21	Flyback Pulse Input	47	Chroma Signal Input
22	B Output	48	Black Level Detection Filter, Fuzzy Input
23	G Output	49	Automatic Brightness Limiter, ABL
24	R Output	50	Automatic Contrast Limiter, ACL
25	Supply Voltage 1 (Video/RGB Output)	51	GND (Video/Chroma)
26	Ys Input	52	Video Signal Input

Test Circuit 1



PAL crystal	116M1 MEW ON1
NTSC crystal	3579 MEIDEN11
1 H Delay line	EFDEN645 A11G1212
Coil	EIK7E80045
Horizontal Vibrator	CSB500F48

● I²C Bus protocol (1)

I²C-BUS Formats

(1) Slave address : 1 0 0 0 1 0 1 (0)

(2) Slave address format :

S	SLAVE ADDR	0	A	SUB ADDR	A	DATA BYTE	A	P

↑ Start condition ↑ Write ↑ Acknowledge bit ↑ Stop condition

(3) Subaddress byte and data byte format :

Sub-addr (H)	Functions	Data Byte								Initial Setting at Power ON
		D7	D6	D5	D4	D3	D2	D1	D0	
00	Colour	0	A06	A05	A04	A03	A02	A01	A00	41 (TYP)
01	Tint	0	A16	A15	A14	A13	A12	A11	A10	41 (TYP)
02	Brightness	A27	A26	A25	A24	A23	A22	A21	A20	81 (TYP)
03	Contrast	0	A36	A35	A34	A33	A32	A31	A30	41 (TYP)
04	Sharpness	0	A46	A45	A44	A43	A42	A41	A40	41 (TYP)
05	Cutoff R	A57	A56	A55	A54	A53	A52	A51	A50	81 (TYP)
06	Cutoff G	A67	A66	A65	A64	A63	A62	A61	A60	81 (TYP)
07	Cutoff B	A77	A76	A75	A74	A73	A72	A71	A70	81 (TYP)
08	Drive R	A87	A86	A85	A84	A83	A82	A81	A80	81 (TYP)
09	Drive B	A97	A96	A95	A94	A93	A92	A91	A90	81 (TYP)
0A	H Center	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0	08 (TYP)
0B	MODE SW (PAL/NTSC)								PNS	Refer to I²C Bus protocol (2)
0B	50/60Hz SW							VFS		Refer to I²C Bus protocol (2)
0B	RGB Back MODE						RGB			Refer to I²C Bus protocol (2)
0B	RGB Back				R	G	B			Refer to I²C Bus protocol (2)
0B	Blanking SW			BLK						Refer to I²C Bus protocol (2)
0B	VCO SW	VCO								Refer to I²C Bus protocol (2)

* AA4, AA5, AA6 : Cutoff SW → Pedestal DC up at HI (Approx. 0.95V) (R.G.B)

AA7 : Fuzzy SW → Fuzzy ON at HI

● I²C Bus protocol (2)

Data byte Condition at Sub-address ($0B_H$)

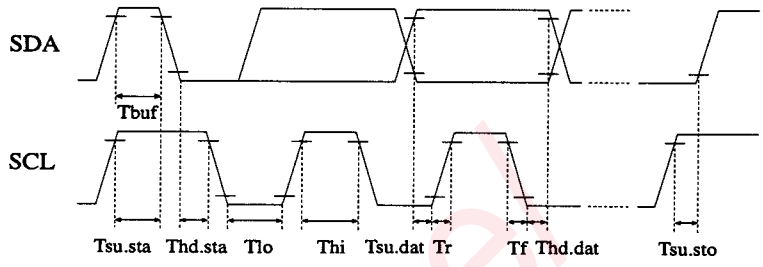
Functions	Data (* mark shows SW ON)		Condition
Mode SW	PNS	*1	PAL
		0	NTSC
50/60Hz	VFS	*0	50Hz
		1	60Hz
RGB Back MODE	RGB	1	Without Vsync. Lock
		*0	With Vsync. Lock
RGB Back	B	1	ON
		*0	OFF
	G	1	ON
		*0	OFF
	R	1	ON
		*0	OFF
Blanking SW	BLK	1	Without Blanking
		*0	With Blanking
VCO SW	VCO	1	3.58MHz
		*0	4.43MHz

* Auto-increment function

Start condition | Slave address | Sub-address | Data 1 | Data 2 | Data 3 | Stop condition

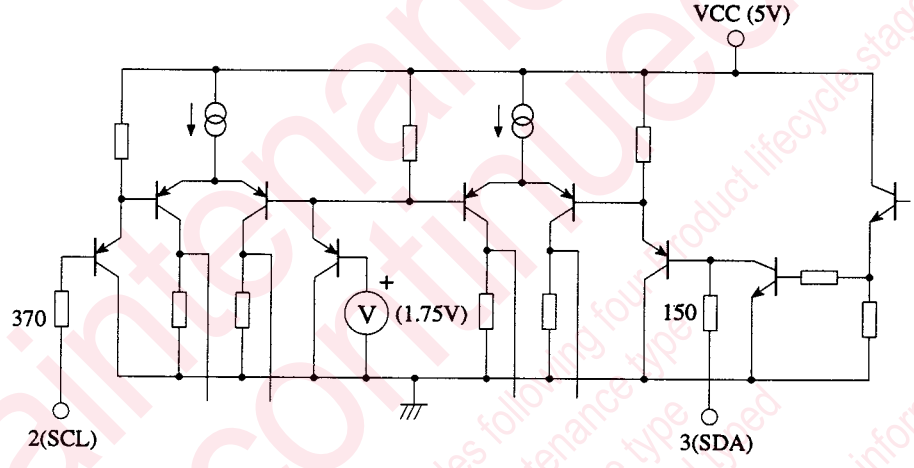
Once the Data input as above, the specified sub-address DAC goes to Data1, the stepped-up sub-address DAC to Data 2 and further stepped-up sub-address DAC to Data 3, which indicates that more than two DACs can be controlled at one time.

● I²C Bus Input Signal Timing



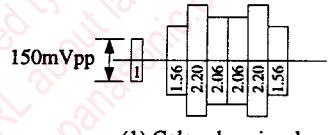
* Refer to Page 313

● I²C Bus Input Circuit Construction

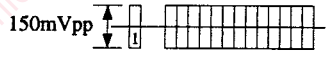


● Colour Difference Output Amplitude Conversion Formula (Input : colour bar→offset colour bar)

The colour bar signal (1) is used as a standard signal for the chrominance signal processing circuit of this IC. When colour difference output amplitude by the offset colour bar signal (2) is needed, the amplitude value is given by the conversion formula below.



(1) Colour bar signal



(2) Offset colour bar signal

(1) B-Y axis

- Colour difference output by colour bar signal
  $e_{B\text{-}Y} = |Y'| + |B'|$
- Colour difference output by offset colour bar signal
  $(|Y'| + |B'|)/\cos\theta$

Here the ratio of the offset colour bar signal level to the colour bar signal level is corrected.

$$e_{B\text{-}Y} = \frac{\alpha}{C_B} (|Y'| + |B'|)/\cos\theta_B$$

(θ_B:13°, α:offset colour bar signal level C_B:colour bar signal level)

(2) R-Y axis

- In the same way as (1)

$$e_{R\text{-}Y} = \frac{\alpha}{C_R} (|R'| + |S'|)/\cos\theta_R$$

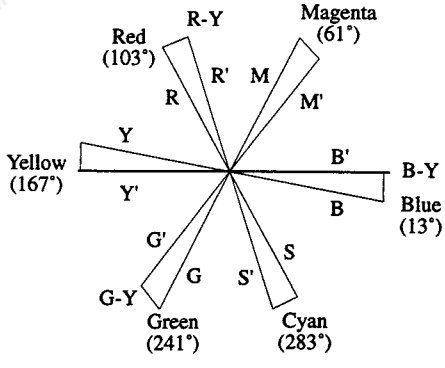
(θ_R:103°- $\angle$R-Y)

(3) G-Y axis

- In the same way as (1)

$$e_{G\text{-}Y} = \frac{\alpha}{C_G} (|G'| + |S'|)/\cos\theta_G$$

(θ_G:241°- $\angle$G-Y)



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