DATA SHEET

TDA9160
PAL/NTSC/SECAM decoder/sync processor

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

PAL/NTSC/SECAM decoder/sync processor TDA9160

FEATURES

- Multistandard PAL, NTSC and SECAM
- I²C-bus controlled
- I²C-bus addresses can be selected by hardware
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- Horizontal and vertical drive output
- East-West correction drive output
- Two CVBS inputs
- S-VHS input
- Vertical divider system
- H_A synchronization pulse
- Two level sandcastle pulse

GENERAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/processor. The device contains horizontal and vertical drive outputs and an east-west correction drive circuit. The TDA9160 has been designed for use with baseband chrominance delay lines and DC-coupled vertical and east-west output circuits.
The device has three inputs, two for CVBS and one for S-VHS. The main signal is available at the luminance and colour difference outputs and, also, at the TXT output (unprocessed). The signal at the PIP output can be selected independently from the main signal.
The circuit provides a drive pulse for the horizontal output stage, a differential sawtooth current for the vertical output stage and an east-west drive current for the EW output stage. These signals can be used to provide geometry correction of the picture. A two level sandcastle pulse and an H_A pulse are made available for synchronization purposes
.The I²C-bus address of the TDA9160 can be programmed by hardware.

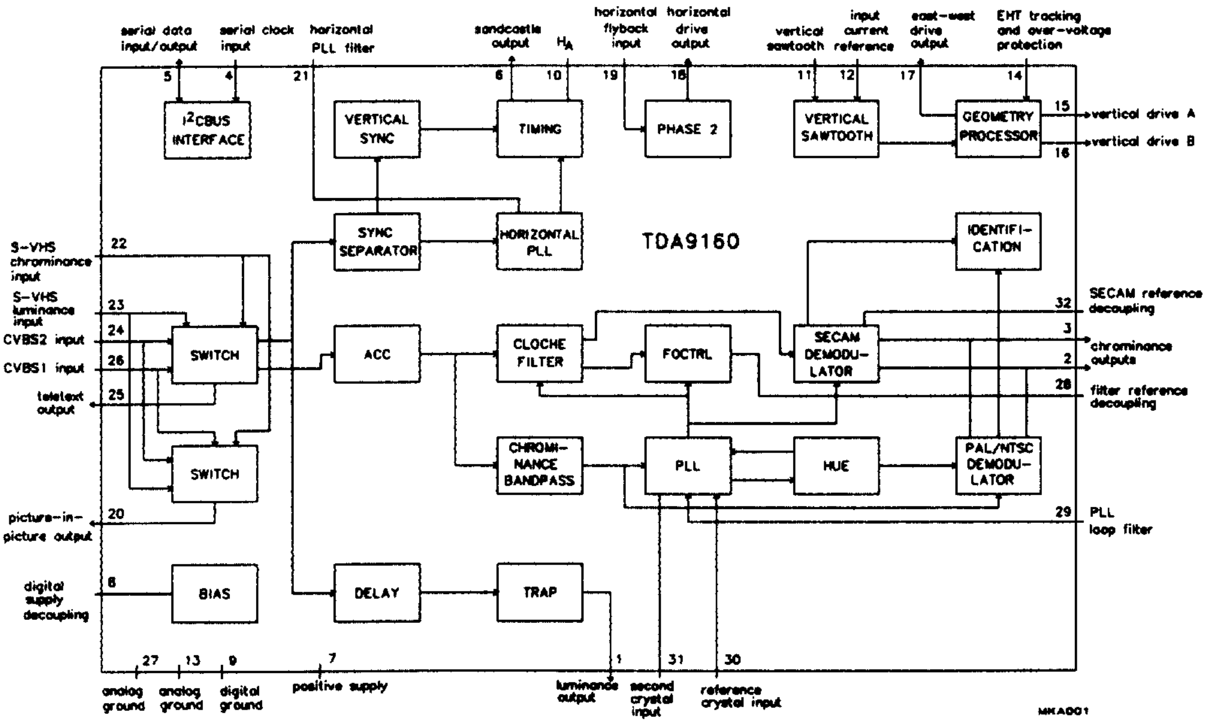


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
$V_{24,26(p-p)}$	CVBS input voltage (peak-to-peak value)		–	1.0	–	V
$V_{23(p-p)}$	S-VHS luminance input voltage (peak-to-peak value)		–	1.0	–	V
$V_{22(p-p)}$	S-VHS chrominance burst input voltage (peak-to-peak value)		–	0.3	–	V
$V_{1(p-p)}$	luminance output voltage (peak-to-peak value)		–	0.45	–	V
$V_{25(p-p)}$	teletext output voltage (peak-to-peak value)		–	1.0	–	V
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	PAL/NTSC	–	525	–	mV
$V_{2(p-p)}$	chrominance output voltage –(R-Y) (peak-to-peak value)	SECAM	–	1.05	–	V
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	PAL/NTSC	–	665	–	mV
$V_{3(p-p)}$	chrominance output voltage –(B-Y) (peak-to-peak value)	SECAM	–	1.33	–	V
V_{10}	H_A output voltage		–	5.0	–	V
$I_{15,16(p-p)}$	vertical drive output current (peak-to-peak value)		–	1	–	mA
I_{18}	horizontal drive output current		–	–	10	mA
I_{17}	EW drive output current		–	–	0.9	mA
V_6	sandcastle clamping voltage level		–	4.5	–	V
V_6	sandcastle blanking voltage level		–	2.5	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9160	32	SDIL	plastic	SOT232(1)

Note

1. SOT232-1; 1996 December 2.

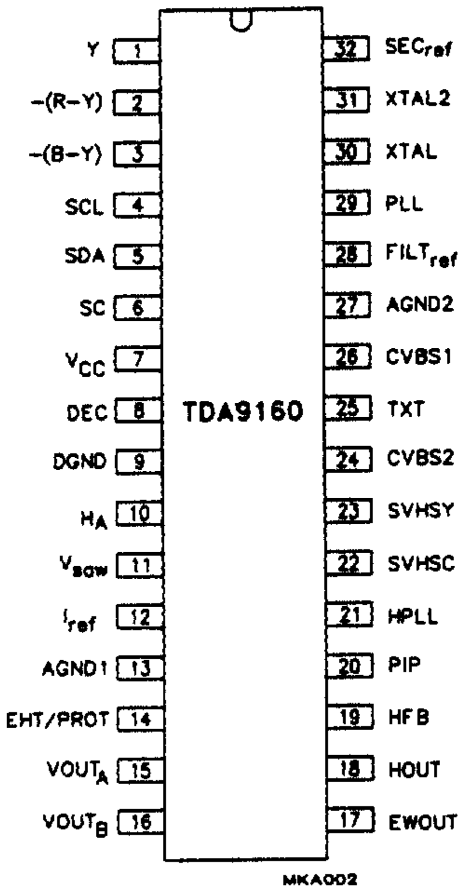


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
Y	1	luminance output
–(R-Y)	2	chrominance output
–(B-Y)	3	chrominance output
SCL	4	serial clock input
SDA	5	serial data input/output
SC	6	sandcastle output
V_{CC}	7	positive supply input
DEC	8	positive supply decoupling
DGND	9	digital ground
H_A	10	horizontal acquisition synchronization pulse
V_{saw}	11	vertical sawtooth
I_{ref}	12	input current reference
AGND1	13	analog ground
EHT/PROT	14	EHT tracking and over-voltage protection
$VOUT_A$	15	vertical drive output A
$VOUT_B$	16	vertical drive output B
EWOUT	17	east-west drive output
HOUT	18	horizontal drive output
HFB	19	horizontal flyback input
PIP	20	picture-in-picture output
HPLL	21	horizontal PLL filter
SVHSC	22	S-VHS chrominance input
SVHSY	23	S-VHS luminance input
CVBS2	24	CVBS2 input
TXT	25	teletext output
CVBS1	26	CVBS1 input
AGND2	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
PLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

FUNCTIONAL DESCRIPTION

The TDA9160 is an I²C-bus controlled, alignment free PAL/NTSC/SECAM colour decoder/sync processor/deflection controller which has been designed for use with baseband chrominance delay lines.
In the standard operating mode the I²C-bus address is 8A . If the TXT output is connected to the positive rail the address will change to 8E

The standards which the TDA9160 can decode are dependent on the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded. Which 3.6 MHz standards can be decoded is dependent on the exact frequencies of the crystal. In an application where not all standards are required only one crystal is sufficient (in this instance the crystal must be connected to the reference crystal input (pin 30)). If a 4.4 MHz crystal is used it must always be connected to pin 30. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator.
To enable the calibrating circuits to be adjusted exactly two bits from the I²C-bus address are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components; the search loop is illustrated in Fig.3.

The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information, concerning which standard and which crystal have been selected and whether the colour killer is ON or OFF is provided by the read out. Using the forced-mode does not affect the search loop, it does, however, prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. forced mode). To reduce the risk of wrong identification PAL has priority over SECAM (only line identification is used for SECAM).

The TDA9160 has two CVBS inputs and one S-VHS input which can be selected via the I²C-bus. The input selector can also be switched to enable CVBS2 to be processed, providing that there is no S-VHS signal present at the input. If the input selector is set to CVBS2 it will switch to S-VHS if an S-VHS sync pulse is detected at the luminance input. The S-VHS detector output can be read via the I²C-bus.
If the voltage at either the S-VHS luminance or the chrominance input (pins 22 and 23) exceeds +5.5 V the IC will revert to test mode.

The TDA9160 also provides outputs for picture-in-picture and teletext (PIP pin 20 and TXT pin 25). The decoder input signal can be switched directly to the TXT output. The PIP output signal can be selected independently from the TXT output. If S-VHS is selected at the TXT output only the luminance signal will be present; if S-VHS is selected at the PIP output then the luminance and chrominance signals will be added.

All filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.28 MHz or 3.58 MHz irrespective of the frequency of the active crystal. The switching is controlled by the identification circuit.

The S-VHS luminance signal does not pass through the notch filter to preserve bandwidth. The luminance delay line delivers the Y signal to the output 40 ns after the –(R-Y) and –(B-Y) signals. This compensates for the delay of the external chrominance delay lines.

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected it will always connect to the crystal at the reference input (pin 30).

The Hue signal, which is adjustable via the I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating PLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical flyback period, when the reference crystal is active. When the second crystal is active the VCO is not calibrated. During this time the frequency of the VCO is kept constant by applying a constant voltage to its control input. If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals.

The main part of the sync circuit is a $432 \times f_H$ (6.75 MHz) oscillator the frequency of which is divided by 432 to lock the phase 1 loop to the incoming signal. The time constant of the loop can be forced by the I^2C-bus (fast or slow). If required the IC can select the time constant, depending on the noise content of the input signal and whether the loop is phase locked or not (medium or slow). The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal.

When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency greater than 6.75 MHz to protect the horizontal output transistor. The oscillator frequency is reset to 6.75 MHz when the crystal indication bits have been loaded into the IC. To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits, when subaddress 01 is received the line oscillator calibration will be initiated. The calibration is terminated when the oscillator frequency reaches 6.75 MHz. The oscillator is again calibrated when an out-of-lock condition with the input signal is realised by the coincidence detector. Again the calibration will be terminated when the oscillator frequency reaches 6.75 MHz.
The phase 1 loop can be opened using the I^2C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal the phase 1 loop can be opened to provide a stable line frequency and thus a stable picture.

The sync part provides an H_A pulse that is coupled to the processed CVBS signal.

The horizontal drive signal can be switched off via the I^2C-bus (standby mode). The horizontal drive is also switched off when the over-voltage protection circuit trips or when a POR is detected. Should either of these two conditions occur the IC will return to the normal operating mode when the appropriate command is received via the I^2C-bus. The duty cycle of the horizontal drive signal is increased from 2%, at start-up, to a constant value of 55% in approximately 300 lines. The two-level sandcastle pulse provides a combined horizontal and vertical blanking signal and a clamping pulse coupled to the display section of the TV.

The vertical sawtooth generator drives the geometry processing circuits which provide control for the horizontal shift, EW width, EW parabola/width ratio, EW corner/parabola ratio, trapezium correction, vertical slope, vertical shift, vertical amplitude and the S-correction. All of these control functions can be set via the I^2C-bus. The geometry processor has a differential current output for the vertical drive signal and a single-ended output for the EW drive. Both the vertical drive and the EW drive outputs can be modulated for EHT compensation. The EHT compensation pin (pin 14) can also be used for over-voltage protection. De-interlace of the vertical output can be set via the I^2C-bus.

The vertical divider system has a fully integrated vertical sync separator. The divider can accommodate both 50 and 60 Hz systems; it can either locate the field frequency automatically or it can be forced to the desired system via the I^2C-bus. A block diagram of the vertical divider system is illustrated in Fig.4. The divider system operates at 432 times the horizontal line frequency. The line counter receives enable pulses at twice the line frequency, thereby counting two lines per pulse.
A state diagram of the controller is illustrated in Fig.5. Because it is symmetrical only the right hand part will be described.

Depending on the previously found field frequency, the controller will be in one of the 'count' states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal) the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR-NORM or NO-NORM depending on the position of the vertical sync pulse in the previous fields. When the counter is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at $LC = 626$, moves to the WAIT state. In this condition it waits for the next pulse of the double line frequency signal and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal.
When the controller is in the NEAR-NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR-NORM window (i.e. $622 < LC < 628$). If no vertical sync pulse is detected, the controller will move back to the COUNT state when the line counter reaches $LC = 628$. The line counter will then be reset.
When the controller is in the NO-NORM state it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a sync pulse is not detected before $LC = 722$ (if the phase loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the phase loop is not locked the controller will move back to the COUNT state when $LC = 628$. The forced mode option keeps the controller in either the left-hand side (60 Hz) or the

right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the 'norm' counter which is an up/down counter that counts up if it finds a vertical sync pulse within the selected window. In the NEAR-NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR-NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field. If no vertical sync pulse is found in the selected window this will always result in a down pulse for the 'norm' counter.

Figure 7 illustrates the timing of the display sandcastle (DSC) and the reset pulse of the vertical sawtooth with respect to the input signal

I²C-bus protocol

If the TXT output is connected to the positive supply the address will change from 8A to 8E.

Valid subaddresses = 00 to 0F
Auto-increment mode available for subaddresses.

Subaddress 00 must always be sent before subaddress 01 in order to protect the horizontal output transistor.

Table 1 Slave address (8A)

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	X	1	X

Table 2 Inputs

SUBADDRESS	**MSB**							**LSB**
00	INA	INB	INC	IND	FOA	FOB	XA	XB
01	FORF	FORS	DL	STB	POC	FM	SAF	FRQF
02	–	–	HU5	HU4	HU3	HU2	HU1	HU0
03	–	–	HS5	HS4	HS3	HS2	HS1	HS0
04	–	–	EW5	EW4	EW3	EW2	EW1	EW0
05	–	–	PW5	PW4	PW3	PW2	PW1	PW0
06	–	–	CP5	CP4	CP3	CP2	CP1	CP0
07	–	–	TC5	TC4	TC3	TC2	TC1	TC0
08	–	–	VS5	CS4	VS3	VS2	VS1	VS0
09	–	–	VA5	VA4	VA3	VA2	VA1	VA0
0A	–	–	SC5	SC4	SC3	SC2	SC1	SC0
0B	SBL	–	VSH5	VSH4	VSH3	VSH2	VSH1	VSH0

Table 3 Outputs

ADDRESS	POR	FSI	STS	SL	PROT	SAK	SBK	FRQ

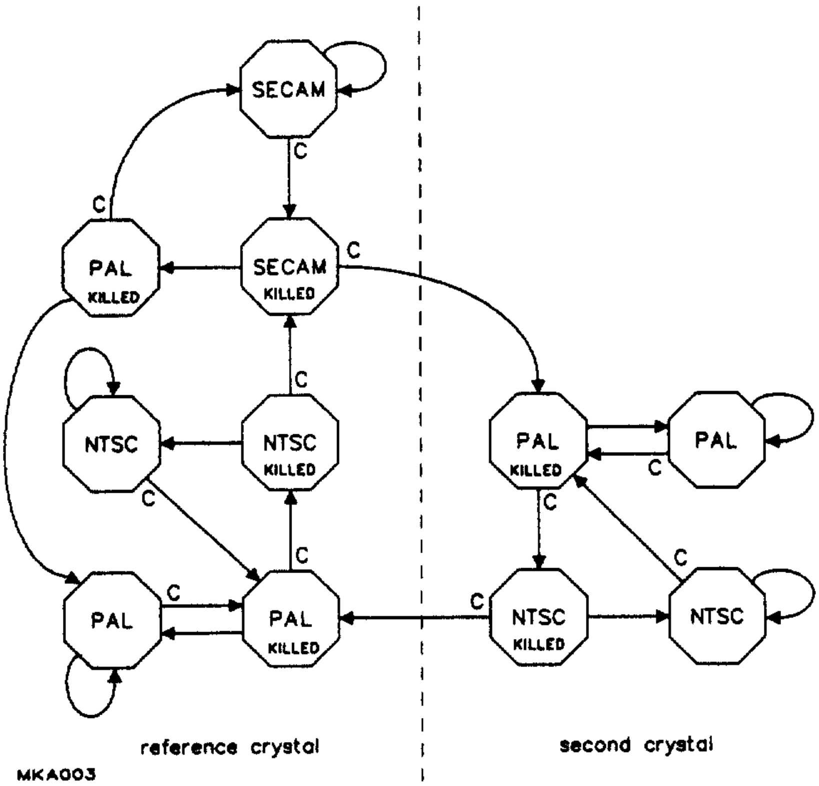


Fig.3 Search loop of the identification circuit.

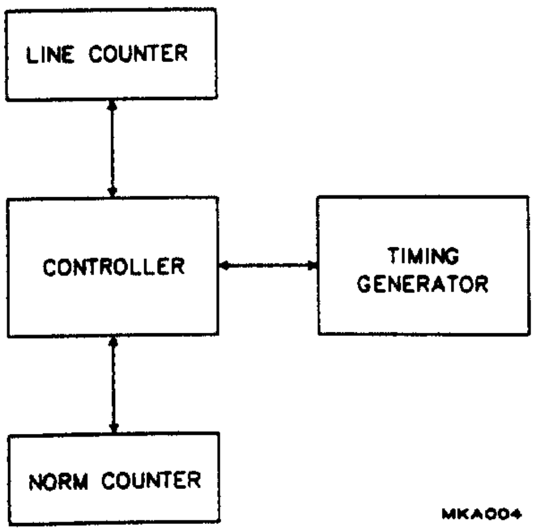


Fig.4 Block diagram of the vertical divider system.

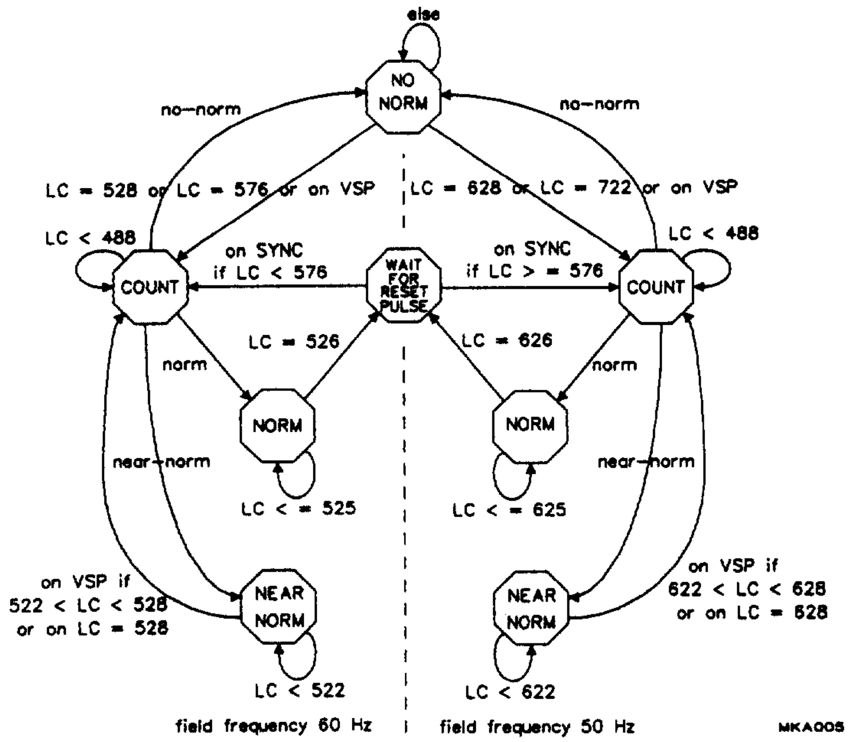


Fig.5 State diagram of the vertical divider system.

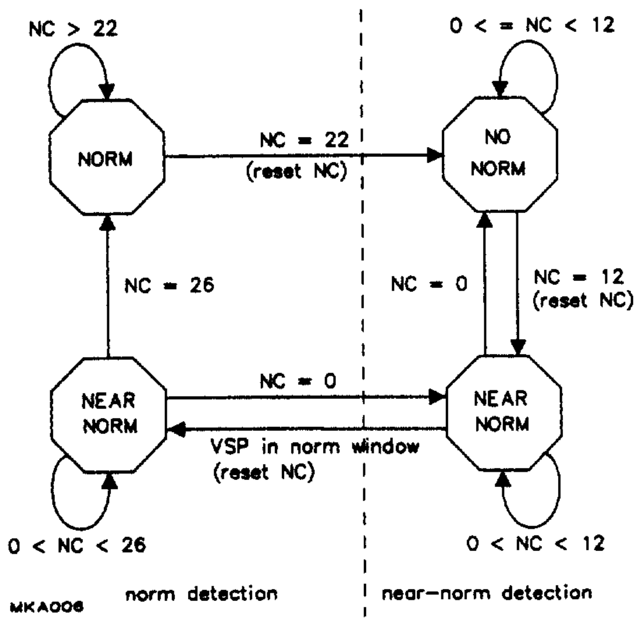


Fig.6 State diagram of the 'norm' counter.

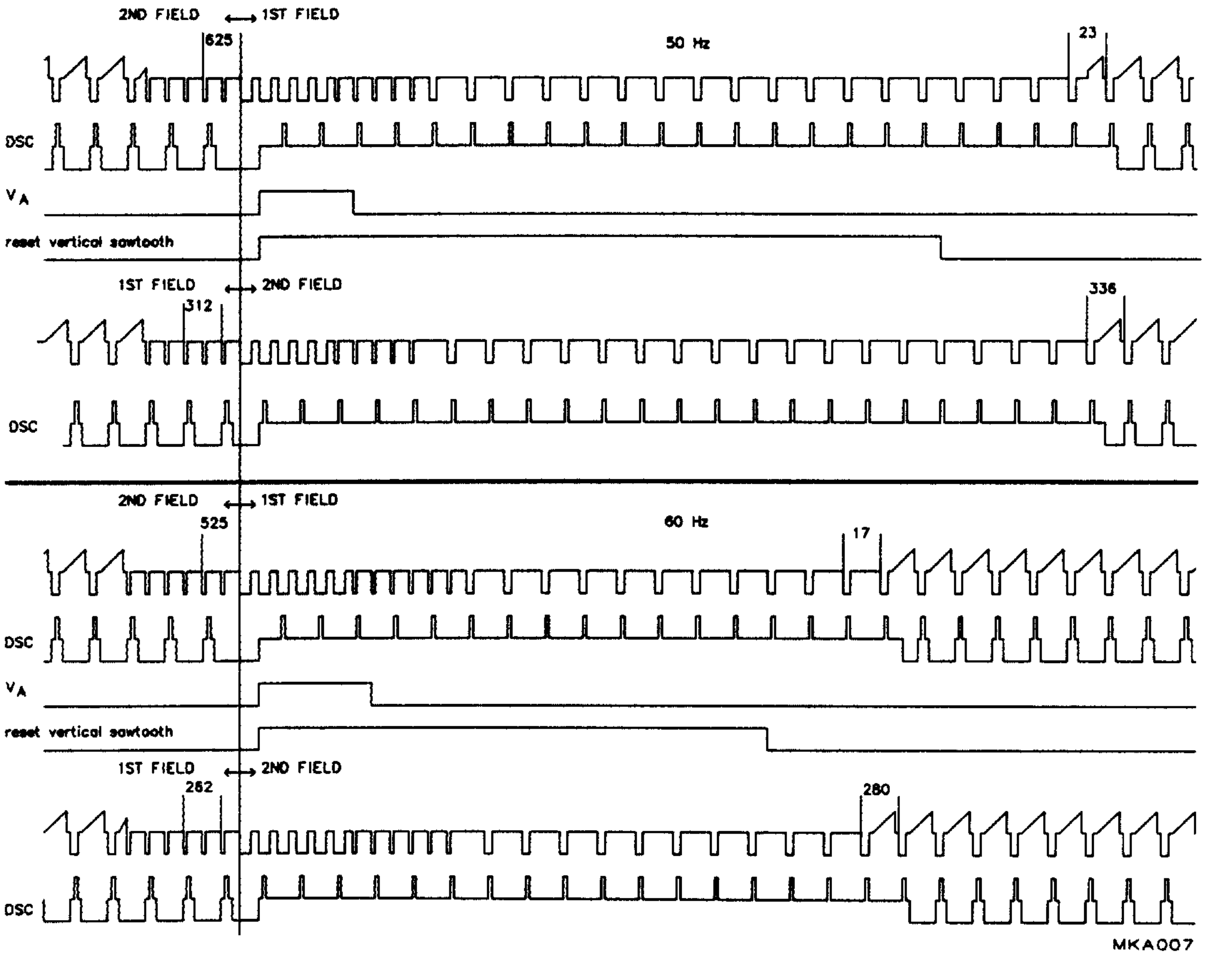


Fig.7 Field timing diagram.

INPUT SIGNALS

Table 4 Source select 1

INA	INB	DECODER AND TXT
0	0	CVBS1
0	1	CVBS2
1	0	S-VHS
1	1	S-VHS (CVBS2)

Table 5 Source select 2

INC	IND	DECODER AND TXT
0	0	CVBS1
0	1	CVBS2
1	0	S-VHS
1	1	S-VHS (CVBS2)

Table 6 Phase time constant

FOA	FOB	MODE
0	0	auto
0	1	slow
1	–	fast

Table 7 XTAL indication

XA	XB	CRYSTAL
0	0	2 x 3.6 MHz
0	1	1 x 3.6 MHz
1	0	1 x 4.4 MHz
1	1	3.6 and 4.4 MHz

Table 8 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto
0	1	60 Hz
1	0	50 Hz
1	1	auto

Table 9 Interlace

DL	CONDITION
0	interlace
1	de-interlace

Table 10 Standby

STB	CONDITION
0	standby
1	normal mode

Table 11 Phase loop control

POC	CONDITION
0	phi one loop closed
1	phi one loop open

Table 12 Forced standard

ADD	LOGIC	CONDITION
FM	0	auto search
	1	forced mode
SAF	0	PAL/NTSC
	1	SECAM
FRQF	0	second crystal
	1	reference crystal

Note to table 12

1. If XA and XB indicate that only one crystal is connected to the IC and FM and FRQF force it to use the second crystal the colour will be switched off.

Table 13 Service blanking

SBL	CONDITION
0	service blanking OFF
1	service blanking ON

Table 14 Other input signals

FUNCTION	ADDRESS	DIGITAL NUMBER
hue	HU5 to HU0	000000 = –45° 111111 = +45°
horizontal shift	HS5 to HS0	000000 = –2.2 μs 111111 = +2.2 μs
EW width	EW5 to EW0	000000 = 80% 111111 = 100%
EW parabola/width	PW5 to PW0	000000 = 0% 111111 = 24%
EW corner/parabola	CP5 to CP0	000000 = 0% 111111 = –44%
EW trapezium	TC5 to TC0	000000 = –4% 111111 = +4%
vertical slope	VS5 to VS0	000000 = –14% 111111 = +14%
vertical amplitude	VA5 to VA0	000000 = –80% 111111 = +120%
S correction	SC5 to SC0	000000 = 0% 111111 = 20%
vertical shift	VSH5 to VSH0	000000 = –4% 111111 = +4%

Table 15 Standard read-out

SAK	SBK	FRQ	STANDARD
0	0	0	PAL, second crystal
0	0	1	PAL, reference crystal
0	1	0	NTSC, second crystal
0	1	1	NTSC, reference crystal
1	0	0	not used
1	0	1	SECAM, reference crystal
1	1	0	colour off
1	1	1	colour off

INPUT SIGNALS

Table 16 Power-on-reset

POR	CONDITION
0	normal mode
1	power-down mode

Table 17 Field frequency indication

FSI	CONDITION
0	50 Hz
1	60 Hz

Table 18 S-VHS status

STS	CONDITION
0	no signal at input
1	signal at input

Table 19 Phase lock indication

SL	CONDITION
0	not locked
1	locked

Table 20 Over-voltage protection

PROT	CONDITION
0	no over-voltage detected
1	over-voltage detected

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		–	8.8	V
I_{CC}	supply current		–	70	mA
P_{tot}	total power dissipation		–	–	W
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–10	+65	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	t.b.f.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	50	–	mA
P_{tot}	total power dissipation		–	400	–	mW
Input switch						
CVBS1 AND CVBS2 INPUTS (PINS 26 AND 24)						
$V_{26,24(p\text{-}p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
S-VHS Y INPUT (PIN 23)						
$V_{23(p\text{-}p)}$	input voltage (peak-to-peak value)		–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
S-VHS CHROMINANCE INPUT <PIN 22>						
$V_{22(p\text{-}p)}$	input voltage (peak-to-peak value)	burst	–	0.3	1.43	V
Z_I	input impedance		60	–	–	kΩ
LUMINANCE OUTPUT (PIN 1)						
$V_{1(p\text{-}p)}$	output voltage (peak-to-peak value)		–	450	–	mV
Z_O	output impedance		–	–	500	Ω
V_O	top sync level		–	2.1	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB
SUPP	suppression of unselected inputs		50	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TXT AND PIP OUTPUTS (PINS 25 AND 20)						
$V_{20,25(p\text{-}p)}$	output voltage (peak-to-peak value)		–	1.0	–	V
Z_O	output impedance		–	–	500	Ω
V_O	top sync level	TXT output PIP output	– –	1.8 2.8	– –	V V
SUPP	suppression of unselected inputs	f = 0 to 5 MHz; PIP output	50	–	–	dB
SUPP	suppression of unselected inputs	f = 0 to 5 MHz; TXT output	35	–	–	dB
Bias generator						
V_8	digital supply voltage		–	5.0	–	V
V_{12}	DC voltage		–	3.9	–	V
Subcarrier regeneration						
$V_{ACC(p\text{-}p)}$	burst amplitude within ACC range (peak-to-peak value)		25	–	500	mV
CR	catching range	note 1	500	–	–	Hz
φ	phase shift for 400 Hz deviation		–	–	5	deg
TC	temperature coefficient of oscillator		–	tbf	–	Hz/K
Z_I	input impedance	reference crystal input second crystal input	– –	1.0 1.5	– –	kΩ kΩ
V_{dep}	supply voltage dependency		–	tbf	–	V
Demodulators						
Δ2/Δ3	change of –(R-Y) and –(B-Y) signals over the ACC range		–	–	1	dB
	ratio of –(R-Y) and –(B-Y) signals		–	1.27	–	
TC	temperature coefficient of –(R-Y) and –(B-Y) amplitude		–	tbf	–	Hz/K
	spread of –(R-Y) and –(B-Y) ratio between standards		–1	–	+1	dB
V_2	output level of –(R-Y) during blanking		–	2.0	–	V
V_3	output level of –(B-Y) during blanking		–	2.0	–	V
B	bandwidth	at –3 dB	–	1	–	MHz
Z_O	output impedance		–	–	500	Ω
V_{dep}	supply voltage dependency		–	tbf	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL/NTSC DEMODULATOR						
$V_{2(p-p)}$	–(R-Y) output voltage (peak-to-peak value)	standard colour bar	–	525	–	mV
$V_{3(p-p)}$	–(B-Y) output voltage (peak-to-peak value)	standard colour bar	–	665	–	mV
α	crosstalk between –(R-Y) and –(B-Y)		–	tbf	–	dB
$V_{2,3(p-p)}$	8.8 MHz residue (peak-to-peak value)	both outputs	–	–	15	mV
$V_{2,3(p-p)}$	7.2 MHz residue (peak-to-peak value)	both outputs	–	–	20	mV
S/N	signal-to-noise ratio		46	–	–	dB
PAL DEMODULATOR						
$V_{R(p-p)}$	H/2 ripple (peak-to-peak value)		–	–	50	mV
S/N	signal-to-noise ratio		46	–	–	dB
NTSC DEMODULATOR						
φ	hue phase shift		–45	–	+45	deg
SECAM DEMODULATOR						
$V_{2(p-p)}$	–(R-Y) output voltage (peak-to-peak value)	standard colour bar	–	1.05	–	mV
$V_{3(p-p)}$	–(B-Y) output voltage (peak-to-peak value)	standard colour bar	–	1.33	–	mV
f_{OS}	black level offset		–	–	7	kHz
S/N	signal-to-noise ratio		–	43	–	dB
$V_{res(p-p)}$	7.8 to 9.4 MHz residue (peak-to-peak value)		–	–	30	mV
f_{pole}	pole frequency of deemphasis		77	85	93	kHz
	ratio of pole and zero frequency		–	3	–	
V_{cal}	calibration voltage		3.0	4.0	5.0	V
NL	non linearity		–	–	3	%
Filters						
V_{tune}	tuning voltage		1.5	3.0	6.0	V
Luminance delay						
t_d	delay time	PAL/NTSC/BW	–	430	–	ns
t_d	delay time	SECAM	–	480	–	ns
Luminance trap						
f_O	notch frequency	f_{SC} = 3.6 MHz f_{SC} = 4.4 MHz SECAM S-VHS/BW; not active	3.53 4.37 4.23	3.58 4.43 4.29	3.63 4.49 4.35	MHz MHz MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	bandwidth at –3 dB	f_{SC} = 3.6 MHz	–	2.8	–	MHz
		f_{SC} = 4.4 MHz	–	3.4	–	MHz
		SECAM	–	3.3	–	MHz
SUPP	subcarrier suppression		26	–	–	dB
CHROMINANCE BANDPASS						
f_{res}	resonant frequency	f_{SC} = 3.6 MHz	–	3.58	–	MHz
		f_{SC} = 4.4 MHz	–	4.43	–	MHz
B	bandwidth at –3 dB	f_{SC} = 3.6 MHz	–	1.6	–	MHz
		f_{SC} = 4.4 MHz	–	2	–	MHz
Cloche filter						
f_{res}	resonant frequency	SECAM	4.26	4.29	4.31	MHz
B	bandwidth	at –3 dB; SECAM	241	268	295	kHz
Sync input						
V_{22}	sync pulse amplitude	CVBS 1/2; S-VHS input	50	300	600	mV
	slicing level		–	50	–	%
t_d	delay of sync pulse due to internal filter		0.2	0.3	0.4	µs
S/N	noise detector threshold level		–	20	–	dB
H	hysteresis		–	3	–	dB
t_d	delay between video signal and internally separated vertical sync pulse		12	18.5	27	µs
Horizontal section						
H_A OUTPUT (PIN 10)						
V_{OH}	output voltage HIGH		2.4	5.0	5.5	V
V_{OL}	output voltage LOW		–	0.3	0.6	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	pulse width	32 clock cycles	–	4.7	–	µs
t_d	delay between middle of horizontal sync pulse and middle of H_A	note 2	0.3	0.45	0.6	µs
FIRST LOOP						
Δf	frequency deviation when not locked		–	–	1.5	%
SVRR	supply voltage ripple rejection		–	tbf	–	V
TC	temperature coefficient		–	tbf	–	Hz/°C
f_{CR}	catching range		625	–	–	Hz
f_{HR}	holding range		–	–	1400	Hz
ϕ	static phase shift		–	–	0.1	µs/kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SECOND LOOP						
φ	control sensitivity		300	–	–	µs/µs
t_{CR}	control range of the positive going edge of horizontal drive to flyback	HS = 00; note 4	13.5	–	–	µs
t_d	delay between second loop reference and mid-sync of processed video		–	3	–	µs
HORIZONTAL SHIFT						
SR	horizontal shift range	63 steps	–2.2	–	+2.2	µs
HORIZONTAL DRIVE OUTPUT (PIN 18)						
R_{18}	output resistance	on-state	–	–	50	Ω
I_{18}	output current		–	–	10	mA
	duty cycle of output current		–	55	–	%
HORIZONTAL FLYBACK INPUT (PIN 19)						
V_{HB}	switching level for horizontal blanking		–	0.3	–	V
$V_{\varphi 2}$	switching level for phase two loop		–	3.8	–	V
V_{19}	maximum input voltage		–	–	V_{CC}	V
Z_I	input impedance		10	–	–	MΩ
Soft start						
CR	duty cycle control range		2	–	55	%
	soft start time		200	300	500	lines
Vertical section (note 3)						
VERTICAL OSCILLATOR						
f_{fr}	free running frequency	divider ratio 628	–	50	–	Hz
f_{LR}	frequency locking range		43	–	64	Hz
LR	divider locking range		488	625	722	
VERTICAL SAWTOOTH (PIN 11)						
$V_{11(p-p)}$	voltage amplitude level (peak-to-peak value)	VS = 1F; C = 100 nF; R = 39 kΩ	–	3.5	–	V
I_{dis}	discharge current		–	1	–	mA
I_{charge}	charge current set by external resistor	f = 50 Hz; VS = 1F	–	19	–	µA
CR	vertical slope control range	63 steps	–14	–	+14	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL DRIVE OUTPUTS (PINS 15 AND 16)						
$I_{diff(p-p)}$	differential output current (peak-to-peak value)	VA = 1F	–	1	–	mA
$I_{15,16}$	common mode current		–	400	–	µA
V_O	output voltage range		0	–	4.0	V
EHT TRACKING AND OVER-VOLTAGE PROTECTION (PIN 14)						
TR	tracking range		1.2	–	2.8	V
SMR	scan modulation range		–6	–	+6	%
α	sensitivity		–	7.5	–	%/V
V_{14}	over-voltage protection detection level		–	3.9	–	V
DE-INTERLACE						
	first field delay		–	0.5H	–	
Sandcastle (pin 6)						
V_6	zero level		0	0.5	1.0	V
I_{sink}	sink current		0.5	–	–	mA
HORIZONTAL AND VERTICAL BLANKING						
V_{bl}	blanking voltage level		2.0	2.5	3.0	V
I_{source}	source current		0.5	–	–	mA
I_{ext}	external current required to force the output to the blanking level		1	–	3	mA
CLAMPING PULSE						
V_{clamp}	clamping voltage level		4.0	4.5	5.0	V
I_{source}	source current		0.5	–	–	mA
t_W	pulse width	PAL (17 LLC pulses) SECAM (24 LLC pulses)	– –	2.5 3.6	– –	µs µs
t_d	delay between mid sync of input and start of clamping pulse		3.6	3.7	3.8	µs
Geometry processing (note 3)						
EW WIDTH						
CR	control range	63 steps	100	–	80	%
I_{eq}	equivalent EW output current		0	–	400	µA
V_O	EW output voltage range		1.0	–	8.0	V
I_O	EW output current range		0	–	900	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW PARABOLA/WIDTH						
CR	control range	63 steps	0	–	24	%
I_{eq}	equivalent EW output current	EW = 3F	0	–	480	µA
EW CORNER/PARABOLA						
CR	control range	63 steps	–44	–	0	%
I_{eq}	equivalent EW output current	EW = 3F; PW = 3F	–210	–	0	µA
EW TRAPEZIUM						
CR	control range	63 steps	–4	–	+4	%
I_{eq}	equivalent EW output current		–80	–	+80	µA
EW EHT TRACKING						
TR	tracking range		1.2	–	2.8	V
SMR	scan modulation range		–6	–	+6	%
I_{eq}	equivalent output current		+120	–	–120	µA
φ	sensitivity		–	–7.5	–	%/V
VERTICAL AMPLITUDE						
CR	control range	63 steps; SC = 00 63 steps; SC = 3F	80 86	– –	120 112	% %
I_{eq}	equivalent differential vertical drive output current	SC = 00	800	–	1200	µA
VERTICAL SHIFT						
CR	control range	63 steps	–4	–	+4	%
I_{eq}	equivalent differential vertical drive output current		–40	–	+40	µA
S CORRECTION						
CR	control range	63 steps	0	–	20	%

Notes to the characteristics

1. All oscillator specifications are measured with the Philips crystal series 4322 143/144. The spurious response of the reference crystal must be less than –7 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ. The spurious response of the second crystal must be less than –7 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.
2. This delay is caused by the low pass filter at the sync separator input.
3. All values are valid for a reference current of 100 µA (R_C = 39 kΩ).
4. Valid for flyback pulse width of 12 µs at the switching level of the phase 2 loop.

QUALITY SPECIFICATION

Quality level according to URV 4-2-59/601.

SYMBOL	PARAMETER	RANGE A	RANGE B	UNIT
ESD	protection circuit specification (note1)	2000	500	V
		100	200	pF
		1500	0	Ω

Test and application information

EW output stage

In order to obtain the correct tracking of the vertical and horizontal EHT correction, the EW output stage should be configured as illustrated in figure 8.

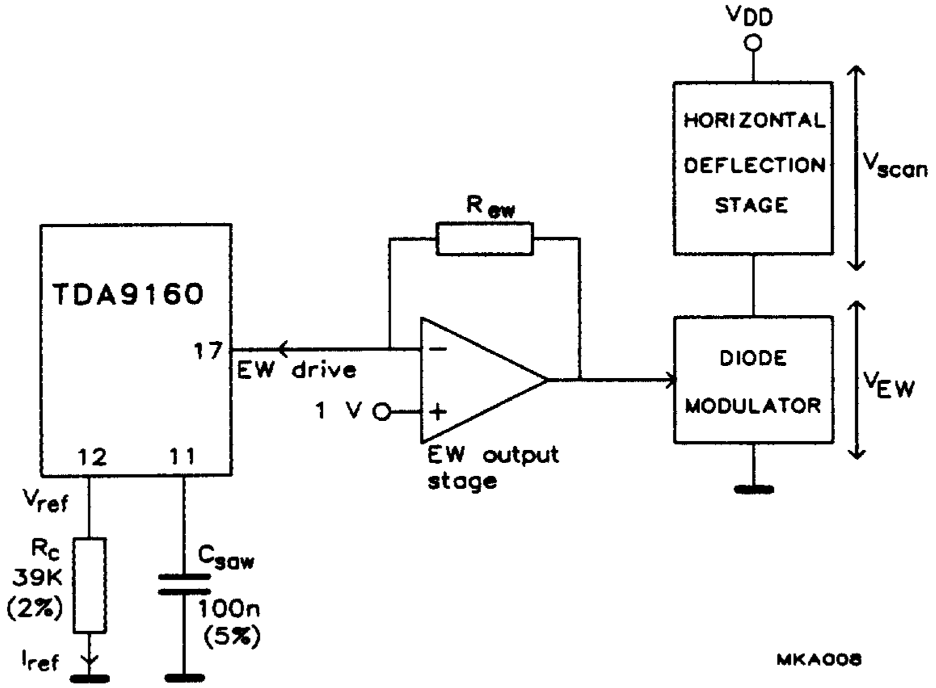


Fig.8 Configuration of the EW output stage.

Note to Fig.8

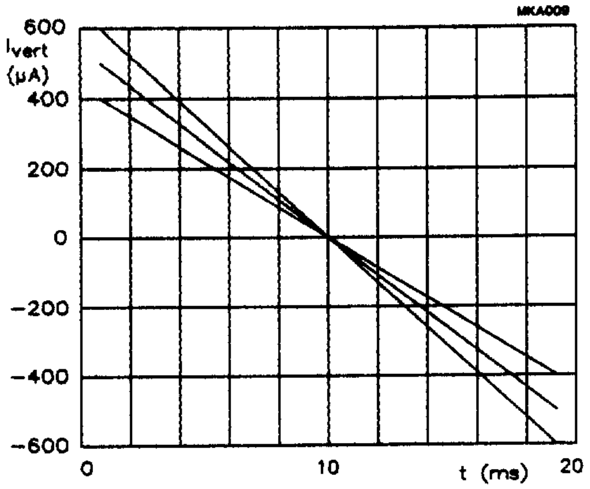
Resistor R_{ew} determines the gain of the EW output stage. Resistor R_c sets the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of R_c = 39 kΩ results in a reference current of 100 µA (V_{ref} = 3.9 V).

The value of R_{ew} is given in the following equation: $R_{ew} = R_c \times \frac{V_{scan}}{(18 \times V_{ref})}$

Example: If V_{ref} = 3.9 kΩ, R_c = 39 kΩ and V_{scan} = 120 V then R_{ew} = 68 kΩ

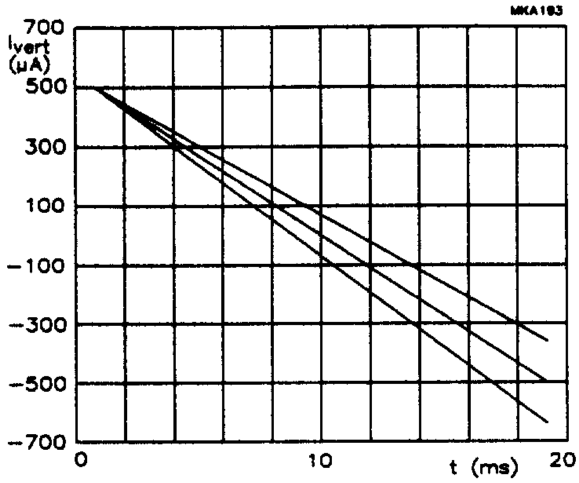
Control ranges of geometry control parameters

Typical case curves (R_c = 39 kΩ; C_{saw} = 100 nF)



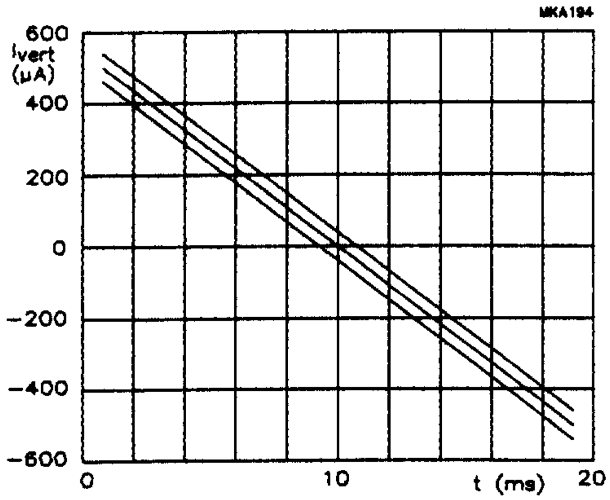
VA = 0, 31 and 63; VSH = 31; SC = 0

Fig.9 Control range of vertical amplitude.



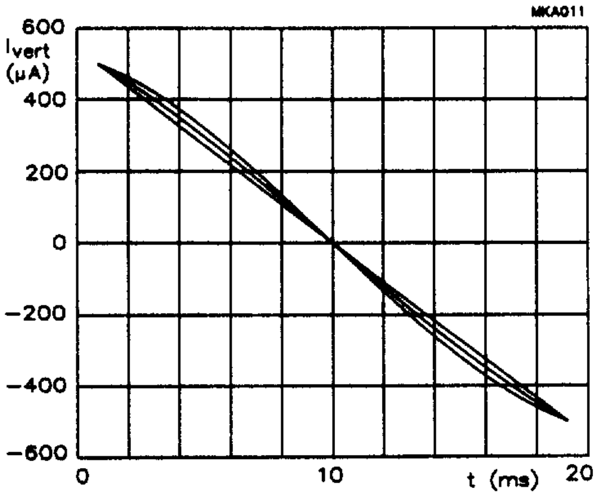
VA = 31; VS = 0, 31 and 63; VSH = 31; SC = 0

Fig.10 Control range of vertical slope.



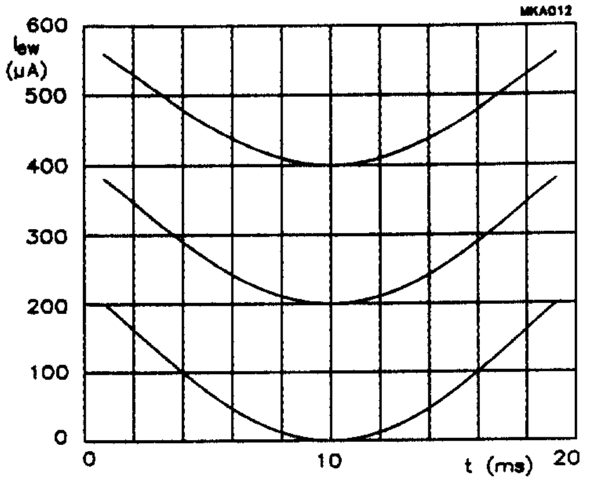
VA = 31; VSH = 0, 31 and 63; SC = 0

Fig.11 Control range of vertical shift.



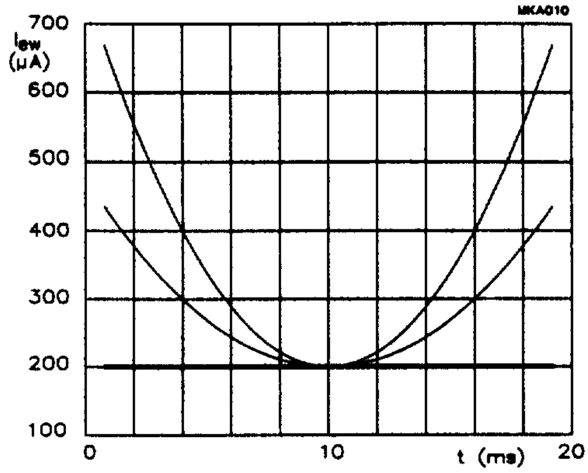
SC = 0, 31 and 63; VA = 31; VSH = 31. The picture height does not change with the setting of S correction for nominal setting of vertical amplitude (VA = 31).

Fig.12 Control range of S correction.



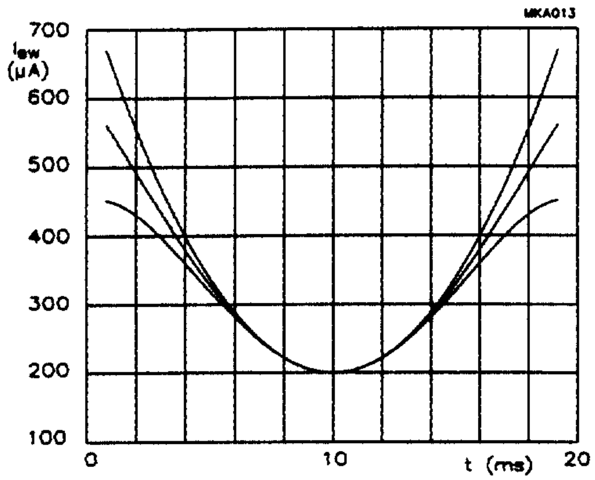
EW = 0, 31 and 63; PW = 31; CP = 31

Fig.13 Control range of EW width.



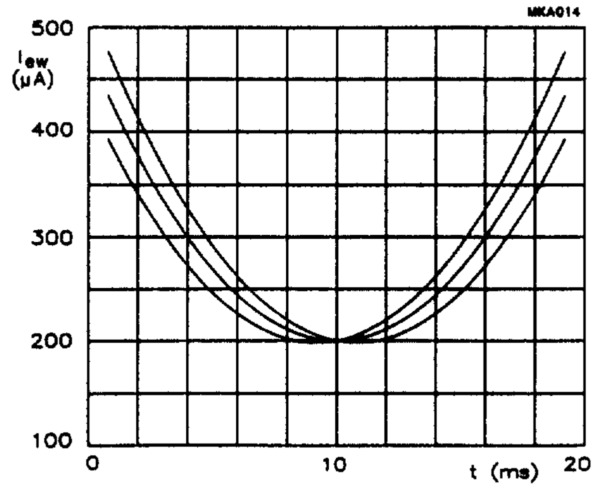
EW = 0, 31 and 63; PW = 31; CP = 31

Fig.14 Control range of EW parabola/width ratio.



CP = 0, 31 and 63; EW = 31; PW = 63

Fig.15 Control range of EW corner/parabola ratio.



TC = 0, 31 and 63; EW = 31; PW = 31; CP = 0

Fig.16 Control range of EW trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA9160 offers nine control parameters for picture alignment:

- S-correction, vertical amplitude, vertical slope and vertical shift for the vertical picture alignment
- Horizontal shift, EW width, EW parabola/width, EW corner/parabola and EW trapezium correction for the horizontal picture alignment

The required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio are determined for a particular combination of picture tube type, vertical output stage and EW output stage. These parameters can be preset via the I^2C-bus and do not require any additional adjustment.
The remainder of the parameters are preset to the mid value of their control range (i.e. 1F), or to values that have obtained from previous TV set adjustments.
After the vertical S-correction has been preset the vertical picture alignment could, in theory, be completed by positioning the top of the picture using the vertical amplitude adjustment and the bottom of the picture using the vertical slope adjustment (see note). It can be shown, however, that without compensation offsets in the external vertical output stage or in the picture tube would result in a certain linearity error especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the offset and to the square of the required S-correction. A vertical shift control is available for offset compensation.
For adjustment of the vertical shift, independent of the vertical slope, a special vertical shift alignment is provided. This mode is entered by setting the SBL bit HIGH. In this mode the –(R-Y) and –(B-Y) outputs are blanked during the second half of the picture. The first line in which the colours are blanked must be positioned in the middle of the screen. The necessity to use the vertical shift alignment depends on the expected offsets in the vertical output stage and picture tube, on the required value of the S-correction and on the demands upon the vertical linearity. If the vertical shift alignment is not used VSH should be set to its mid value (i.e. VSH = 1F).
The actual factory adjustments of the picture consist of the following steps:

- The vertical shift is adjusted as previously described (if required).
- The top of the picture is positioned by adjusting the vertical amplitude and the bottom of the picture by adjusting the vertical slope
- The picture is positioned in the horizontal direction by adjusting the EW width and horizontal shift
- The left and right hand sides of the picture are aligned in parallel by adjusting the EW trapezium correction (if required).

Note

The value of the vertical slope determines the charge current of the vertical sawtooth capacitor (C_{saw} as shown in Fig.8) and thus the amplitude of the sawtooth voltage at pin 11. This voltage serves as the input voltage for the geometry processor. Consequently the setting of the vertical slope will affect both the vertical and EW output currents.

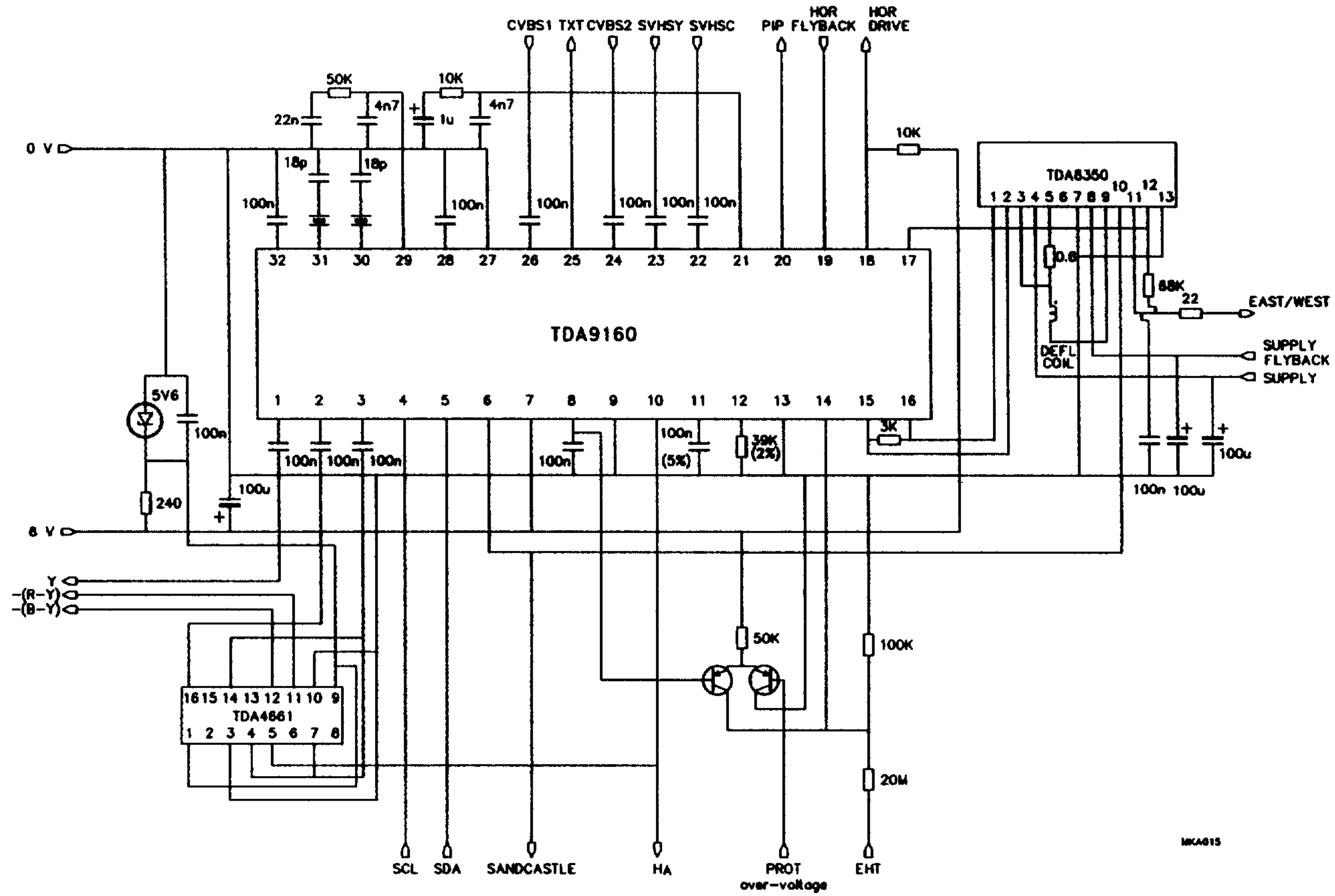


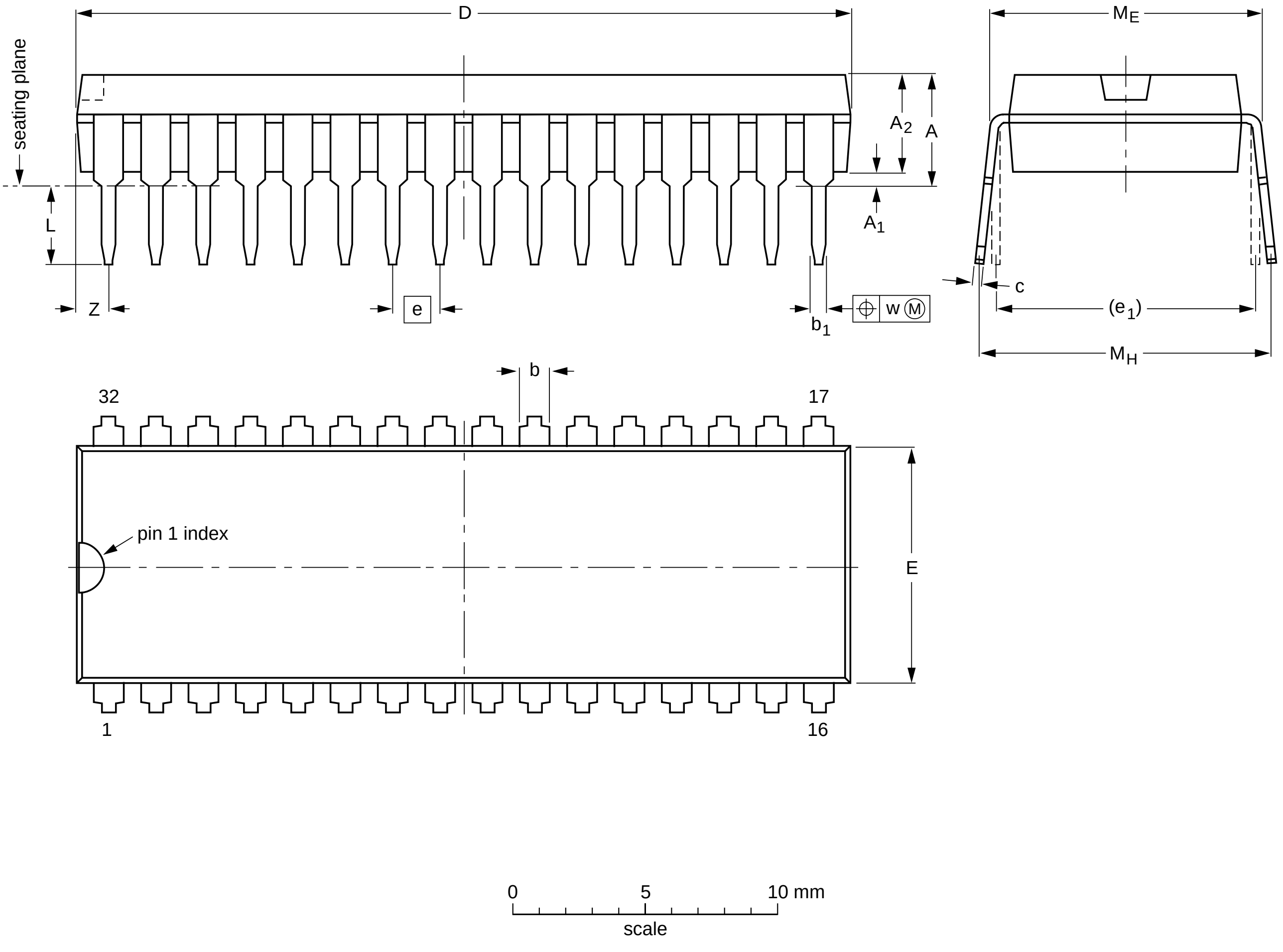
Fig.17 Application diagram.

Notes to figure 17

1. Pins 31 and 32 are sensitive to leakage current.
2. The analog and digital ground currents should be well separated.
3. The decoupling capacitor connected between pins 8 and 9 must be placed as close to the IC as possible.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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