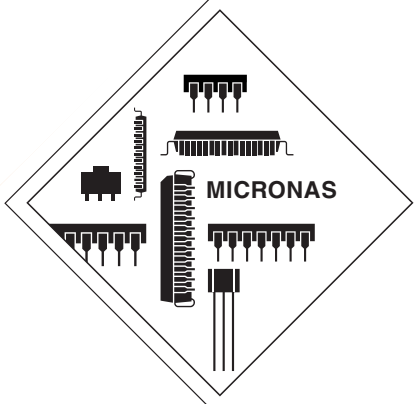

ADVANCE INFORMATION

DDP 3315C
Display and Deflection Processor

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MICRONAS

Contents

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DDP 3315C
Display and Deflection Processor

1. Introduction

The DDP 3315C is a mixed-signal single-chip digital display and deflection processor, designed for high-quality backend applications in double scan and HDTV TV sets with 4:3 or 16:9 picture tubes. The interfaces qualify the IC to be combined with state of the art digital scan rate converters, as well as analog HDTV sources. The DDP 3315C contains the entire digital video component, deflection processing, and all analog interfaces to display the picture on a CRT. The main features are

Video Processing

- linear horizontal scaling (0.25 ... 4), as well as nonlinear horizontal scaling “panorama vision”
- dynamic black level expander
- luma sharpness enhancement by dynamic peaking and luma transient improvement (LTI)
- color transient improvement (CTI)
- programmable RGB matrix
- black stretch, blue stretch, gamma correction via programmable Non-linear Colorspace Enhancer (NCE) on RGB
- two analog double scan inputs with fast blank (one RGB and one RGB/YC_rC_b/YP_rP_b selectable)
- average and peak beam current limiter
- automatic picture tube adjustment (cutoff, drive)

Deflection Processing

- scan velocity modulation output
- digital EHT compensation for vertical / east-west
- vertical angle and bow correction
- differential vertical outputs
- vertical zoom via deflection adjustment
- horizontal and vertical protection circuit
- horizontal frequency for VGA/SVGA/1080I
- black switch off procedure
- supports horizontal and vertical dynamic focus

Miscellaneous

- selectable ITU-R 601 4:1:1 / 4:2:2 YC_rC_b input at 27/32 MHz or double scan ITU-R 656 input at 54 MHz line-locked clock
- crystal oscillator for horizontal safety
- picture frame generator
- hardware for simple 50/60 Hz to 100/120 Hz conversion (display frequency doubling)
- PQFP80 package, 5 V analog and 3.3 V digital supply

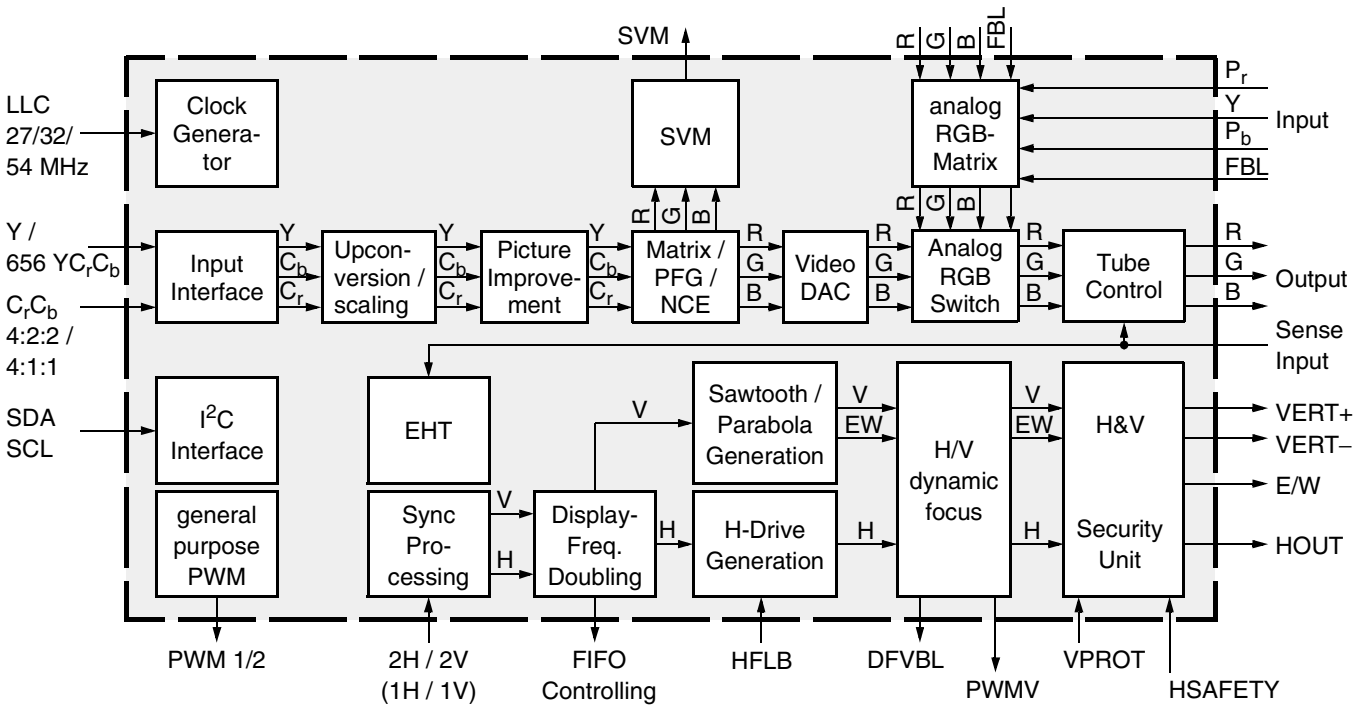


Fig. 1–1: Block diagram of the DDP 3315C

1.1. System Architecture

Fig. 1–1 shows the block diagram of the DDP 3315C.

A clock generator converts different external line locked clock rates to a common internal sample rate of ~40 MHz, in order to provide a higher horizontal resolution. The input interface accepts ITU-R 601 at 27 or 32 MHz and ITU-R 656 with encoded or external sync at 54 MHz. The horizontal scaler is used for the scan rate conversion and for the nonlinear aspect ratio conversion as well.

For the picture improvement, luma and chroma are processed separately. The luminance contrast ratio can be extended with a dynamic black level expander. In addition the frequency characteristic is improved by a transient improvement (LTI) and an adaptive dynamic peaking circuit. The peaking adapts to small AC amplitudes of high frequency parts, while large AC amplitudes are processed by the LTI. The chroma signal is enhanced with a transient improvement (CTI) with proper limitation to avoid wrong colors.

The full programmable RGB matrix covers control of color saturation and temperature. A digital white drive control is used to adjust the white balance and for the beam current limitation to prevent the CRT from overload. A non-linear colorspace enhancer (NCE) for RGB gives full flexibility for any amplitude characteristic.

High speed10-bit D/A converters are used to convert digital RGB to analog signals. Separate 9-bit D/A converters control brightness and cutoff. For picture tubes equipped with an appropriate yoke a scan velocity modulation (SVM) signal is calculated using a differentiated luminance signal.

Two analog sources can be inserted in the main RGB, controlled by separate fastblank (FBL) signals. Contrast and brightness are adjusted separately from main RGB. One input is dedicated to RGB for on screen display (OSD). The second input is processed with an analog RGB matrix to insert YC_bC_r/YP_bP_r or RGB with control of color saturation and programmable half contrast. The bandwidth of ~30 MHz guarantees pixel based graphics to be displayed with full accuracy.

All previously mentioned features are implemented in dedicated hardware. An integrated processor controls the horizontal and vertical deflection, tube measurement loops and beam current limitation. It is also used to calculate an amplitude histogram of the displayed image.

The horizontal deflection is synchronized with two numeric phase-locked loops (PLL) to the incoming sync. One PLL generates the horizontal timing signals, e.g. blanking and key-clamping. The second PLL adjusts the phase of the horizontal drive pulse with a subpixel accuracy less than 1 ns.

Vertical deflection and east/west correction waveforms are calculated as 6th order polynomials. This allows adjustment of an east/west parabola with trapezoidal, pincushion and an upper/lower corner correction (even for real flat CRT's), as well as a vertical sawtooth with linearity and S-correction. Scaling both waveforms, and limiting to fix amplitudes, performs a vertical zoom or compression of the displayed image. A field and line frequent control loop compensates picture content depending EHT distortions.

1.2. System Application

To form a complete TV set, the video backend must be complemented with additional components. Due to the flexible architecture of the DDP, it can be placed in various environments (see Fig. 1–2). Applications to display digital MPEG or PC graphics on large screens, inserting analog VGA sources in a TV as well as memory based image processing for 100/120 Hz or progressive scan rate conversion of TV sources, are intended with the DDP.

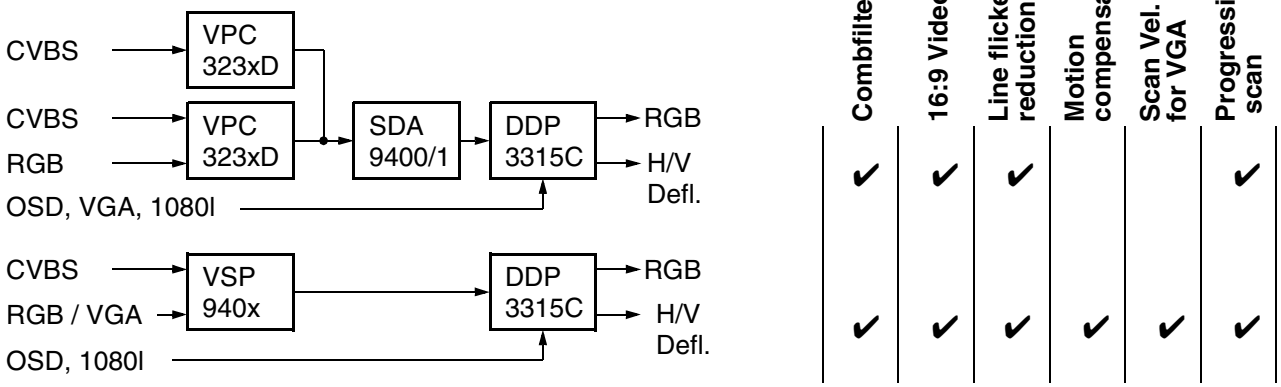


Fig. 1–2: DDP 3315C applications

2. Functional Description

2.1. Display Part

The display part converts the digital YC_rC_b to analog RGB (see Fig. 2–1). In case of YC_rC_b 4:1:1 an interpolation converts the digital input signal to YC_rC_b 4:2:2 standard format. The 4:2:2 YC_rC_b signal is processed by the horizontal scaler. In the luminance processing path, contrast and brightness adjustments and a variety of features, such as black level expander and luma sharpness enhancer, are provided. In the chrominance path, the C_rC_b signals are converted to 4:4:4 format and filtered by a color transient improvement circuit. The YC_rC_b signals are converted by a programmable matrix to RGB color space.

2.1.1. Digital Input Interface

The digital input interface supports

– 16 bit 4:2:2 YC_rC_b with separate H/V-syncs and clock (ITU-R-601 format)

– 12 bit 4:1:1 YC_rC_b with separate H/V-syncs and clock (ITU-R-601 format)

– 8 bit 4:2:2 YC_rC_b multiplexed with encoded or separate H/V-syncs and clock (ITU-R-656 format)

The data inputs Y0...Y7 and C0...C7 are clocked with the external clock LLC2. The clock frequency is selectable between 27 or 32 MHz for 12 and 16 bit data input and 54 MHz for 8 bit data input. The horizontal sync pulse at the HS pin should be an active video signal, which is not vertically blanked.

A clock generator converts the different external line locked clock rates to a common internal sample rate of approximately 40.5 MHz, in order to provide a fix bandwidth for all digital filters. Therefore the input data is sample rate converted to the common processing frequency by the horizontal scaler.

2.1.2. Chroma Input

The chroma input signal can either be YC_rC_b in 4:1:1 or in 4:2:2 format. For the digital signal processing the time-multiplexed chroma samples will be demultiplexed, synchronized with the signal at the HS Pin. The input formatter accepts either two's complement or binary offset code. Also the delay can be adjusted within a range of ±2 input clocks relative to the luma signal; this doesn't effect the chroma multiplex.

Table 2–1: 4:1:1 chroma format

Pin Name	Pixel Number			
	1	2	3	4
C7	C_{b1}^{7}	C_{b1}^{5}	C_{b1}^{3}	C_{b1}^{1}
C6	C_{b1}^{6}	C_{b1}^{4}	C_{b1}^{2}	C_{b1}^{0}
C5	C_{r1}^{7}	C_{r1}^{5}	C_{r1}^{3}	C_{r1}^{1}
C4	C_{r1}^{6}	C_{r1}^{4}	C_{r1}^{2}	C_{r1}^{0}

Table 2–2: 4:2:2 chroma format

Pin Name	Pixel Number			
	1	2	3	4
C7	C_{b1}^{7}	C_{r1}^{7}	C_{b3}^{7}	C_{r3}^{7}
C6	C_{b1}^{6}	C_{r1}^{6}	C_{b3}^{6}	C_{r3}^{6}
C5	C_{b1}^{5}	C_{r1}^{5}	C_{b3}^{5}	C_{r3}^{5}
C4	C_{b1}^{4}	C_{r1}^{4}	C_{b3}^{4}	C_{r3}^{4}
C3	C_{b1}^{3}	C_{r1}^{3}	C_{b3}^{3}	C_{r3}^{3}
C2	C_{b1}^{2}	C_{r1}^{2}	C_{b3}^{2}	C_{r3}^{2}
C1	C_{b1}^{1}	C_{r1}^{1}	C_{b3}^{1}	C_{r3}^{1}
C0	C_{b1}^{0}	C_{r1}^{0}	C_{b3}^{0}	C_{r3}^{0}

Note: C_x^y; x = pixel number; y = bit number

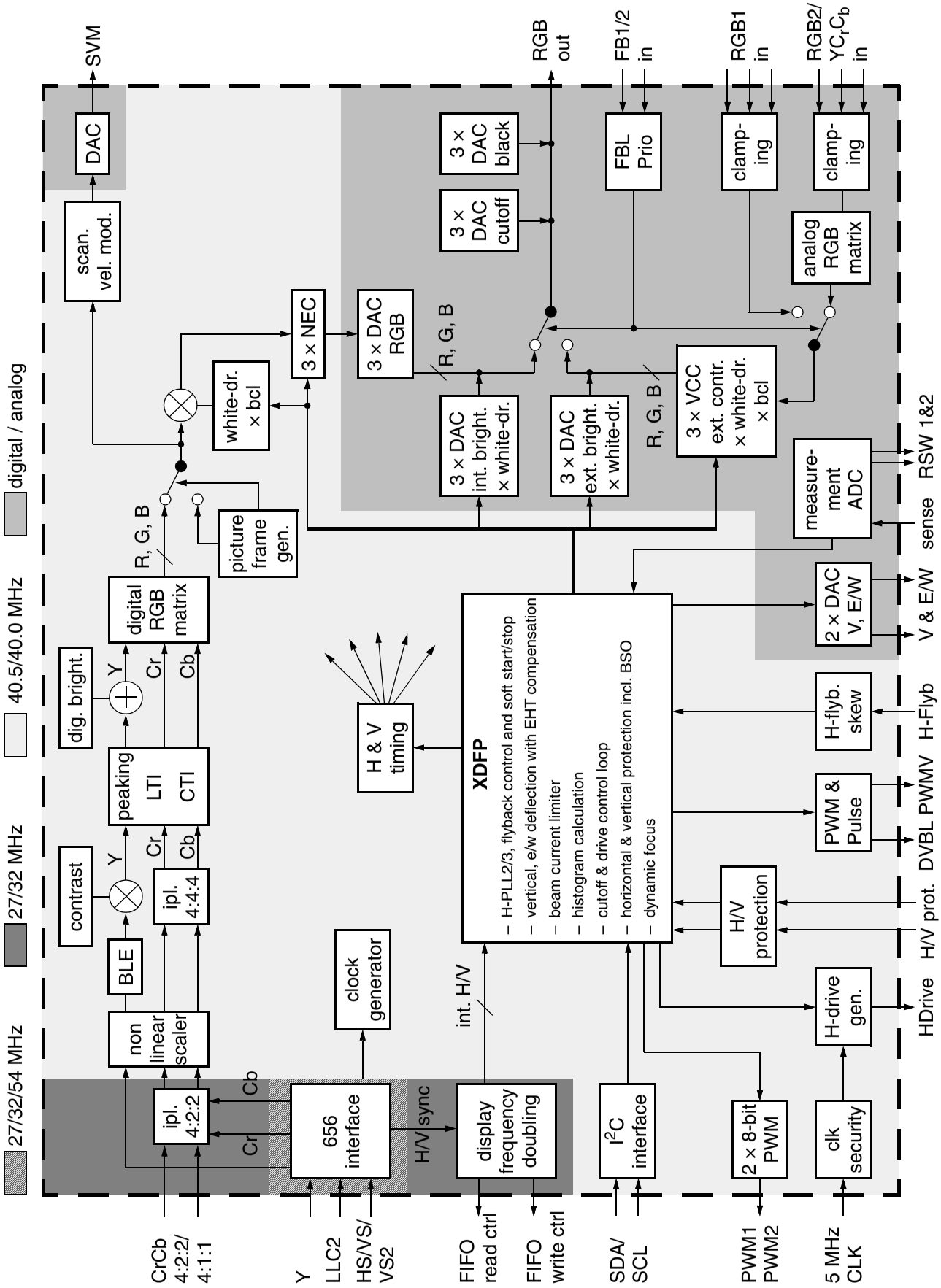


Fig. 2–1: Detailed block diagram

2.1.3. Horizontal Scaler

The horizontal scaler supports linear or nonlinear horizontal scaling of the digital input video signal in the range of 0.25 to 4. Nonlinear scaling, also called “panorama vision”, provides a geometrical distortion of the input picture. It is used to fit a picture with 4:3 format on a 16:9 screen by stretching the picture geometry at the borders. Also, the inverse effect can be produced by the scaler.

A summary of scaler modes is given in Table 2–3.

Table 2–3: Scaler modes

Mode	Scale Factor	Description
Panorama 4:3 ➔16:9	non linear compr.	4:3 source displayed on a16:9 tube, borders distorted
Panorama 4:3 ➔ 4:3	non linear zoom	Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan, borders distorted, no cropping
27 ➔ 40.5 MHz	1.5 linear	sample rate conversion from external to internal pixel clock
32 ➔ 40 MHz	1.25 linear	sample rate conversion from external to internal pixel clock

2.1.4. Luma Contrast and Brightness

The luminance signal is multiplied by a factor of 0...2 in 64 steps. Simultaneously the matrix coefficients are adapted to preserve the color saturation (see Section 2.1.9. on page 11)

With a contrast adjustment of 32 (gain=1) the signal can be shifted by ±100% of its maximal amplitude with the digital brightness value. This is for adjustment of the headrooms for under- and overshoot. After the brightness addition, the negative going signals are limited to zero. It is desirable to keep a small positive offset with the signal to prevent undershoots produced by the peaking from being cut.

2.1.5. Black Level Expander/Compressor (BLEC)

The black level expander/compressor modifies the luminance signal with an adjustable non-linear function to enhance the contrast of the picture (see Fig. 2–2). Dark areas are stretched to black, while bright areas remain unchanged. Advantageously, this black level processing is performed dynamically and only if it will be most noticeable to the viewer.

The BLEC supports the following modes (see Fig. 2–3):

– dynamic BLEC mode
  This is the normal operation mode. The expansion depends on a pixel analysis.

– auto contrast mode
  In the auto contrast mode, the TILT point is shifted to its maximum.

– static BLEC mode
  In the static mode, the expansion depends on a programmable value SBLE.

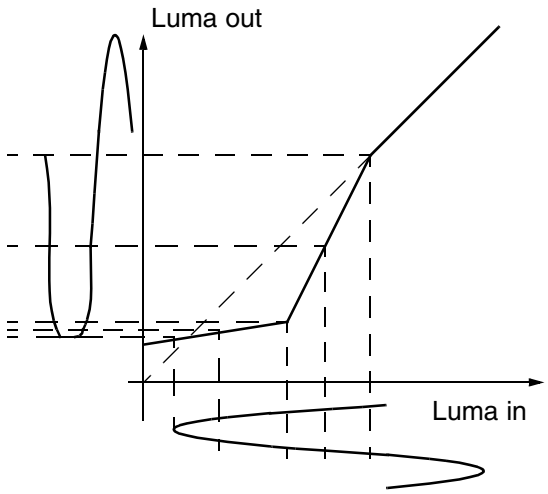
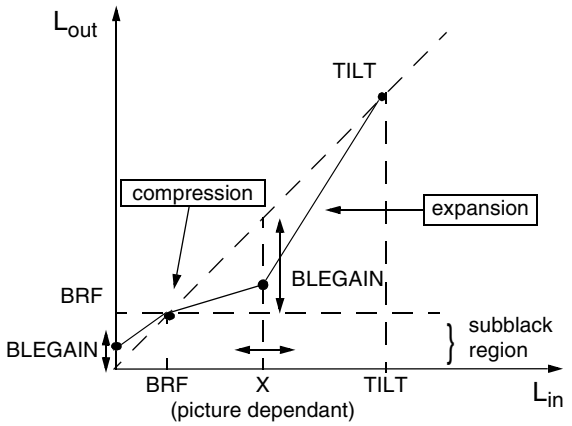
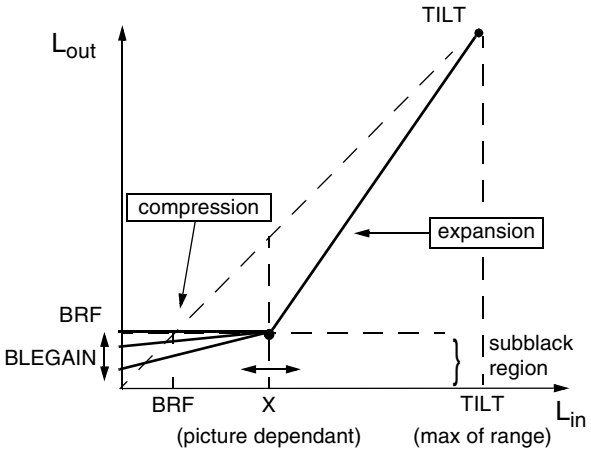


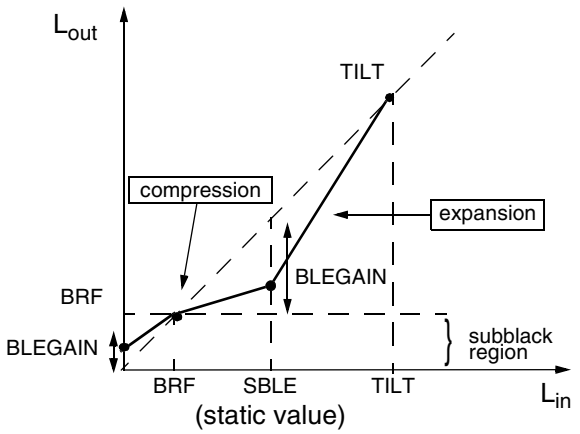
Fig. 2–2: BLEC function



Dynamic BLEC mode



Autocontrast mode



Static BLEC mode

Fig. 2–3: BLEC modes

2.1.6. Luma Sharpness Enhancer (LSE)

Sharpness is one of the most critical features for optimum picture quality. This important processing is performed in the LSE circuitry of DDP 3315C.

It consists of the dynamic peaking, the luma transient improvement (LTI) and an adaptive mixer. The luma input signal is processed in the peaking and LTI block in parallel. Both output signals are combined in the mixer depending on the selected LSE characteristic.

2.1.6.1. Dynamic Peaking

The dynamic peaking improves the details of a picture by contour emphasis. It adapts to the amplitude and the frequency of the input signal. Small detail amplitudes are sharpened, while large detail amplitudes stay nearly unmodified.

The max. dynamic range of small high-frequency detail amplitudes is 14 dB. The dynamic range of large detail amplitudes is limited automatically by a non-linear function that does not create any visible alias components (see Fig. 2–4).

The peaking features two selectable center frequencies of 2.5 MHz or 3.2 MHz (see Fig. 2–5). An adjustable coring threshold prevents the enhancement of small noise amplitudes.

2.1.6.2. Luma Transient Improvement (LTI)

For small detail amplitudes the dynamic peaking is the most appropriate processing to improve the sharpness. However, for large amplitudes even small over- and/or undershoots of the peaking are too annoying.

The luma transient improvement enhances the slope of picture detail without these effects by a non-linear processing. The contour correction signal calculated in this block, is limited to the adjacent extreme values to prevent over- and undershoots (see Fig. 2–7).

The LTI features an adjustable gain control and an adjustable coring threshold to prevent the enhancement of small noise amplitudes.

The contour correction signals of the dynamic peaking and the LTI block are combined adaptively to achieve best sharpness impression.

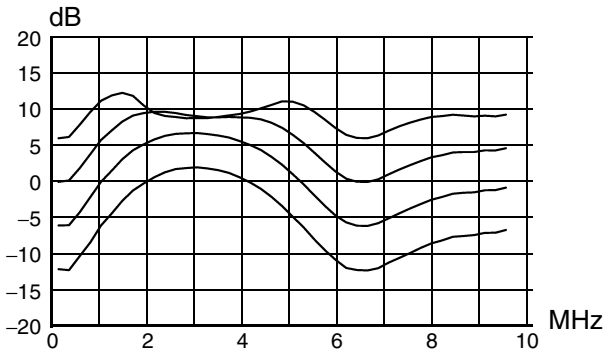


Fig. 2–4: Dynamic peaking frequency response

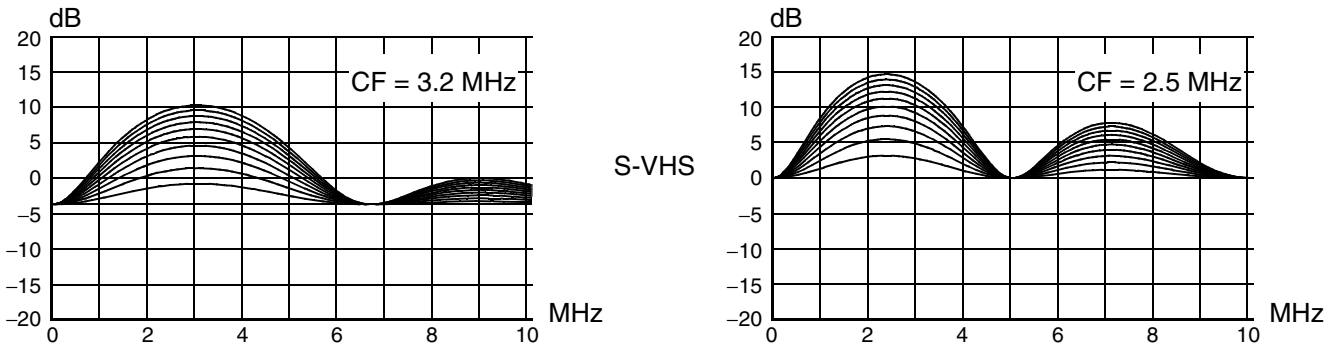


Fig. 2–5: Dynamic peaking frequency response in S-VHS (all frequencies refers to a 50/60 Hz video signal)

2.1.7. Chroma Interpolation

In case of YC_rC_b 4:1:1 input format, the digital input signal is converted to 4:2:2 format by an interpolation filter working at the input pixel clock frequency.

The signal is passed to the scaler in YC_rC_b 4:2:2 format, in order to convert the incoming pixel clock frequency (27/32 MHz) to the internal frequency (40.5/ 40 MHz).

A linear phase interpolator is used to convert the chroma sampling rate from 4:2:2 to 4:4:4. The frequency response of the interpolator is shown in Fig. 2–6. All further processing is carried out at the full sampling rate.

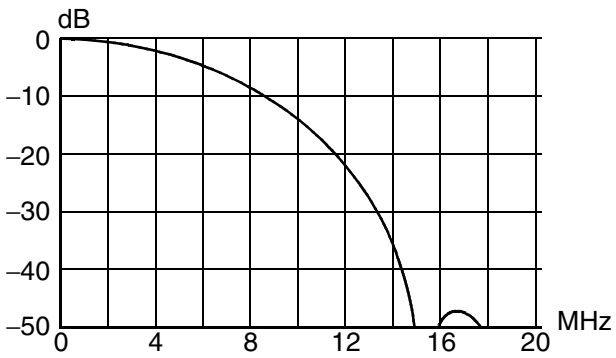
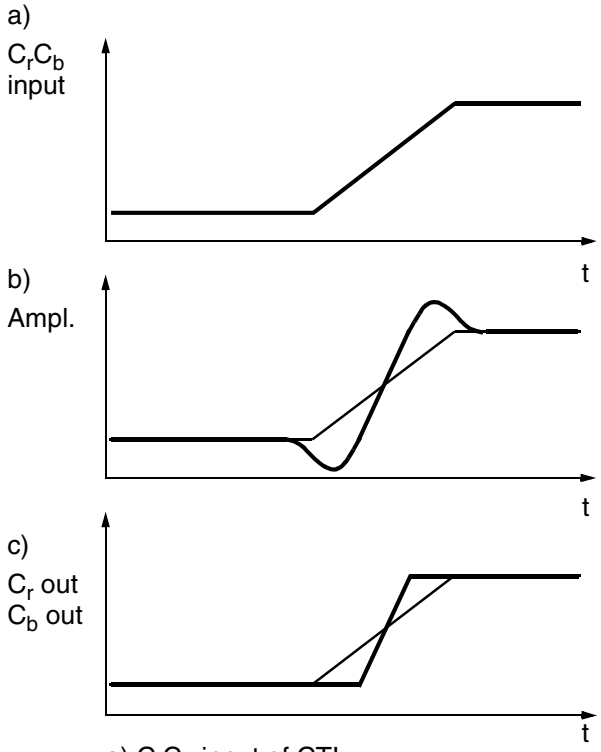


Fig. 2–6: Frequency response of the chroma 4:2:2 to 4:4:4 interpolation filter

2.1.8. Chroma Transient Improvement

The intention of this block is to enhance the chroma resolution. A correction signal is calculated by differentiation of the color difference signals. The differentiation can be selected according to the signal bandwidth, e.g. for PAL/NTSC/SECAM or digital component signals, respectively. The amplitude of the correction signal is adjustable. Small noise amplitudes in the correction signal are suppressed by an adjustable coring circuit. To eliminate “wrong colors”, which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically (see Fig. 2–7).



a) C_rC_b input of CTI
b) C_rC_b input + correction signal
c) sharpened and limited C_rC_b

Fig. 2–7: Luma/chroma transient improvement

2.1.9. Inverse Matrix and Digital RGB Processing

Six multipliers in parallel perform the matrix multiplication to transform the C_r and C_b signals to R-Y, B-Y, and G-Y. The initialization values for the matrix are computed from the standard ITU-R matrix:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1{,}402 \\ 1 & -0{,}345 & -0{,}713 \\ 1 & 1{,}773 & 0 \end{bmatrix} \times \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix}$$

The multipliers are also used to adjust color saturation and picture contrast. The matrix computes:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \frac{CTM}{32} \times \frac{SATM}{32} \times \frac{1}{64} \times \begin{bmatrix} MR1M & MR2M \\ MG1M & MG2M \\ MB1M & MB2M \end{bmatrix} \times \begin{bmatrix} Cb \\ Cr \end{bmatrix} + \left(\frac{CTM}{32} \times Y \right)$$

2.1.10. Picture Frame Generator

The picture frame generator produces a programmable border surrounding the displayed image. By swapping the start and stop parameters a windows is produced instead.

The color of the complete border is stored in a programmable frame register. The format is 3x4 bit RGB. The contrast can be adjusted separately.

2.1.11. Scan Velocity Modulation

Picture tubes equipped with an appropriate yoke can use the Scan Velocity Modulation signal to vary the speed of the electron gun during the entire video scan line dependent upon its content. Transitions from dark to bright will first speed up and then slow down the scan; vice versa for the opposite transition (see Fig. 2–8).

The signal delay is adjustable by ±3.5 clocks in half-clock steps in respect to the analog RGB output signals. This is useful to match the different groupdelay of analog RGB amplifiers to the one for the SVM yoke current.

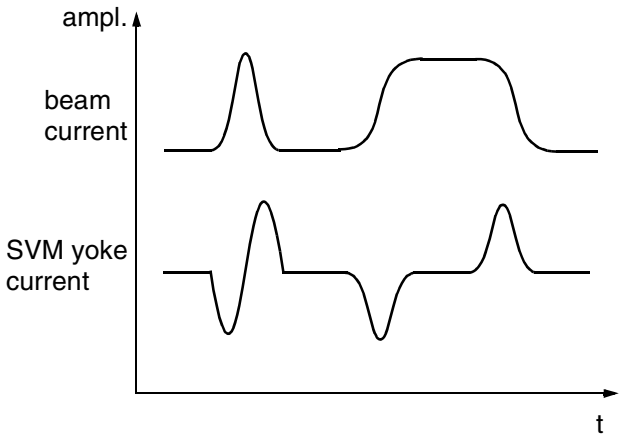


Fig. 2–8: SVM signal waveform

2.1.12. Non-linear Colorspace Enhancer (NCE)

This block allows all kinds of non-linear functions such as gamma correction, blue stretch, peak white limitation, for each path R,G and B separately. In the following only one path is described (see Fig. 2–9).

Whereas the full input range of the NCE is 0...2047, the non-linear function is a combination of 8 I^2C programmable linear segments S_0 to S_7 lying in the range 0...1023. Beyond 1023, the non-linear curve consists of the continuation of S_7 and the limitation to 1023.

If the segments S_0 to S_7 cover the full input range from 0 to 1023 they can be placed on a grid of 32. In the case where all segments lie in a smaller range, the following modes with higher precision are available.

Table 2–4: Input range and grid covered by S_0...S_7

Mode	Range	Grid
XSEG = 0	0...1023	32
XSEG = 1	0...511	16
XSEG = 2	0...255	8
XSEG = 3	0...127	4

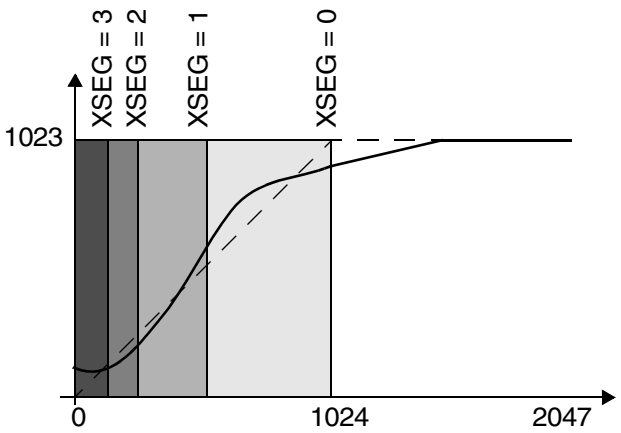


Fig. 2–9: NCE characteristic

2.2. Analog Back End

The digital RGB signals are converted to analog RGB by three 10-bit digital to analog converters (DAC).

Each RGB signal has two additional DACs with 9-bit resolution to adjust analog brightness (40% of the full RGB range) and cutoff / black level (60% of the full RGB range). An additional fixed current is applied for the blanking level.

The back-end supports the insertion of two external analog component signals, e. g. OSD or analog HDTV. These signals are clamped, processed in an analog matrix (RGB2), converted by a voltage/current converter (VCC), and inserted into the main RGB by the fast blank switch.

The analog RGB outputs are current outputs with current-sink characteristics. The maximum current drawn by the output stage is obtained with peak white RGB.

The controlling of the whitedrive/analog brightness and also the external contrast and brightness adjustments is done via the internal Processor.

2.2.1. Analog RGB Insertion

The DDP 3315C supports the insertion of

– 2 external analog RGB signals or

– 1 external analog RGB and 1 external YC_rC_b/YP_rP_b signal.

Each component signal is clamped, converted to RGB if required, and inserted into the main RGB by the fast blank switch. The external component signals are adjustable independently as regards DC level (brightness) and magnitude (contrast).

The second external analog input is processed by an analog matrix with control of color saturation and programmable half contrast.

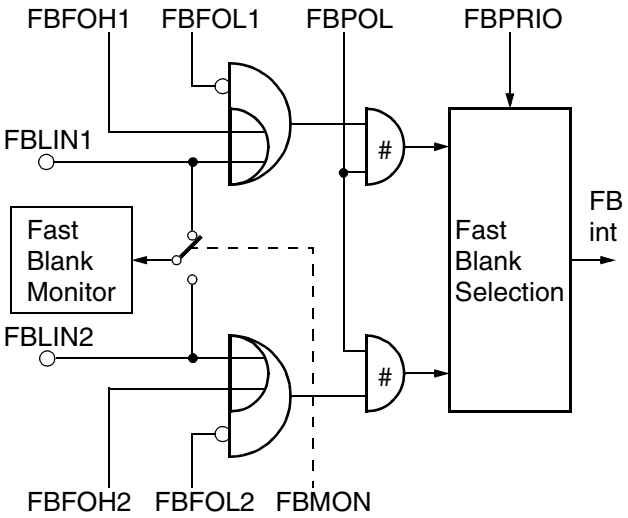


Fig. 2–10: Fast Blank selection logic

Over-/underlay of the external component signal and the main RGB signal depends on the fast blank input signals and the corresponding I^2C-register (see Fig. 2–10). Both fast blank inputs must be either active low or active high.

All signals for analog component insertion (RIN1/2, GIN1/2, BIN1/2, FBLIN1/2, HCS) must be synchronized to the digital RGB.

External YC_rC_b/YP_rP_b signals are converted to RGB by the following matrix.

Table 2–5: Matrix coefficients for 480P and 1080I

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & K_{rr} \\ 1 & K_{gb} & K_{gr} \\ 1 & K_{bb} & 0 \end{bmatrix} \otimes \begin{bmatrix} Y \\ C_b \\ C_r \end{bmatrix}$$

	I^2C Setting		
MAT-Type	**0 1 0**	**1 0 0**	**0 0 1**
Standard	**ITU-R 601 / 480P (SMPTE 293M)**	**1080I (ITU-R709)**	**RGB (Bypass)**
K_{rr}	1.402	1.575	0
K_{gb}	–0.344	–0.187	0
K_{gr}	–0.7144	–0.468	0
K_{bb}	1.773	1.856	0

2.2.2. Fast Blank Monitor

The presence of external analog RGB sources can be detected by means of a fast blank monitor. The status of the selected fast blank input can be monitored via an I^2C register. There is a 2 bit information, giving static and dynamic indication of a fast blank signal. The static bit is directly reading the fast blank input line, whereas the dynamic bit is reading the status of a flip flop triggered by the negative edge of the fast blank signal.

With this monitor logic it is possible to detect if there is an external RGB source active and if it is a full screen insertion or only a box. The monitor logic is connected directly to the FBLIN1 or FBLIN2 pin. Selection is done via I^2C register.

2.2.3. Half Contrast Control

Insertion of transparent text pages or OSD onto the video picture is often difficult to read, especially if the video contrast is high. The DDP 3315C features a contrast reduction of the video background of 30 or 50% by means of a half contrast input (HCS pin). This input can be supplied with a fast switching signal (similar to the fast blank input), typically defining a rectangular box. Inside this box the video picture is displayed with reduced contrast, while the analog component signals are still displayed with full contrast.

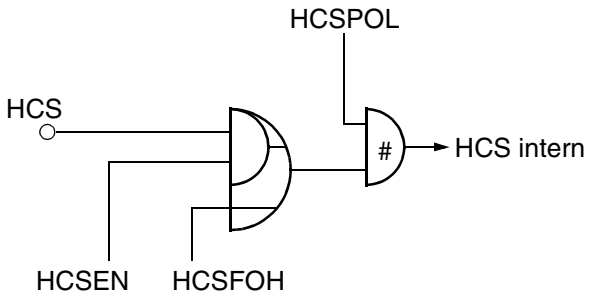


Fig. 2–11: Half Contrast switch logic

2.2.4. CRT Measurement and Control

In order to define accurate color on different CRT displays, the cut-off and white drive settings have to be adjusted depending on the characteristic of CRT phosphor. To guarantee correct colors during the for the lifetime of the display, a build in automatic tube control loop measures and adjusts the black level on every field and white point every third field.

The display processor is equipped with an 9/12-bit PDM-ADC for all picture tube measuring purposes. This MADC is connected to the SENSE input pin, the input range is 0 to 2.6 V.

Cutoff and white drive current measurement are carried out with 8-bit resolution during the vertical blanking interval. The current range for cutoff measurement is set by connecting the sense resistor R1 to the SENSE input. Due to the fact of a 1:10 relation between cutoff and white drive current the range select 2 output (RSW2) becomes active for the white drive measurement and connects R3 in parallel to R1, thus determining the correct current range. During the active picture, the MADC is used for the average beam current limiter with a 12-bit resolution. Again a different measurement range is selected with active range select 1&2 outputs (RSW1&RSW2) connecting R2 in parallel to R3 and R1. See Fig. 2–12 and Fig. 2–13 for the corresponding timing.

These measurements are typically done at the summation point of the picture tube cathode currents.

Another method uses two different current measurements:

– The range switch 1 pin (RSW1) can be used as a second sense input, selectable by software. In this case, the cutoff and white drive currents are measured as before at the SENSE input.
– The active picture measurement can be done with the second sense input (RSW1). The signal may come (via a proper interface) from the low end of the EHT coil (CRT anode current). In this case, the resistor R2 in Fig. 2–12 has to be removed.

The picture tube measurement returns results on every field for:

– cutoff R
– cutoff G
– cutoff B
– white drive R or G or B (sequentially)

Thus a cutoff control cycle for RGB requires one field only, while a complete white drive control cycle requires three fields. During cutoff and whitedrive measurement, the average beam current limiter function (see Section 2.2.5.) is switched off. The amplitude of the cutoff and white drive measurement lines can be programmed separately with IBRM and WDRM (see Fig. 2–13). The start line for the tube measurement (cutoff red) can be programmed via I^2C-bus (TML).

The built-in control loop for cutoff and white drive can operate in three different modes selected by CUT(WDR)_GAIN and CUT(WDR)_DIS.

– The user control mode is selected by setting CUT(WDR)_GAIN = 0. In this mode the registers CUT(WDR)_R/G/B are used as direct control values for cutoff and drive. If the measurement lines are enabled (CUT(WDR)_DIS = 0) the user can read the measured cutoff & white drive values in the CUTOFF(WDRIVE)_R/G/B registers. An external software can now control the settings of the CUT(WDR)_R/G/B registers.
– The automatic mode is selected by setting CUT(WDR)_GAIN > 0 and CUT(WDR)_DIS = 0. In this mode, the registers CUT(WDR)_R/G/B are used as reference for the measured values (CUTOFF(WDRIVE)_R/G/B). The calculated error is used with a small hysteresis (1.5%) to adjust cutoff and drive. The higher the loopgain (CUT(WDR)_GAIN) the smaller the time constant for the adjustment.
– If the automatic mode was once enabled (CUT(WDR)_GAIN > 0), the control loop can be stopped by setting CUT(WDR)_DIS = 1. In this mode the calculated cutoff and drive values will no longer be modified and the measurement lines are suppressed. Changes of the reference values (CUT(WDR)_R/G/B) have no effect.

If one of the calculated red, green or blue white drive values exceeds it's maximal possible value (WDR_R/G/B>511), the white balance gets misadjusted. An automatic drive saturation avoidance prevents from this effect (WDR_SAT = 1). If one drive value exceeds the maximum allowed threshold (MAX_WDR) the amplitude of the white drive measurement line will be increased and decreased if one of them goes below the fixed threshold 475.

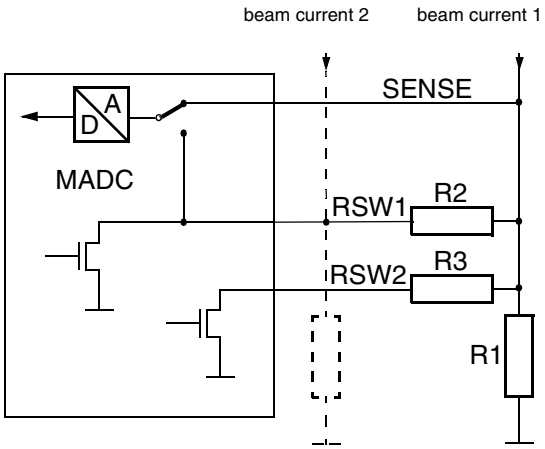


Fig. 2–12: MADC range switch

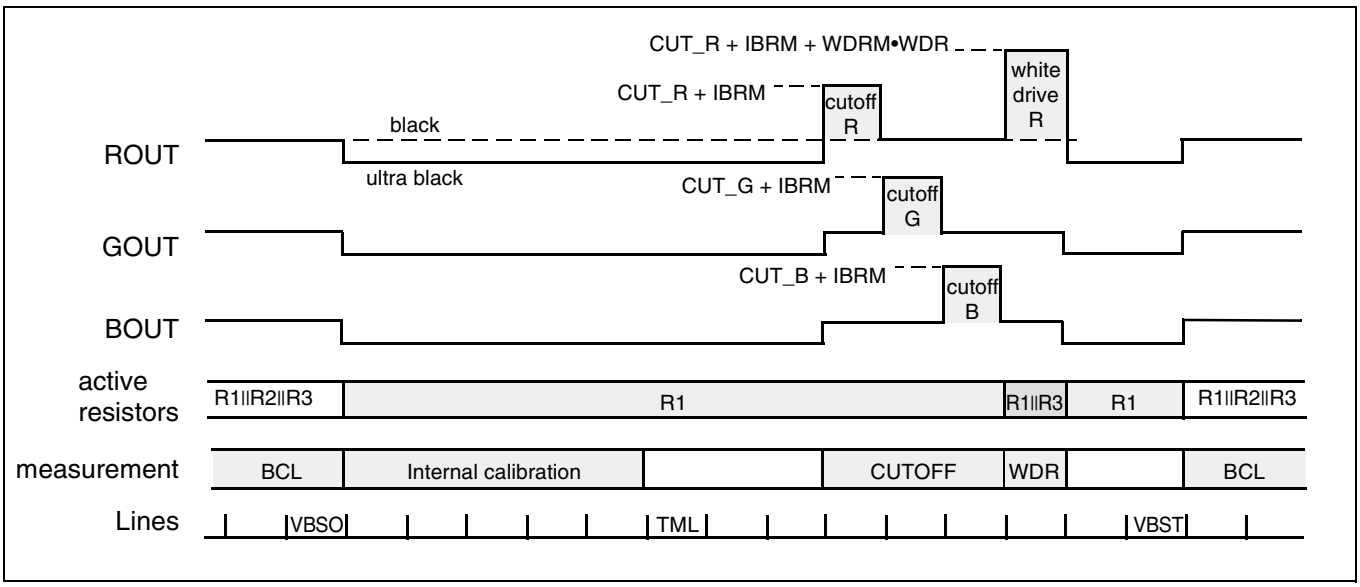


Fig. 2–13: MADC measurement timing

2.2.5. Average Beam Current Limiter

The average beam current limiter (BCL) works on both the digital YC_rC_b input and the inserted analog RGB signals by using either the sense input or the RSW1 input for the beam current measurement. The BCL uses a different filter to average the beam current during the active picture resulting in a 12-bit resolution. The filter bandwidth is approximately 4 kHz.

The beam current limiter allows the setting of a threshold current, a gain and an additional time constant. If the beam current is above the threshold, the excess current is low-pass filtered with the according gain and time constant. The result is used to attenuate the RGB outputs by adjusting the white drive multipliers for the internal (digital) RGB signals, and the analog contrast multipliers for the analog RGB inputs, respectively. The lower limit of the attenuator is programmable, thus a minimum contrast can always be set. If the minimum contrast is reached, the brightness will be decreased to a programmable minimum as well. Typical characteristics of the BCL for different loop gains are shown in Fig. 2–14; for this example the tube has been assumed to have square law characteristics.

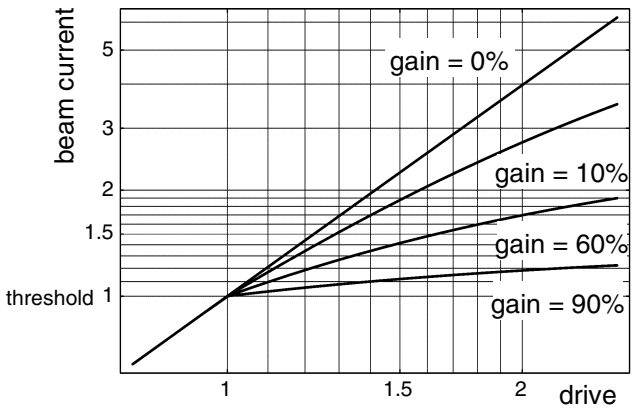


Fig. 2–14: Beam current limiter characteristics: beam current output vs. drive

2.3. Synchronization and Deflection

2.3.1. Deflection Processing

The deflection processing generates the signals for the horizontal and vertical drive (see Fig. 2–15). This block contains two numeric phase-locked loops and a security unit:

– PLL2 generates the horizontal and vertical timing, e.g. blanking, clamping and sync signals. Phase and frequency are synchronized by the incoming sync signals.

– PLL3 adjusts the phase of the horizontal drive pulse and compensates for the delay of the horizontal output stage.

– The security unit observes the H-Drive output signal. With an external 5 MHz reference clock this unit controls the H-drive “off time” and period. In case of an incorrect H-drive signal the security unit generates a free running h-drive signal divided down from the 5 MHz reference clock.

The DDP 3315C is able to synchronize to various horizontal frequencies, even VGA frequencies. Supported horizontal input frequencies are listed in Table 2–6.

2.3.2. Security Unit for H-Drive

The security unit observes the H-Drive output signal with an external 5 MHz reference clock. For different horizontal frequencies the security unit uses different ranges to control the H-Drive signal. Selecting a specific horizontal frequency via I^2C-Register HFREQ, automatically switches to the corresponding security range. The control ranges are listed in Table 2–6.

The window of the control range has to lie within a main control window which is selectable with the FREQSEL input pin. With a low signal at this pin the main control range is 28.8... 34.4 µs and with a high signal the main control range is 25.6... 29.2 µs.
This is to prevent male functions if the horizontal deflection stage is prepared for VGA frequencies.

The Horizontal Drive Output can be forced to the high level during Flyback. This means, the falling edge of the drive pulse is earliest possible at the end of the flyback pulse. This function can be enabled via the I2C bus (EFLB).

Table 2–6: Supported horizontal input frequencies

Supply Clock (MHz)	Pixels per line Supply clk	Main clock (in MHz)	Pixels per line Main clk	horiz. freq. (Hz)	Minimum H-Drive period (in µs)	Maximum H-Drive period (in µs)	HFREQ (I^2C)
27	864	40.5	1296	31.24968	29.60	34.40	000
27	858	40.5	1287	31.46853	29.60	34.40	010
27	800	40.5	1200	33.750	28.80	30.60	100
27	768	40.5	1152	35.15625	27.80	29.20	001
27	720	40.5	1080	37.500	25.60	28.00	101
27	712	40.5	1068	37.92135	25.60	28.00	110
32	1024	40.0	1280	31.24952	29.60	34.40	000
32	944	40.0	1180	33.89776	28.80	30.60	100
32	912	40.0	1140	35.08747	27.80	29.20	001
32	852	40.0	1065	37.55869	25.60	28.00	101
32	844	40.0	1055	37.91469	25.60	28.00	110
40.5	1296	40.5	1296	31.24968	29.60	34.40	000

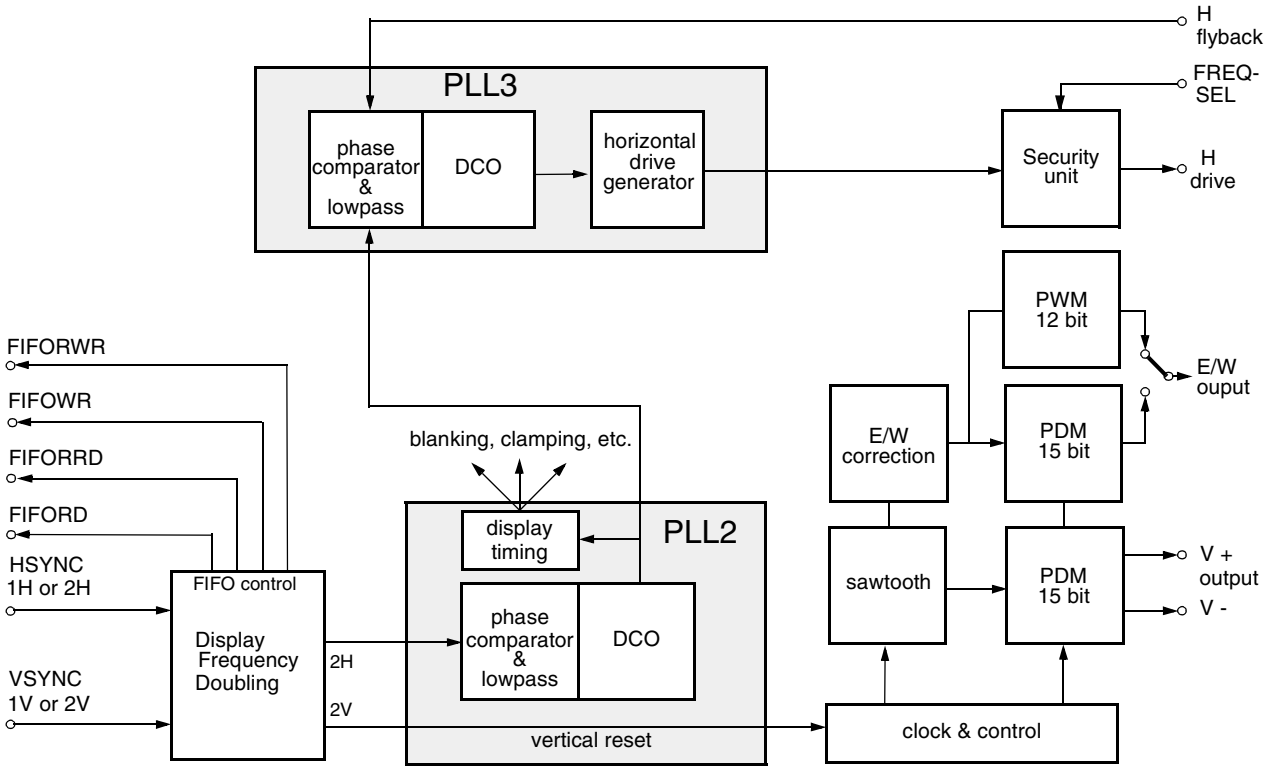


Fig. 2–15: Deflection processing block diagram

2.3.3. Horizontal Phase Adjustment

This section describes a simple way to get a correct horizontal frame position and clamp window for analog RGB insertion.

1. For a correct scaler function in panorama/waterglass mode the digital input data should be centered to the active video input signal.

2. The clamping pulse for analog RGB insertion can be adjusted to the pedestal of the input signal with POFS2.

3. The horizontal raster position of the analog inserted RGB1/2 signal can be set to the desired frame position with POFS3.

4. The horizontal position of the digital RGB signal can be shifted to the left and right with NEWLIN. Following values allowed in respect to POFS2:

$90 < (POFS2+NEWLIN) - (clk \bullet SFIF) < 580$

clk = 3 @ LLC2 = 27 MHz

clk = 2,5 @ LLC2 = 32 MHz

5. Now the positioning of horizontal blanking and the picture frame generator can be done.

2.3.4. Vertical Synchronization

The number of lines per field can be adjusted by software (LPFD). This number is used to calculate the vertical raster. The DDP synchronizes only to a vertical sync within a programmable detection window (LPFD $\pm$ VSYNCWIN). If there is no vsync the DDP runs with maximum allowed lines and if the vertical frequency is to high it runs with minimum allowed lines. The smaller the detection window the slower the DDP gets synchronized to the incoming vertical sync. In case of an interlaced input signal it is possible to display both fields at the same raster position by setting R_MODE to 1 or 2.

An automatic field length adaptation can be selected (VA_MODE). In this case the vertical raster will be calculated according to the counted number of lines per field instead from LPFD. This is useful for video recorder search mode when the number of lines per field does not comply with the standard, or if you want to use a common value of LPFD for PAL and NTSC (e.g.: LPFD = 290; VSYNCWIN = 54).

2.3.5. Vertical and East/West Deflection

The calculations of the Vertical deflection and East/West correction waveforms are done in the internal processor. They are described as polynomials in x, where x varies from –0.5•zoom to +0.5•zoom for one field. For zoom>1, the range is limited between –0.5 and +0.5.

The vertical deflection waveform is calculated as follows (without EHT compensation):

$$V = vpos + ampl(x + lin(x^2 - offset) + scor \cdot x(x^2 - offset))$$

– VPOS defines the vertical raster position
– AMPL is the vertical raster amplitude (zoom ≥ 1)
– LIN is the linearity coefficient
– SCOR is the coefficient for S-correction
– OFFSET is an internal parameter

The vertical sawtooth signal will be generated from a differential current D/A converter and can drive a DC coupled power stage. In order to get a faster vertical retrace timing, the output current of the vertical D/A-converter can be increased during the retrace for a programmable number of lines (FLYBL). The range between the end of the flyback and the beginning of the raster is also programmable (HOLDL).

The East/West deflection waveform, generated from a single ended D/A converter, is given with the equation:

$$E/W = width + trapez \cdot x + cush \cdot x^2 + corner \cdot x^4$$

– WIDTH is a DC value for the picture width
– TRAPEZ is the trapezoidal correction
– CUSH is the pincushion correction
– CORNU is the upper corner correction
– CORNL is the lower corner correction

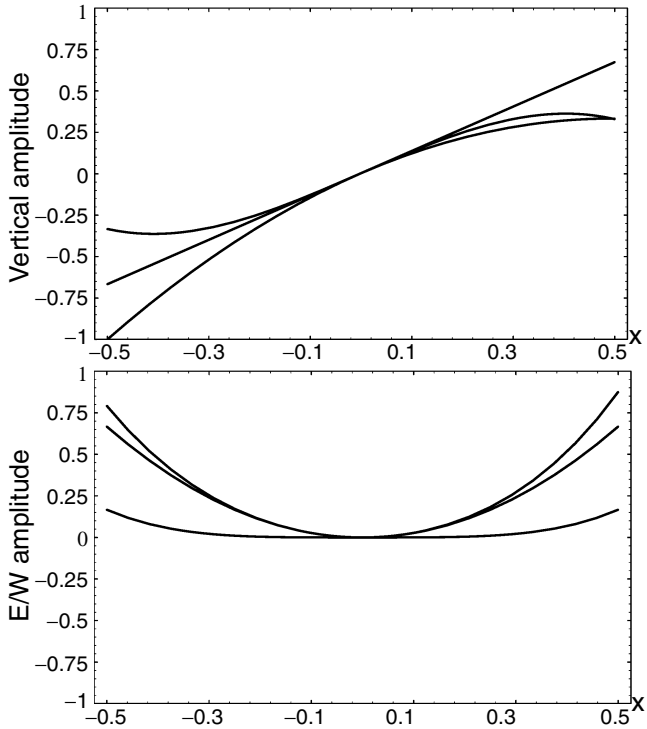


Fig. 2–16: Vertical and East/West deflection waveforms

2.3.6. Vertical Zoom

With vertical zoom the DDP 3315C is able to display different aspect ratios of the source signal on tubes with 4:3 or 16:9 aspect ratio by adapting the corresponding raster.

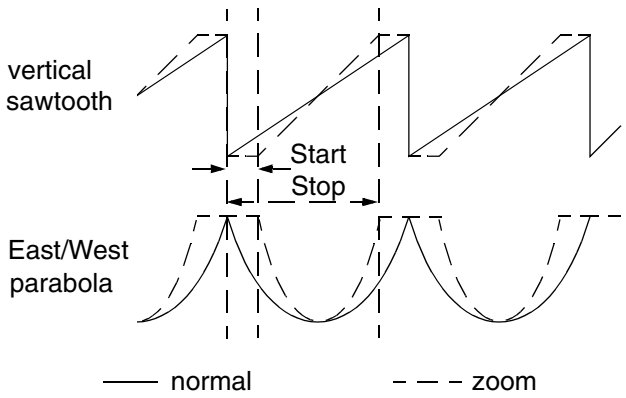


Fig. 2–17: Vertical zoom

2.3.7. EHT Compensation

The vertical deflection waveform can be scaled according the average beam current. This is used to compensate the effects of electric high tension changes due to beam current variations. EHT compensation for East/West deflection is done with an offset corresponding to the average beam current. The time constant of this process is free programmable with a resolution of 18 bit. Both corrections can be enabled separately. The maximum scaling coefficient for vertical deflection is 1±x and the maximum offset for east/west is y, where x, y are adjustable from 0 to 0.25. The horizontal phase at the output HOUT can be influenced according to the average beam current in a range of ±1.5 µs.

2.3.8. Protection Circuitry

Picture tube and drive stage protection is provided through the following measurements:

– Vertical protection input: this pin watches the vertical sawtooth signal. In every field the sawtooth must descend below the lower threshold A and ascend above the upper threshold B. In this case the protection flag is set (sawtooth o.k.). If an error occurs the protection flag is cleared.
After a programmable number of fields with cleared flag the RGB drive signals are blanked. The blanking is cancelled if the flag is set a programmable number of lines (see Fig. 2–18)

– Drive shutoff during flyback: this feature can be selected by software (EFLB)

– Safety input pin: this pin has two thresholds. The lower threshold A watches for a positive edge in every line, and the upper threshold B must not be overshoot, otherwise the RGB signals are blanked and a soft stop can be performed (HPROT_SS). Both thresholds have a small hysteresis.

2.3.9. Display Frequency Doubling

The DDP 3315C handles single or double vertical and horizontal input frequencies. The display frequency doubling is used when single H/V frequencies are applied and an external FIFO for scan rate conversion is used. In this mode it is mandatory to supply an active video signal to the HS pin, which is not vertical blanked.

Three different raster modes are selectable via I2C bus:

A A‘ B‘ B (normal operation)
A A B B (improved vertical resolution)
A A B‘ B‘ (non interlaced)

A/B means field A/B in original raster position and A‘/B‘ means field A/B in the opposite raster position.

A minimum field length filter can be switched on (DFD-FILT) to write only the smallest field length of the past up to four fields into the memory. This prevents read before write errors in signals with a strong changing field length (e.g. VCR signals).

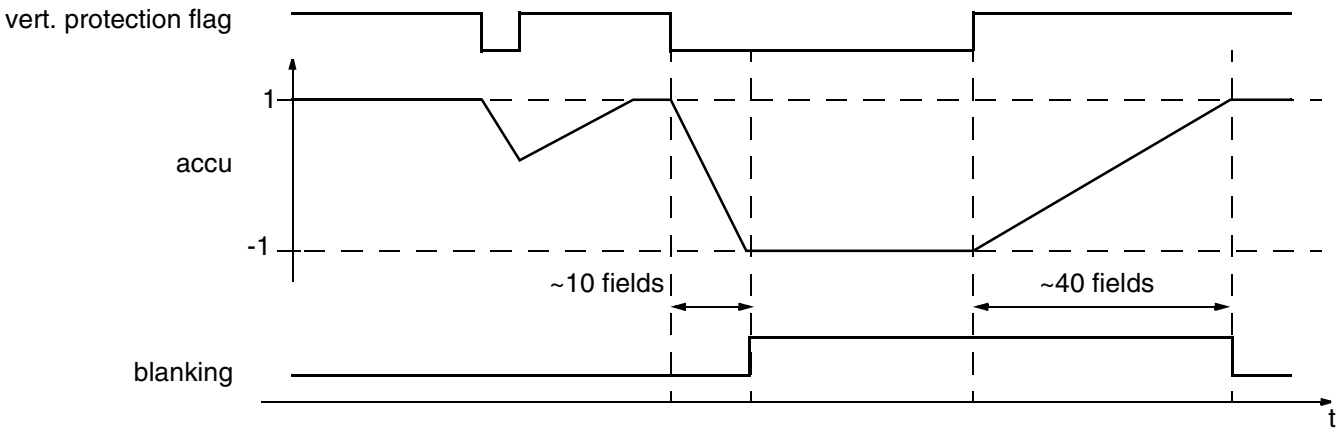


Fig. 2–18: Vertical protection timing

2.3.10. General Purpose D/A Converter

There are two D/A converters using pulse width modulation. The resolution is 8 bit and the clock frequency is 20.25 MHz. The outputs are push pull types. For a ripple-free output voltage a first order lowpass filter with a corner frequency < 120 Hz should be applied.

The D/A converters are adjusted via the I^2C bus. They can be used to generate two DC voltages, for example for horizontal raster position, raster tilt or just as switching outputs, when the values 0 and 255 are selected.

2.3.11. Clock and Reset

The DDP 3315C supports 27, 32, 40.5 and 54 MHz line-locked clock rates. This external clock rate is converted internally to a clock rate of 40.5 or 40 MHz by means of a PLL. Selection of external clock frequency is done with Pins CM1 and CM0. See Table 2–7 for clock frequency selection. To ensure lock of PLL a reset pulse of at least 500 µs must be applied after power up.

Table 2–7: Clock frequency selection

656EN	CM1	CM0	LLC2
0	0	0	27 MHz
0	0	1	32 MHz
0	1	0	40.5 MHz
1	0	0	54 MHz

2.3.12. Reset and Power-On

The IC provides an internal voltage supervision to generate an internal reset during power on or when the supply voltage goes below a certain level (V_{STBY} and V_{SUPD} < 2.75 V and/or V_{SUPO} < 4.2 V). Also a clock supervision of the 5 MHz clock keeps the internal reset active until proper clock signal is detected (e.g three clock cycles with the correct period). When the reset Pin RESQ or the internal reset becomes active all counters and registers are set to zero. When the reset pin is released, the internal reset is still active for approximately 4 µs. Then all registers are loaded with their default values listed in Table 3–5 on page 29. This initialization takes about 100 µs.

The HOUT signal becomes high with the VSTBY supply after power-on, regardless of RESQ, VSUPP/D, and VSUPO. When a proper 5 MHz clock is established (e.g. 8 ms after VSTBY is powered up), HOUT outputs a 55 kHz pulse. This state remains until an I^2C command starts the self-start procedure (RAMP_EN = 1).

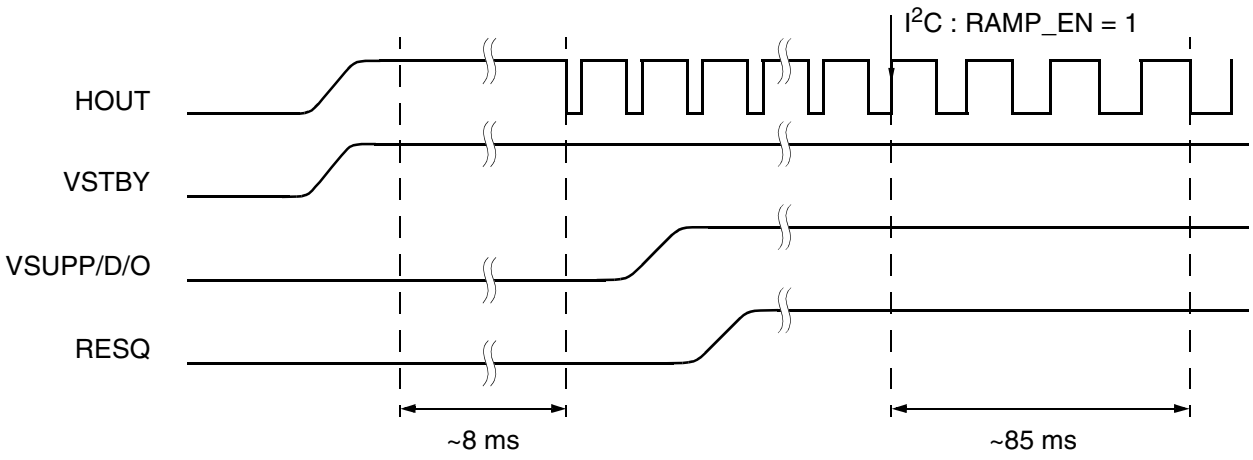


Fig. 2–19: Reset timing

3. Serial Interface

3.1. I²C-Bus Interface

Communication between the DDP 3315C and the external controller is done via I²C-bus. The DDP 3315C has an I²C-bus slave interface and uses I²C clock synchronization to slow down the interface if required.

Basically there are two classes of registers in the DDP 3315C.

The first class are directly addressable I²C registers. They are embedded in the hardware. These registers are 8 or 16 bits wide.

The second class are “XDFP-REGISTERS”, which are used by the “XDFP” onchip controller. These registers are all 16 bits wide and support read/write operation. Communication with these registers requires I²C packets with a 16 bit XDFP-register address and 16 bit data.

Communication with both classes of registers (I²C and XDFP-REGISTERS) are performed via I²C. The format of the I²C telegram depends on which type of register is being accessed.

The I²C-bus chip address of the DDP 3315C is given below:
Note: The I²C address is subject to change.

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	0	1	1/0

3.2. I²C Control and Status Registers

The I²C-bus interface uses one level of subaddress. First the bus address selects the IC, then a subaddress selects one of the internal registers. They have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words. Writing is done by sending the device address first followed by the subaddress byte and one or two data bytes. For reading, the read address has to be transmitted first by sending the device write address followed by the subaddress a second start condition with the device read address and reading one or two bytes of data. Fig. 3–2 shows I2C protocol for read and write operations; the read operation requires an extra start condition and repetition of the chip address with read command set. Table 3–2 gives definitions of the I²C control and status registers.

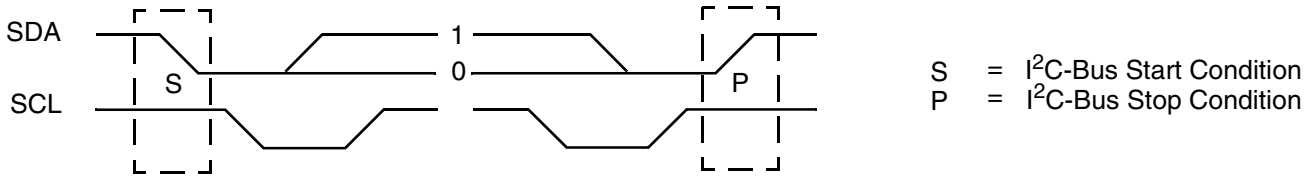


Fig. 3–1: I²C-Bus protocol (MSB first, data must be stable while clock is high)

Write to I²C control register :

S	1000 101	W	Ack	sub-addr.	Ack	1 or 2 byte data	Ack	P

Read from I²C control register :

S	1000 101	W	Ack	sub-addr.	Ack	S	1000 101	R	Ack	high byte data	Ack	low byte data	Nak	P

W = 0 (Write bit)
R = 1 (Read bit)

S = Start condition
P = Stop condition

Ack = 0 (Acknowledge bit from DDP = grey or Controller = hatched)
Nak = 1 (Not acknowledge bit from Controller = hatched or indicating an error state from DDP = grey)

Fig. 3–2: I²C-Bus protocol

Table 3–1: I²C Register List in Numerical Order

Ref. Addr. (hex)	Mode	Register Name	Updated
10	8–r/w	PSTR	immediately
11	16–w	PFC	immediately
12	16–w	dfpwr	immediately
13	16–w	dfprd	immediately
14	8–r/w	LUTCTRL	immediately
15	8–r/w	PSTRV	immediately
16	16–w	MINHY	immediately
17	16–w	ATVTY	immediately
18	8–w	MCRTL	immediately
1E	8–r	FBLSTAT	immediately
9F	16–r	HW_VER	immediately

Table 3–2: I²C Control and Status Registers in Functional Order

Ref. Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Hardware Version						
9F				hardware version number		HW_VER
	bit[3:0]			minor version number	1	HWVER_MIN
	bit[7:4]			major version number	2	HWVER_MAJ
	bit[15:8]			not used		
XDFP Interface						
12				XDFP write address		
	bit[9:0]	0	511	10-bit XDFP RAM address	0	DFPWR
	bit[15:10]		0	reserved, set to "0"		
13				XDFP read address		
	bit[9:0]	0	511	10-bit XDFP RAM address	0	DFPRD
	bit[15:10]		0	reserved, set to "0"		

Table 3–2: I²C Control and Status Registers in Functional Order, continued

Ref. Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Black Level Expander						
17				BLE activity control		ATVTY
	bit[3:0]	0	15	BLE tilt point	7	TILT
	bit[5:4]	0	3 0 3	BLE gain maximum gain minimum gain	1	BLEGAIN
	bit[8:6]	0	7	10 IRE black offset level (NTSC)	3	IRE10
	bit[11:9]	0		reserved, set to “0”	0	
	bit[14:12]	0	7	noise margin for the activity measurement	1	AMPLTHR
	bit[15]	0		reserved, set to "0"		
18				BLE mode control		MCRTL
	bit[1:0]	0	3 0 1 2 3	BLE mode 0: BLE off 1: autocontrast mode 2: dynamic mode 3: static mode	2	BLEMODE
	bit[4:2]	0	7	static BLE break point	3	SBLE
	bit[7:5]	0		reserved, set to "0"		
Non-linear Colorspace Enhancer (NCE)						
14				NCE configuration register		LUTCTRL
	bit[1:0]		 0 1 2 3	input segment resolution 32 bits per step input range: 0..1023 16 bits per step input range: 0..511 8 bits per step input range: 0..255 4 bits per step input range: 0..127	0	XSEG
	bit[2]	0	1	enables/disables LSB correction	0	LSBCORDIS
	bit[3]	0	1	enables/disables rounding always	0	APWMDIS
	bit[4]	0	1	y range extension bit	0	YEX
	bit[5]	0	1	bypass	1	NLBY
	bit[7:6]			reserved, set to "0"	0	
Picture Frame Generator						
11				picture frame color, 12-bit wide		PFC
	bit[3:0]	0	15	blue amplitude	0	PFCB
	bit[7:4]	0	15	green amplitude	0	PFCG
	bit[11:8]	0	15	red amplitude	0	PFCR
	bit[15:12]	0		reserved, set to "0"		

Table 3–2: I^2C Control and Status Registers in Functional Order, continued

Ref. Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Analog Fast Blank Monitor						
1E				fast blank signal status		FBLSTAT
	bit[0]	0	1	FBLIN level low/high		FBLEV
	bit[1]	0	1	FBLIN slope		FBSLO
	bit[7:2]	0		reserved, set to "0"		
Output Pins						
10				output pin configuration		PSTR
	bit[1:0]		 0 1 2 3	pin driver strength, FIFO control maximum strength (7) medium strength (5) minimum strength (3) tristated	0	PSTSY
	bit[2]	0	1	strong/weak (7/3) driver strength PWM1	0	PSTPW1
	bit[3]	0	1	strong/weak (7/3) driver strength PWM2	0	PSTPW2
	bit[4]	0	1	strong/weak (7/3) driver strength PWMV	0	PSTPV2
	bit[5]	0	1	disable/enable PWM output for EW Pin	0	EWPWM
	bit[6]	0	1	high/low active horizontal flyback input	0	FLYPOL
	bit[7]	0	1	strong/weak (7/3) driver strength DFVBL	0	PSTDF
15				output pin configuration		PSTRV
	bit[1:0]	0	3 0 3	pin driver strength for EW maximum strength (7) minimum strength (4)	0	PSTEW
	bit[3:2]	0	3 0 3	pin driver strength for H-/V-SYNC maximum strength (7) minimum strength (4)	0	PSTHVS
	bit[7:4]	0		reserved, set to "0"	0	

3.3. XDFP Control and Status Registers

The second class are “XDFP-REGISTERS”, which are used by the XDFP onchip controller. Access to these registers is achieved by subaddressing. Writing to these registers is done by sending the device write address first, followed by the XDFP-write subaddress, two address bits for the desired XDFP-register and the two data bytes. For reading, the XDFP-register address has to be transmitted first by sending the device write address, followed by the XDFP-read subaddress and the two XDFP-register address bytes. Without sending a stop condition, reading of the addressed data is done by sending the device read address and reading two bytes of data. Fig. 3–3 shows I2C protocol for read and write operations.Table 3–5 on page 29 gives definitions of the XDFP control and status registers. If these registers are smaller than 16 bit the remaining bits should be 0 on write and read operations. Due to the internal architecture, the IC cannot react immediately to an I^2C requests, which interacts with the onchip controller. The maximum response timing is appr. 20 ms. If the addressed controller is not ready for further transmissions on the I^2C-bus, the clock line SCL is pulled low. This puts the current transmission into a wait state. After a certain period of time the clock line will be released and the interrupted transmission is carried on.

Table 3–3: XDFP read/write address

XDFP Read address	h’13
XDFP Write address	h’12

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 3–5 on page 29.

The register modes are

8/16- bit width
r read only register
w write only register
r/w write/read data register

Note: set unused bits to ‘0‘!

The mnemonics used in the Micronas demo software are given in the last column.

Write to XDFP control register:

S	1000101	W	Ack	XDFP-writeaddr.	Ack	highbyte addr.	Ack	lowbyte addr.	Ack	highbyte data	Ack	lowbyte data	Ack	P

Read from XDFP control register:

S	1000101	W	Ack	XDFP-readaddr.	Ack	highbyte addr.	Ack	lowbyte addr.	Ack	S	1000101	R	Ack	highbyte data	Ack	lowbyte data	Nak	P

W = 0 (Write bit)
R = 1 (Read bit)

S = Start condition
P = Stop condition

Ack = 0 (Acknowledge bit from DDP = grey or Controller = hatched)
Nak = 1 (Not acknowledge bit from Controller = hatched or indicating an error state from DDP = grey)

Fig. 3–3: XDFP protocol

Table 3–4: XDFP Register List in Numerical Order

Ref. Addr. (hex)	Mode	Register Name	Updated
20	16–r	VER	immediately
59	16–r/w	BC	immediately
6B	16–r/w	CUTOFF_R	vertical
6C	16–r/w	CUTOFF_G	vertical
6D	16–r/w	CUTOFF_B	vertical
6E	16–r/w	WDRIVE_R	vertical
6F	16–r/w	WDRIVE_G	vertical
70	16–r/w	WDRIVE_B	vertical
116	16–r/w	AMCTRL	vertical
117	16–r/w	RCTRL0	vertical
11F	16–r/w	GCTRL0	vertical
127	16–r/w	BCTRL0	vertical
131	16–r/w	SCMODE	vertical
132	16–r/w	FFLIM	vertical
133	16–r/w	SCINC1	vertical
134	16–r/w	SCINC2	vertical
135	16–r/w	SCINC	vertical
136	16–r/w	SCW1_1	vertical
137	16–r/w	SCW1_2	vertical
138	16–r/w	SCW1_3	vertical
139	16–r/w	SCW1_4	vertical
13A	16–r/w	SCW1_5	vertical
13B	16–r/w	SCW2_1	vertical
13C	16–r/w	SCW2_2	vertical
13D	16–r/w	SCW2_3	vertical
13E	16–r/w	SCW2_4	vertical
13F	16–r/w	SCW2_5	vertical
14A	16–r/w	LTI	vertical
14B	16–r/w	SFIF	vertical
14E	16–r/w	LTIMIX1	vertical
14F	16–r/w	BCT	vertical
152	16–r/w	LTIMIX2	vertical
153	16–r/w	GCT	vertical

Table 3–4: XDFP Register List in Numerical Order

Ref. Addr. (hex)	Mode	Register Name	Updated
154	16–r/w	PFG	vertical
157	16–r/w	RCT	vertical
158	16–r/w	PBFB1	vertical
15A	16–r/w	BRM	vertical
15B	16–r/w	SVM2	vertical
15C	16–r/w	TML	vertical
15F	16–r/w	SVLIM	vertical
160	16–r/w	vbso	vertical
164	16–r/w	vbst	vertical
167	16–r/w	SVM1	vertical
168	16–r/w	PFGVE	vertical
16A	16–r/w	PK1	vertical
16B	16–r/w	DTICTRL	vertical
16C	16–r/w	PFGVB	vertical
16E	16–r/w	PK2	vertical
16F	16–r/w	CRCTRL	vertical
170	16–r/w	INFMT	vertical
171	16–r/w	HDRV	vertical
172	16–r/w	NEWLIN	vertical
173	16–r/w	HBST	vertical
174	16–r/w	HBSO	vertical
175	16–r/w	PFGHB	vertical
176	16–r/w	PFGHE	vertical
178	16–r/w	DFHB	vertical
179	16–r/w	DFHE	vertical
17B	16–r/w	PWM2	vertical
17C	16–r/w	PWM1	vertical
17D	16–r/w	DFDCTRL	vertical
17E	16–r/w	PWMV	vertical
17E	16–r/w	PWMV	vertical
180	16–r/w	HCTRL	vertical
181	16–r/w	POFS2	horizontal
182	16–r/w	POFS3	horizontal

Table 3–4: XDFP Register List in Numerical Order

Ref. Addr. (hex)	Mode	Register Name	Updated
183	16–r/w	PKP2	horizontal
185	16–r/w	PKP3	horizontal
187	16–r/w	ANGLE	horizontal
188	16–r/w	BOW	horizontal
18F	16–r/w	CENTER	vertical
190	16–r/w	AMPL	vertical
191	16–r/w	ZOOM	vertical
192	16–r/w	VPOS	vertical
193	16–r/w	LIN	vertical
194	16–r/w	SCORR	vertical
195	16–r/w	VSYNWIN	vertical
196	16–r/w	LPFD	vertical
197	16–r/w	HOLDL	vertical
198	16–r/w	FLYBL	vertical
19A	16–r/w	WIDTH	vertical
19B	16–r/w	TCORR	vertical
19C	16–r/w	CUSH	vertical
19D	16–r/w	CRNU	vertical
19E	16–r/w	CRNL	vertical
19F	16–r/w	CRNUS	vertical
1A0	16–r/w	CRNLS	vertical
1A6	16–r/w	SATM	vertical
1A7	16–r/w	CTM	vertical
1A8	16–r/w	MB2M	vertical
1A9	16–r/w	MB1M	vertical
1AA	16–r/w	MG2M	vertical
1AB	16–r/w	MG1M	vertical
1AC	16–r/w	MR2M	vertical
1AD	16–r/w	MR1M	vertical
1AF	16–r/w	EHT_THRES	horizontal
1B0	16–r/w	EHT_STC	horizontal
1B1	16–r/w	EHTV_SA1	horizontal
1B2	16–r/w	EHTV_SA2	horizontal

Table 3–4: XDFP Register List in Numerical Order

Ref. Addr. (hex)	Mode	Register Name	Updated
1B3	16–r/w	EHTH_SA1	horizontal
1B4	16–r/w	EHTH_SA2	horizontal
1C0	16–r/w	IBRM	vertical
1C1	16–r/w	MADCLAT	vertical
1C2	16–r/w	MCTRL	vertical
1C3	16–r/w	CUT_R	vertical
1C4	16–r/w	CUT_G	vertical
1C5	16–r/w	CUT_B	vertical
1C6	16–r/w	CUT_GAIN	vertical
1C8	16–r/w	WDR_R	vertical
1C9	16–r/w	WDR_G	vertical
1CA	16–r/w	WDR_B	vertical
1CB	16–r/w	MAX_WDR	vertical
1CF	16–r/w	BCL_BRED	immediately
1D0	16–r/w	BCL_GAIN	immediately
1D1	16–r/w	BCL_THRES	immediately
1D2	16–r/w	BCL_TC	immediately
1D3	16–r/w	BCL_TCUP	immediately
1D4	16–r/w	BCL_MIN_C	immediately
1D5	16–r/w	BCL_MIN_B	immediately
1D6	16–r/w	BC_MIN	immediately
1D7	16–r/w	BC_MAX	immediately
1DB	16–r/w	EXT_CONTR	vertical
1DC	16–r/w	EXT_BRT	vertical
1DD	16–r/w	INT_BRT	vertical
1DF	16–r/w	FBLMODE	vertical
1E2	16–r/w	VS_MODE	vertical
1E3	16–r/w	R_MODE	vertical
1E8	16–r/w	VA_MODE	vertical
1E9	16–r/w	WDR_SAT	vertical
1EA	16–r/w	HPROT_SS	vertical
1EA	16–r/w	HSTOP	vertical
1EB	16–r/w	BSO_EN	vertical

Table 3–5: XDFP Control and Status Registers in Functional Order

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
XDFP Status Register						
20				firmware version number		VER
	bit[7:0]			firmware release	0x21	FW_REL
Input Formatter						
170				input format		INFMT
	bit[0]	0	1	0/1 4:2:2/4:1:1 mode	1	M411
	bit[1]	0	1	0/1 binary offset/2‘s complement	1	COB
	bit[2]	0	1	0/1 enable/disable blanking to black (for luma and chroma input when HS = 0)	1	BLNK
	bit[4:3]	0	3	select color multiplex	0	CMUX
	bit[5]	0	1	use HS, VS/VS2 pin instead of embedded 656 sync	0	EXTSYNC
	bit[6]	0	1	invert field ID flag	0	INVFIELD
Scaler Control Register						
131				scaler mode register	0	SCMODE
	bit[1:0]		 0 1 2 3	scaler mode linear scaling mode nonlinear scaling mode, ’panorama’ nonlinear scaling mode, ’waterglass’ reserved		PANO
	bit[13:2]			reserved, set to "0"		
	bit[14]	0	1	0 scaler update command, set to "1" to update only scaler mode register		SCMODUP
	bit[15]	0	1	0 scaler update command, set to "1" to update all scaler control registers		SCUPDATE
132	bit[11:0]	0	1295	active video length for 1–h FIFO, length in pixels 720 LLC mode (864/h)	720	FFLIM
133	bit[11:0]	1024	4095	scaler 1 coefficient, this scaler compresses the signal, compression by a factor "c", the value c*1024 is required	1024	SCINC1
134	bit[11:0]	256	1024	scaler 2 coefficient, this scaler expands the signal, expansion by a factor "c", the value 1/c*1024 is required	682	SCINC2
135	bit[11:0]	0	4095	scaler1/2 nonlinear scaling coefficient	0	SCINC
136	bit[11:0]	0	4095	scaler 1 window register for control of nonlinear scaling	0	SCW1_1
137	bit[11:0]	0	4095	scaler 1 window register for control of nonlinear scaling	0	SCW1_2
138	bit[11:0]	0	4095	scaler 1 window register for control of nonlinear scaling	0	SCW1_3
139	bit[11:0]	0	4095	scaler 1 window register for control of nonlinear scaling	0	SCW1_4
13A	bit[11:0]	0	4095	scaler 1 window register for control of nonlinear scaling	0	SCW1_5
13B	bit[11:0]	0	4095	scaler 2 window register for control of nonlinear scaling	0	SCW2_1
13C	bit[11:0]	0	4095	scaler 2 window register for control of nonlinear scaling	1	SCW2_2
13D	bit[11:0]	0	4095	scaler 2 window register for control of nonlinear scaling	2	SCW2_3

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
13E	bit[11:0]	0	4095	scaler 2 window register for control of nonlinear scaling	3	SCW2_4
13F	bit[11:0]	0	4095	scaler 2 window register for control of nonlinear scaling	4	SCW2_5
Luma Channel						
14A				LTI control		LTI
	bit[3:0]	0	15	LTI gain	4	LTIGAIN
	bit[6:4]	0	7	LTI coring	1	LTICOR
	bit[7]	0	1	peaking/LTI enable	1	LTIEN
14E				LTI mixer control 1		LTIMIX1
	bit[0]	0	1	LTI mode	0	LTIMODE
	bit[5:1]	0	31	amplitude offset to start ampl. adaptive mixing (1 step corresponds to 32 amplitude levels) 0...31 no ...max. offset	6	MIXOFFSET
	bit[7:6]	0	3	velocity of mixing 0: fast 3: slow	3	MIXGAIN
	bit[8]	0	1	amplitude adaptive/static mixing	0	MIXMODE
152				LTI mixer control 2		LTIMIX2
	bit[5:0]	0	63	static mixer coefficient 0: 100% peaking 63: 100% LTI	0	MIXCOEFF
	bit[8:6]	0		reserved, set to "0"	0	
15A	bit[8:0]	–256	255	luma DC-offset	0	BRM
16A				luma peaking filter, the gain at high frequencies and small signal amplitudes is 1 + (k1+k2)/8		PK1
	bit[3:0]	0	15	k1: peaking level undershoot	4	PKUN
	bit[7:4]	0	15	k2: peaking level overshoot	4	PKOV
	bit[8]	0	1	peaking value normal/inverted (peaking/softening)	0	PKINV
16E	bit[2:0]			luma peaking filter, coring		PK2
	bit[4:0]	0	31	coring level	3	COR
	bit[7:5]	 000 001 01X 100 101 11X		peaking reduction 100% 80% 60% 50% 40% 30%	0	PKRD
	bit[8]	0	1	peaking filter center frequency high/low	0	PFS

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Chroma Channel						
16B				digital transient improvement		DTICTRL
	bit[3:0]	0	15	coring value	1	DTICO
	bit[7:4]	0	15	DTI gain	5	DTIGA
	bit[8]	0	1	narrow/wide bandwidth mode	1	DTIMO
16F				luma/chroma matching delay		CRCTRL
	bit[2:0]	–2	2	variable chroma delay	0	CDEL
	bit[3]	0		reserved, set to "0"	0	
	bit[4]	0	1	CB (U) sample first / CR (V) sample first	0	ENVU
	bit[5]	0		reserved, set to "0"		
Inverse Matrix						
1A6	bit[14:9]	0	63	picture saturation in steps of 1/32	32	SATM
				picture matrix coefficient B–Y = MB1M/64*CB + MB2M/64*CR		
1A8	bit[15:7]	–64	63		0	MB2M
1A9	bit[15:7]	0	127		113	MB1M
				picture matrix coefficient G–Y = MG1M/64*CB + MG2M/64*CR		
1AA	bit[15:7]	–64	63		–44	MG2M
1AB	bit[15:7]	–64	63		–22	MG1M
				picture matrix coefficient R–Y = MR1M/64*CB + MR2M/64*CR		
1AC	bit[15:7]	0	127		86	MR2M
1AD	bit[15:7]	–64	63		0	MR1M
Non-Linear Color-Space Enhancer						
117 - 11E	bit[8:0]	–256	255	difference between Y-coordinate of the current basepoint and the linear characteristic	0	RDY0 - RDY7
	bit[9]	0		reserved, set to “0”	0	
	bit[14:10]	0	31	X-coordinate of segment basepoint	0	RX0 - RX7
	bit[15]	0		reserved, set to “0”	0	
11F - 126	bit[8:0]	–256	255	difference between Y-coordinate of the current basepoint and the linear characteristic	0	GDY0 - GDY7
	bit[9]	0		reserved, set to “0”	0	
	bit[14:10]	0	31	X-coordinate of segment basepoint	0	GX0 - GX7
	bit[15]	0		reserved, set to”0”	0	

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
127 - 12E	bit[8:0]	–256	255	difference between Y-coordinate of the current basepoint and the linear characteristic	0	BDY0 - BDY7
	bit[9]	0		reserved, set to “0”	0	
	bit[14:10]	0	31	X-coordinate of segment basepoint	0	BX0 - BX7
	bit[15]	0		reserved, set to “0”	0	
Picture Frame Generator						
14F	bit[3:0]	0		reserved, set to "0"	0	
	bit[7:4]	0	13 14,15	picture frame contrast B B amplitude = PFCB · (PFBCT + 4) invalid	8	PFBCT
153	bit[3:0]	0		reserved, set to "0"	0	
	bit[7:4]	0	13 14,15	picture frame contrast G G amplitude = PFCG · (PFGCT + 4) invalid	8	PFGCT
154	bit[2:0]	0	7	picture frame generator priority id	7	PFGID
	bit[8]	0	1	enable prio id for picture frame generator	0	PFGEN
157	bit[3:0]	0		reserved, set to "0"	0	
	bit[7:4]	0	13 14,15	picture frame contrast B R amplitude = PFCR · (PFRCT + 4) invalid	8	PFRCT
158	bit[7:0]	0	1	disable/enable analog fast blank input1/2 if bit[x] is set to "1", then the function is active for the respective signal priority	0	PBFB1
168	bit[8:0]	0	511	vertical picture frame end line	57	PFGVE
16C	bit[8:0]	1	511 0	vertical picture frame start line (+128) vertically disabled	0	PFGVB
175	bit[10:0]	0	1295 0 h'7FF	horizontal picture frame begin (see table for max. pixels per line) horizontally disabled full frame	280	PFGHB
176	bit[10:0]	0	1295	horizontal picture frame end (see table for max. pixels per line)	137	PFGHE

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Brightness and Contrast						
1A7	bit[14:9]	0	63	picture contrast in steps of 1/32	32	CTM
1DB	bit[14:6]	0	511	analog contrast for external RGB	360	EXT_CONTR
1DC	bit[15:6]	–256	255	analog brightness for external RGB The range allows for both increase and reduction of brightness.	128	EXT_BRT
1DD	bit[15:6]	–256	255	internal analog brightness The range allows for both increase and reduction of brightness.	24	INT_BRT
Scan Velocity Modulation						
15B	bit[3:0]	0	15	delay of SVMOUT in steps of 12.5 ns (SVMOUT vs. RGBOUT is 60 ns @7)	7	SVDEL
	bit[7:4]	0	15	coring value	0	SVCOR
	bit[8]	0		reserved, set to"0"		
15F	bit[7:0]	0	255	limit value	100	SVLIM
	bit[8]	0		reserved, set to"0"	0	
167				video mode coefficients		SVM1
	bit[5:0]	0	63	gain	60	SVG
	bit[8:6]	0	6	differentiator delay (0 = filter off)	1	SVD
Beam Current Limiter (BCL)						
59	bit[14:3]	0	4095	beam current, latched every line except during vertical blanking	0	BC
1CF	bit[11:4]	0	255	brightness reduction depending on measured BC	0	BCL_BRED
1D0	bit[14:6]	0	511	BCL loopgain	0	BCL_GAIN
1D1	bit[15:3]	0	4095 -4096	BCL threshold current if sense input used if RSW1 input used	0	BCL_THRES
1D2	bit[8:0]	 1	 0 511	BCL time constant: BCL off 800 ms...0.025 ms	0	BCL_TC
1D3	bit[8:0]	1	511 0	second BCL time constant for increasing contrast take BCL_TC instead	0	BCL_TCUP
1D4	bit[14:6]	0	511	BCL minimum contrast (= 0..max contrast)	0	BCL_MIN_C
1D5	bit[14:6]	0	511	BCL minimum brightness (= 0..max bright.)	0	BCL_MIN_B
1D6	bit[14:3]	0	4095	minimum beam current (reset every field)	0	BC_MIN
1D7	bit[14:3]	0	4095	maximum beam current (reset every field)	0	BC_MAX
1DB	bit[0]		0 1	beam current limitation reduces ext. RGB BCL does not reduce ext. RGB	0	NOOSDBCL

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Tube Measurement						
15C	bit[8:0]	0	511	tube measurement linestart line for tube measurement (+2 lines)	10	TML
1C1	bit[10:0]	0	1295	latch timing of madc data in pixels before the begin of horiz. blanking HBST	128	MADCLAT
1C2				measurement control word		MCTRL
	bit[8]	0	1	enable/disable ultra black blanking	0	ULBLK_DIS
	bit[9]	0 1	0 1	all outputs blanked (video mute) normal mode	0	BLANK_DIS
	bit[10]	0	1	broad/narrow measurement bandwidth	0	BW_SEL
	bit[13]	0	1	disable/enable horizontal blanking during measurement	0	MBLANK
	bit[14]	0	1	disable/enable RSW1 pin as input for beam current measurement	0	SMODE
Cutoff and Drive Measurement						
6B	bit[11:3]	0	511	latched cutoff Red	0	CUTOFF_R
6C	bit[11:3]	0	511	latched cutoff Green	0	CUTOFF_G
6D	bit[11:3]	0	511	latched cutoff Blue	0	CUTOFF_B
6E	bit[11:3]	0	511	latched White Drive Red	0	WDRIVE_R
6F	bit[11:3]	0	511	latched White Drive Green	0	WDRIVE_G
70	bit[11:3]	0	511	latched White Drive Blue	0	WDRIVE_B
146	bit[8:0]	0	511	RGB values for white drive beam current measurement	0	WDRM
1C0	bit[14:6]	0	511	internal brightness for measurement.	256	IBRM
1C2	bit[11]	0	1	enable/disable white drive measurement	0	WDR_DIS
1C2	bit[12]	0	1	enable/disable cutoff measurement	0	CUT_DIS
1C3	bit[12:4]	0	511	reference for cutoff Red	511	CUT_R
1C4	bit[12:4]	0	511	reference for cutoff Green	511	CUT_G
1C5	bit[12:4]	0	511	reference for cutoff Blue	511	CUT_B
1C6	bit[14:6]	 1	0 511	the reference values were taken directly as cutoff values; gain for cutoff control loop	0	CUT_GAIN
1C7	bit[14:6]	 1	0 511	the reference values were taken directly as white drive values gain for white drive control loop	0	WDR_GAIN
1C8	bit[12:4]	0	511	reference for White Drive Red	511	WDR_R
1C9	bit[12:4]	0	511	reference for White Drive Green	511	WDR_G
1CA	bit[12:4]	0	511	reference for White Drive Blue	511	WDR_B
1CB	bit[14:6]	475	511	threshold for automatic drive saturation avoidance	491	MAX_WDR
1E9	bit[0]	0	1	disable/enable automatic drive saturation avoidance	0	WDR_SAT

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Timing						
14B	bit[8:0]	0	511	start point of active video relative to incoming HS signal in steps of 2 LLC2 clocks; can be used e.g. for panning	0	SFIF
160				vertical blanking stop		
	bit[8:0]	0	511	last line of vertical blanking	22	VBSO
164				vertical blanking start		
	bit[8:0]	0	511	first line of vertical blanking (+ 128 offset)	182	VBST
172	bit[10:0]	0	1295	bit[10:0] 0..1295 start of the line in respect to the pixel counter 90 < (POFS2+NEWLIN)−(3/2xSFIF)< 580	330	NEWLIN
173	bit[10:0]	0	1295	horizontal blanking start	253	HBST
174	bit[10:0]	0	1295	horizontal blanking stop	331	HBSO
178	bit[10:0]	0	1295	start of dynamic focus pulse	0	DFHB
179	bit[10:0]	0	1295	stop of dynamic focus pulse	0	DFHE
	bit[12:11]		0 1 2 3	H-pulse vert. blanked H-pulse V-pulse not used	0	HDF
Horizontal Deflection						
171	bit[5:0]	20	35	horizontal drive pulse duration (high time)	30	HDRV
17D	bit[9]	0	1	high/low active HS input	0	HSYPOL
180				horizontal deflection control register		HCTRL
	bit[0]	0		reserved, set to "0"	0	
	bit[1]	0	1	enable/disable vertical protection	0	VPROT_DIS
	bit[2]	0	1	enable/disable h-safety protection	0	HPROT_DIS
	bit[3]	0	1	disable/enable drive high during flyback	0	EFLB
	bit[4]		1	start ramp up/down	0	RAMP_EN
	bit[7:5]		 000 001 010 100 110	horizontal frequency H-Freq pixels per line @LLC in kHz 27 MHz 32 MHz 31.25 864 1024 35.1 768 912 31.46 858 1024 33.8 800 944 37.9 712 844	0	HFREQ
181	bit[15:1]	−600	600	adjustable delay of PLL2, clamping, and blanking (relative to incoming hsync) adjust clamping pulse for analog RGB input; 1 step = 1 pixel clock	5	POFS2
182	bit[15:1]	−600	600	adjustable delay of flyback, H/VSYNC and analog RGB (relative to PLL2) adjust horizontal drive or H/VSYNC; 1 step = 1 pixel clock	0	POFS3
183	bit[14:6]	0	511	proportional coefficient PLL2, c*2^−9	184	PKP2
185	bit[14:6]	0	511	proportional coefficient PLL3, c*2^−9	102	PKP3

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
187	bit[15:6]	–512	511	vertical angle	0	ANGLE
188	bit[15:6]	–512	511	vertical bow	0	BOW
1EA	bit[0]	0	1	disable/enable soft stop if h-safety protection is active	0	HPROT_SS
	bit[1]	0	0 1	end of RAMP down is constant high end of RAMP down is a pulse	0	HSTOP
Vertical Modes						
1E2	bit[0]	0	1	VSYNC synchronized/free running	0	VS_MODE
1E3	bit[1:0]		 0 1 2 3	raster mode same input and output raster field 2 is delayed (only A raster is written) field 1 is delayed (only B raster is written) not used	0	R_MODE
1E8	bit[0]	0	1	automatic lines-per-field adaption (constant raster amplitude) off/on	0	VA_MODE
1EB	bit[0]	0	1	disable/enable black switch off procedure on h-safety failure	0	BSO_EN
Vertical Parameters						
17D	bit[8]	0 1		automatic VSYNC polarity detection force VS/VS2 input low active	0	VSYPOL
17D	bit[10]	0	1	VS/VS2 pin is source of VSYNC	0	VSYSRC
195	bit[6:0]	0	127	window (LPFD±VSYNWIN) for sync detection	32	VSYNWIN
196	bit[9:0]	0	1023	lines per field	312	LPFD
197	bit[9:0]	0	1023	number of hold lines	10	HOLDL
198	bit[9:0]	0	1023	number of flyback lines (flyback booster active)	5	FLYBL
Vertical Sawtooth Correction (%-values according to DAC range)						
190	bit[15:8]	–512	511	vertical amplitude (±25%)	0	AMPL
191	bit[14:6]	0	510	zoom (0...100...200%)	256	ZOOM
192	bit[15:8]	–512	511	vertical picture position (± 25%); (DC offset of sawtooth output). This offset is independent of EHT compensation.	0	VPOS
193	bit[15:8]	–512	511	linearity (±25%)	0	LIN
194	bit[15:8]	–512	511	S-correction (±20%)	0	SCORR

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Extreme High Tension (EHT) Compensation (%-values according to DAC range)						
1AF	bit[14:6]	0	2047	threshold for second coefficients of horizontal and vertical EHT compensation	2047	EHT_THRES
1B0	bit[14:6]	0 1	511	EHT static time constant for horizontal and vertical amplitude compensation off 800 .. 0.025 ms	0	EHT_STC
1B1	bit[15:6]	–512	511	first coefficient for static EHT compensation of vertical amplitude (±100%)	0	EHTV_SA1
1B2	bit[15:6]	–512	511	second coefficient for static EHT compensation of vertical amplitude (±100%)	0	EHTV_SA2
1B3	bit[15:6]	–512	511	first coefficient for static EHT compensation of horizontal amplitude (±100%)	0	EHTH_SA1
1B4	bit[15:6]	–512	511	second coefficient for static EHT compensation of horizontal amplitude (±100%)	0	EHTH_SA2
East-West Parabola (%-values according to DAC range)						
19A	bit[15:7]	–256	255	picture width (0...100%)	51	WIDTH
19B	bit[15:8]	–512	511	trapeze correction (±50%)	0	TCORR
19C	bit[15:8]	–512	511	cushion correction (±25%)	0	CUSH
19D	bit[15:8]	–512	511	upper corner correction (±6%)	0	CRNU
19E	bit[15:8]	–512	511	lower corner correction (±6%)	0	CRNL
19F	bit[15:8]	–512	511	upper corner correction 6th order (±6%)	0	CRNUS
1A0	bit[15:8]	–512	511	lower corner correction 6th order (±6%)	0	CRNLS
17E	bit[0]		0 1	use complete DAC range scale EW amplitude to linelength for PWM output	0	EWPWMSC

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
Display Frequency Doubling						
17D				display frequency doubling control word		DFDCTRL
	bit[1:0]			display raster mode (A' = field A in raster B)	0	DFDMODE
			0	A A' B' B		
			1	A A B B		
			2	A A B' B'		
			3	not used		
	bit[3:2]			minimum field length filter	0	DFDFILT
			0	off		
			1	2 fields		
			2	3 fields		
			3	4 fields		
	bit[5:4]			input sync doubling switch	0	DFDSW
			0	leave H and V sync unchanged		
			1	double VSYNC and leave HSYNC unchanged		
			2	double HSYNC and leave VSYNC unchanged		
			3	double H and V sync		
	bit[10:6]	0		reserved, set to "0"		
	bit[11]	0	1	dis-/enable still picture (only available if display frequency doubling is enabled)	0	STILL
	bit[12]	0	1	high/low active FIFO control signals	0	FIFOPOL
Analog RGB Insertion						
116				control signals for analog matrix		AMCTRL
	bit[5:0]	0		reserved, set to "0"	0	
	bit[8:6]	0	4	select YUV matrix	0	MATTYPE
			1	RGB		
			2	480P		
			4	1080I		
	bit[14:10]	0	31	saturation for analog RGB/YUV	0	ASAT
	bit[15]	0		reserved, set to "0"	0	

Table 3–5: XDFP Control and Status Registers in Functional Order, continued

Ref Addr. (hex)	Bit Slice	Min.	Max.	Function	Default	Register Name
1DF				fast blank interface mode		FBLMODE
	bit[0]		0 1	fast blank from FBLIN1 pin force internal fast blank signal to high	0	FBFOH1
	bit[1]	0	1	fast blank active high/low at FBLIN pin		FBPOL
	bit[2]		0 1	fast blank from FBLIN1 pin force internal fast blank signal to low	0	FBFOL1
	bit[3]		 0 1	fast blank priority FBLIN1>FBLIN2 FBLIN1<FBLIN2	0	FBPRIO
	bit[4]		0 1	fast blank from FBLIN2 pin force internal fast blank signal to low		FBFOL2
	bit[5]		0 1	fast blank from FBLIN2 pin force internal fast blank signal to high	0	FBFOH2
	bit[6]	0	1	fast blank monitor input select FBLIN1/2		FBMON
	bit[7]	0	1	disable/enable clamping for RGBIN1&2		CLAMP
	bit[8]	0	1	vertical blanking of clamp pulse	0	CLAMPVB
	bit[9]	0	1	half contrast signal active high/low at HCS pin		HCSPOL
	bit[10]	0	1	disable/enable half contrast switching	0	HCSEN
	bit[11]		0 1	half contrast signal from HCS pin force internal half contrast signal to high		HCSFOH
	bit[12]		0 1	half contrast level at –6 dB (= 50%) half contrast level at –10 dB (= 30%)	0	HCSLEVEL
	bit[15:13]	0		reserved, set to”0”		
I^2C Controlled 8-Bit PWM						
17B	bit[7:0]	0	255	PWM2 data word	0	PWM2
17C	bit[7:0]	0	255	PWM1 data word	0	PWM1
17E	bit[9:2]	0	255	PWMV data word/amplitude of parabola (if bit[1] is set)	0	PWMV
	bit[1]		0 1	use PWMV as static PWM output use PWMV as parabola output	0	PWMVEN

3.3.1. Scaler Adjustment

In case of linear scaling, most of the scaler registers need not to be set. Only the scaler mode, active video length, and the fixed scaler increments (SCINC1 / SCINC2) must be written.

The adjustment of the scaler for nonlinear scaling should use the parameters given in Table 3–6. An example for ‘panorama vision’ mode is depicted in Fig. 3–4. It shows the scaling of the input signal and the variation of the scaling factor during the active video line. The scaling factor starts below 1, i.e. for the borders the video data is expanded and after it exceeds 1 it is compressed. When the picture center is reached, the scaling factor is held constant. At the second border the scaling factor changes back symmetrically.

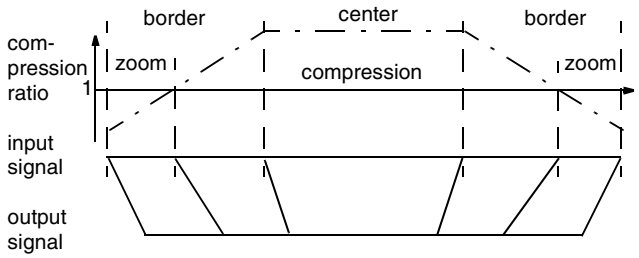


Fig. 3–4: Scaler operation for “panorama” mode

Table 3–6: Setup values for nonlinear scaler modes

Mode	27 MHz				32 MHz			
	‘waterglass’ border 35%		‘panorama’ border 30%		‘waterglass’ border 35%		‘panorama’ border 30%	
Register	center 3/4	center 5/6	center 4/3	center 6/5	center 3/4	center 5/6	center 4/3	center 6/5
SCINC1	1099	1064	1024	1024	1195	1122	1024	1024
SCINC2	1024	1024	259	407	1024	1024	305	489
SCINC	60	65	56	38	54	42	68	46
FFLIM	715	717	758	796	833	845	831	871
SCW1 – 0	20	10	106	106	51	37	109	126
SCW1 – 1	156	123	106	106	161	166	125	126
SCW1 – 2	202	236	273	292	256	257	291	310
SCW1 – 3	338	349	273	292	366	386	307	310
SCW1 – 4	358	359	379	398	417	423	416	436
SCW2 – 0	20	10	186	177	51	37	168	175
SCW2 – 1	156	123	186	177	161	166	184	175
SCW2 – 2	384	417	354	363	373	368	350	359
SCW2 – 3	520	530	354	363	483	497	366	359
SCW2 – 4	540	540	540	540	534	534	534	534

4. Specifications

4.1. Outline Dimensions

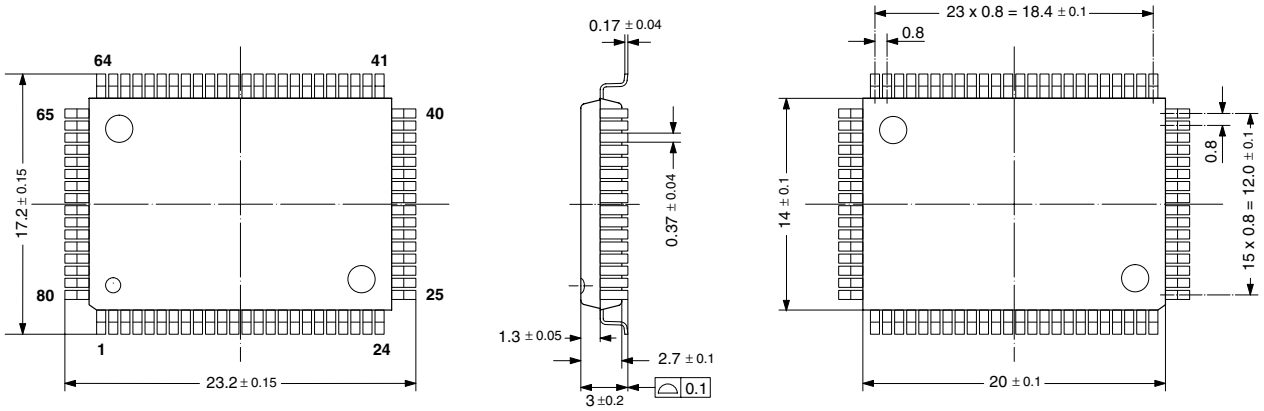


Fig. 4–1:
80-pin Plastic Quad Flat Package
(**PQFP80**)
Weight approximately 1.61 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
IN = input
OUT = output
SUPPLYA = analog supply pin
SUPPLYD = digital supply pin

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	Y6	IN	GNDD	Picture Bus Luma
2	Y7	IN	GNDD	Picture Bus Luma (MSB)
3	656EN	IN	X	Enable 656 input mode (LLC2 = 54 MHz)
4	LLC2	IN	X	System Clock Input
5	HS	IN	X	Horizontal Sync Input
6	VS	IN	GNDD	Vertical Sync Input
7	FREQSEL	IN	X	Selection of H-Drive Frequency Range
8	CM1	IN	X	Clock Select 1
9	CM0	IN	X	Clock Select 0
10	VS2	IN	GNDD	Additional VSYNC input
11	XTAL2	OUT	X	Analog Crystal Output (5-MHz Security Clock)

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
12	XTAL1	IN	X	Analog Crystal Input (5-MHz Security Clock)
13	NC			connect to ground GNDD
14	GNDP	SUPPLYD	X	Ground, Output Pin Driver
15	VSUPP	SUPPLYD	X	Supply Voltage, Output Pin Driver
16	FIFORRD	OUT	LV	FIFO Read counter Reset
17	FIFORD	OUT	LV	FIFO Read Enable
18	FIFOWR	OUT	LV	FIFO Write Enable
19	FIFORWR	OUT	LV	FIFO Write counter Reset
20	PWM1	OUT	LV	I^2C-controlled DAC
21	PWM2	OUT	LV	I^2C-controlled DAC
22	PWMV	OUT	LV	I^2C-controlled DAC
23	HOUT	OUT	X	Horizontal Drive Output
24	VSTBY	SUPPLYD	GNDP	Standby Supply Voltage, HOUT generation
25	DFVBL	OUT	LV	Dynamic focus blanking / horizontal DAF pulse
26	HSYNC	OUT	LV	Horizontal sync output
27	VSYNC	OUT	LV	Vertical sync output
28	NC			connect to ground GNDO
29	ASG1	SUPPLYA	X	Analog Shield Ground
30	HFLB	IN	HOUT	Horizontal Flyback Input
31	SAFETY	IN	GNDO	Safety Input
32	VPROT	IN	GNDO	Vertical Protection Input
33	RSW2	OUT	LV	Range Switch2, Measurement ADC
34	RSW1	IN/OUT	LV	Range Switch1, Measurement ADC
35	SENSE	IN	GNDO	Sense ADC Input
36	GNDM	SUPPLYA	X	Ground, MADC Input
37	VERT+	OUT	GNDO	Differential Vertical Sawtooth Output
38	VERT−	OUT	GNDO	Differential Vertical Sawtooth Output
39	EW	OUT	GNDO	East West CorrectionOutput
40	NC			connect to ground GNDO
41	SVM	OUT	VSUPO	Scan Velocity Modulation
42	ROUT	OUT	VSUPO	Analog Output Red

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
43	GOUT	OUT	VSUPO	Analog Output Green
44	BOUT	OUT	VSUPO	Analog Output Blue
45	GNDO	SUPPLYA	X	Ground, Analog Back-end
46	XREF	IN	X	Reference Input for RGB DACs
47	VSUPO	SUPPLYA	X	Supply Voltage, Analog Back-end
48	VRD/BCS	IN	X	DAC Reference, Beam Current Safety
49	AGND	SUPPLYA	X	Analog Ground for analog Matrix
50	FBLIN1	IN	GNDO	Fast-Blank1 Input
51	RIN1	IN	GNDO	Analog Red1 Input
52	GIN1	IN	GNDO	Analog Green1 Input
53	BIN1	IN	GNDO	Analog Blue1 Input
54	FBLIN2	IN	GNDO	Fast-Blank2 Input
55	RIN2 / P_R	IN	GNDO	Analog Red2 / P_R Input
56	GIN2 / Y	IN	GNDO	Analog Green2 / Y Input
57	BIN2 / P_B	IN	GNDO	Analog Blue2 / P_B Input
58	ASG2	SUPPLYA	X	Analog Shield Ground
59	HCS	IN	GNDD	Half-Contrast
60	NC			connect to GNDO
61	TEST	IN	GNDD	Test Pin, connect to GNDD
62	RESQ	IN	X	Reset Input, active low
63	SCL	IN/OUT	X	I^2C-bus Clock
64	SDA	IN/OUT	X	I^2C-bus Data
65	C0	IN	GNDD	Picture Bus Chroma (LSB)
66	C1	IN	GNDD	Picture Bus Chroma
67	C2	IN	GNDD	Picture Bus Chroma
68	C3	IN	GNDD	Picture Bus Chroma
69	C4	IN	GNDD	Picture Bus Chroma
70	C5	IN	GNDD	Picture Bus Chroma
71	C6	IN	GNDD	Picture Bus Chroma
72	C7	IN	GNDD	Picture Bus Chroma (MSB)
73	VSUPD	SUPPLYD	X	Supply Voltage, Digital Circuitry

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
74	GNDD	SUPPLYD	X	Ground, Digital Circuitry
75	Y0	IN	GNDD	Picture Bus Luma (LSB)
76	Y1	IN	GNDD	Picture Bus Luma
77	Y2	IN	GNDD	Picture Bus Luma
78	Y3	IN	GNDD	Picture Bus Luma
79	Y4	IN	GNDD	Picture Bus Luma
80	Y5	IN	GNDD	Picture Bus Luma

4.3. Pin Descriptions

Pin 3, Enable 656 mode, 656EN (Fig. 4–3)
Low level selects parallel mode with LLC2 = 27/32 MHz, a high level selects 656 mode with LLC2=54 MHz.

Pin 4, Main Clock Input, LLC2 (Fig. 4–3)
This is the input for the line-locked clock signal. The frequency can be 27, 32, 40.5, 54 MHz.

Pin 5, Sync Signal Input, HS (Fig. 4–3)
This pin gets the horizontal sync information. Either single or double horizontal frequency or VGA horizontal sync signal.

Pin 6, Sync Signal Input, VS (Fig. 4–3)
This pin gets the vertical sync information. Either single or double vertical frequency or VGA vertical sync signal.

Pin 7, H-Drive frequency of range select, FREQSEL (Fig. 4–3)
This pin selects the frequency range for the horizontal drive signal (see Section 2.3.2. on page 16).

Pin 8, Clock Select 1, CM1 (Fig. 4–3)
In case of a low level on 656EN, a low level on this pin selects 27/32 MHz, a high level selects 40.5 MHz (see Section 2.3.11. on page 21).

Pin 9, Clock Select 0, CM0 (Fig. 4–3)
In case of a low level on 656EN, a low level on this pin selects 27 MHz, a high level selects 32 MHz (see Section 2.3.11. on page 21).

Pin 10, Sync Signal Input, VS2 (Fig. 4–3)
Additional pin for the vertical sync information. Via I^2C-Register the used vertical sync can be switched between the inputs VS2 and VS (Pin 6)

Pin 11,12, Crystal Output, Input, XTAL2 , XTAL1 (Fig. 4–15)
These Pins are connected to an 5 MHz crystal oscillator. The security unit for the HOUT signal uses this clock signal as reference.

Pin 14, Ground, Output Pin Driver, GNDP[1)]
Output Pin Driver Reference

Pin 15, Supply Voltage, Output Pin Driver, VSUPP[1)]
This pin is used as supply for the following digital output pins: FIFORRD, FIFORD, FIFOWR, FIFORWR, PWM1, PWM2, PWMV, HOUT, DFVBL, HSYNC, VSYNC.

Pin 16, Reset for FIFO read counter, FIFORRD (Fig. 4–4)
This signal is active high and resets the read counter in the display frequency doubling FIFO.

Pin 17, Read enable for FIFO, FIFORD (Fig. 4–4)
This signal is active high and enables the read counter in the display frequency doubling FIFO.

Pin 18, Write enable for FIFO, FIFOWR (Fig. 4–4)
This signal is active high and enables the write counter in the display frequency doubling FIFO.

Pin 19, Reset for FIFO write counter, FIFORWR (Fig. 4–4)
This signal is active high and resets the write counter in the display frequency doubling FIFO.

Pin 20, Adjustable DC Output 1, PWM1 (Fig. 4–4)
This output delivers a DC voltage with a resolution of 8 bit, adjustable over the I2C bus. The output is driven by a push-pull stage. The PWM frequency is appr. 79.4 kHz. For a ripple-free voltage a first order low-pass filter with a corner frequency < 120 Hz should be applied.

Pin 21, Adjustable DC Output 2, PWM2 (Fig. 4–4)
See pin 20.

Pin 22, PWMV (Fig. 4–4)
This PWM output generates an adjustable vertical parabola with 7 bit resolution and appr. 79.4 kHz PWM frequency.

Pin 23, Horizontal Drive, HOUT (Fig. 4–7)
This open source output supplies the drive pulse for the horizontal output stage. A pulldown resistor has to be used (see Section 2.3. on page 16).

Pin 24, Standby Supply Voltage, HOUT generation, VSTBY[1)]
In standby mode, only the horizontal drive circuitry is active, regardless of **RESQ** (pin 62), with a duty cycle of ~79% at 55 kHz (represents the beginning of the softstart procedure). If this pin is connected to **GNDP** (pin 14), HOUT stays high after reset.

Pin 25, DFVBL (Fig. 4–4)
Blank pulse for dynamic focus during vertical blanking period, or free programmable horizontal pulse for horizontal dynamic focus generation

Pin 26, HSYNC (Fig. 4–4)
Horizontal sync output (in phase with the analog clamp pulse)

Pin 27, VSYNC (Fig. 4–4)
Vertical sync output (interlaced or progressive)

Pin 29, Shield Ground, Analog Backend, ASG1[1)]
Analog shield ground for the backend

Pin 30, Horizontal Flyback Input, HFLB (Fig. 4–3)
Via this pin the horizontal flyback pulse is supplied to the DDP (see Section 2.3. on page 16).

Pin 31, Safety Input, SAFETY (Fig. 4–3)
This input has two thresholds. A signal between the lower and upper threshold means normal function. A signal below the lower threshold or above the upper threshold is detected as malfunction and the RGB signals will be blanked. (see Section 2.3.8. on page 20).

Pin 32, Vertical Protection Input, VPROT (Fig. 4–3)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. If the peak-to-peak value of the vertical sawtooth signal is too small, the RGB output signals are blanked (see Section 2.3.8. on page 20).

Pin 33, Range Switch2 for measuring ADC, RSW2 (Fig. 4–9)
These pin is a open drain pulldown output. During cut-off measurement the switch is off. During white drive measurement the switch is on. Also during the rest of time it is on. (see Section 2.2.4. on page 14).

Pin 34, Range Switch1 or second input for measuring ADC, RSW1 (Fig. 4–10)
These pin is a open drain pulldown output. During cut-off and white drive measurement the switch is off. During the rest of time it is on. The RSW1 pin can be used as second measurement ADC input (see Section 2.2.4. on page 14).

Pin 35, Measurement ADC Input, SENSE (Fig. 4–8)
This is the input of the analog to digital converter for the picture and tube measurement. Three measurement ranges are selectable with RSW1 and RSW2 (see Section 2.2.4. on page 14).

Pin 36, Measurement ADC Reference Input,GNDM
This is the ground reference for the measurement A/D converter.

Pin 37, Vertical Sawtooth Output, VERT+ (Fig. 4–11)
This pin supplies the drive signal for the vertical output stage. The drive signal is generated with 15-bit precision. The analog voltage is generated by a 4 bit current-DAC with external resistor and uses digital noise shaping. An internal pull-down resistor can be enabled by software.

Pin 38, Vertical Sawtooth Output inverted, VERT– (Fig. 4–11)
This pin supplies the inverted signal of VERT+. Together with this Pin it can be used to drive symmetrical deflection amplifiers. An internal pull-down resistor can be enabled by software.

Pin 39, East-West Parabola Output, EW (Fig. 4–12)
This pin supplies the parabola signal for the East-West correction. The drive signal is generated with 15 bit precision. The analog voltage is generated by a 4 bit current-DAC with external resistor and uses digital noise shaping. An internal pull-down resistor can be enabled by software.

Pin 41, Scan Velocity Modulation Output, SVM (Fig. 4–14)
This output delivers the analog SVM signal (see Section 2.1.11. on page 12). The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

Pin 42, 43, 44, Analog RGB Output, ROUT, GOUT, BOUT (Fig. 4–14)
This are the analog Red/Green/Blue outputs of the backend. The outputs are current sinks.

Pin 45, Ground, Analog Backend, GNDO[1)]
This pin has to be connected to the analog ground. No supply current for the digital stages should flow through this line.

Pin 46, DAC Current Reference, XREF (Fig. 4–13)
External reference resistor for DAC output currents, typical 10 kΩ to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to analog ground as closely as possible to the pin.

Pin 47, Supply Voltage, Analog Backend, VSUPO[1)]
This pin has to be connected to the analog supply voltage. No supply current for the digital stages should flow through this line.

Pin 48, DAC Reference Decoupling/Beam Current Safety, VRD/BCS (Fig. 4–13)
Via this pin the DAC reference voltage is decoupled by an external capacitor. The DAC output currents depend on this voltage, therefore a pulldown transistor can be used to shut off all beam currents. A decoupling capacitor of 4.7 µF in parallel to 100 nF (low inductance) is required.

Pin 49, Reference Ground, Analog matrix, AGND[1)]
Analog reference ground for the analog RGB matrix

Pin 50, 54, Fast Blank Input, FBLIN1/2 (Fig. 4–5)
These pins are used to switch the RGB outputs to the external analog RGB inputs. FBLIN1 switches the RIN1, GIN1 and BIN1 inputs, FBLIN2 switches the RIN2, GIN2 and BIN2 inputs. The active level (low or high) can be selected by software.

Pin 51, 52, 53, Analog RGB Input 1, RIN1, GIN1, BIN1 (Fig. 4–6)
These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can by switched to the analog RGB outputs with the fast blank signal. Separate brightness and contrast settings for the external analog signals are provided (see Section 2.2.1. on page 13 and Fig. 2–18 on page 20).

Pin 55, 56, 57, Analog RGB / YP_BP_R Input2, RIN2/P_R, GIN2/Y, BIN2/P_B (Fig. 4–6)
These pins are used to insert an external analog RGB or YP_BP_R signal, e.g. from a SCART connector which can by switched to the analog RGB outputs with the fast blank signal. In case of YP_BP_R an analog HDTV RGB matrix transforms the input to RGB signals. Separate brightness and contrast settings for the external analog signals are provided (see (see Section 2.2.1. on page 13 and Fig. 2–18 on page 20).

Pin 58, Shield Ground, Amalog Backend, ASG2[1)]
Analog shield ground for the backend

Pin 59, Half Contrast Input, HCS (Fig. 4–3)
Via this input pin the output level of the analog RGB signals can be reduced by 6dB.

Pin 61, Test Input, TEST (Fig. 4–3)
This pin enables factory test modes. For normal operation it must be connected to ground.

Pin 62, Reset Input, RESQ (Fig. 4–3)
A low level on this pin resets the DDP 3315C.

Pin 63, I^2C Clock Input, SCL (Fig. 4–16)Via this pin the clock signal for the I2C-bus will be supplied. The signal can be pulled down by an internal transistor.

Pin 64, I^2C Data Input/Output, SDA (Fig. 4–16)
Via this pin the I2C-bus data are written to or read from the DDP.

Pin 65...72, Picture Bus Chroma, C0...C7 (Fig. 4–3)
The Picture Bus Chroma lines carry the multiplexed color component data. For the 4:1:1 input signal (4 bit chroma) the pins C4...C7 are used.

Pin 73, Supply Voltage, Digital Circuitry, VSUPD[1)]

Pin 74, Ground, Digital Circuitry, GNDD[1)]
Digital Circuitry Input Reference

Pin 75...80, 1, 2, Picture Bus Luma, Y0...Y7 (Fig. 4–3)
The Picture Bus Luma lines carry the digital luminance data.

[1)] **Application Note**:
All ground pins should be connected separately with short and low resistive lines to a central power supply ground. Accordingly all supply pins should be connected separately with short and low resistive lines to the power supply. Decoupling capacitors from VSUPP to GNDP, VSUPD to GNDD, and VSUPO to GNDO are recommended as close at possible to the pins.

4.4. Pin Configuration

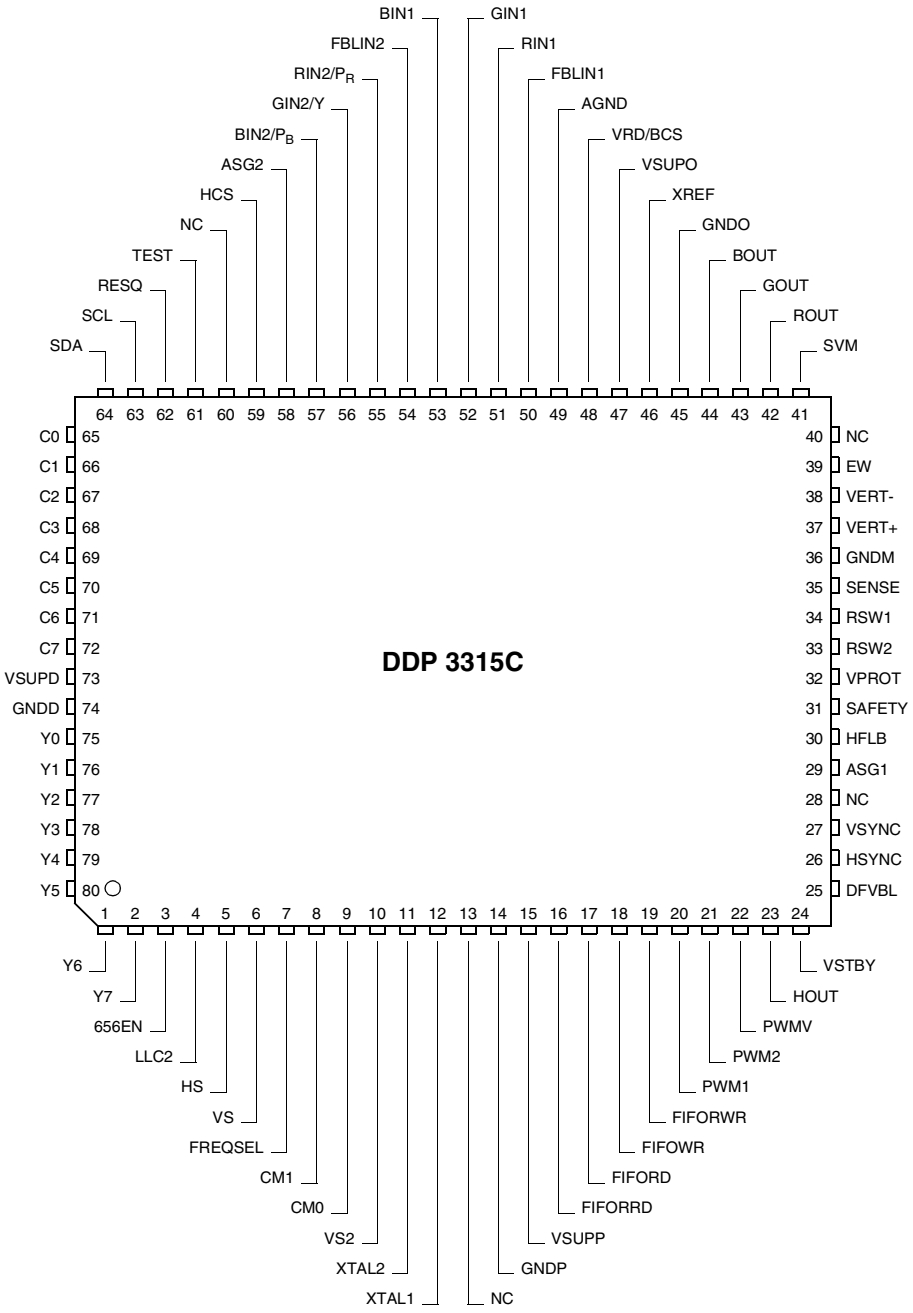


Fig. 4–2: PQFP80 package

4.5. Pin Circuits

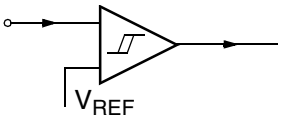


Fig. 4–3: Input pins LLC2, C[7:0], Y[7:0], HS, VS, VS2, HFLB, SAFETY, VPROT, 656EN, CM0, CM1, FREQSEL, RESQ, TEST, HCS

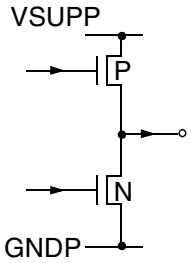


Fig. 4–4: Output pins FIFORRD, FIFORD, FIFOWR, FIFORWR, DFVBL, HSYNC, VSYNC, PWM1, PWM2, PWMV

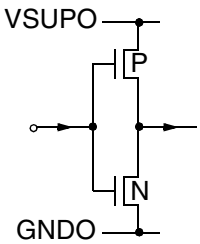


Fig. 4–5: Analog fastblank pins FBLIN1, FBLIN2

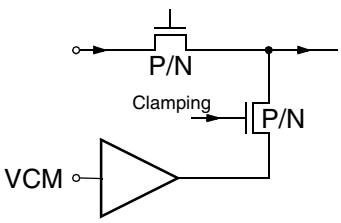


Fig. 4–6: Input pins RIN1, GIN1, BIN1, RIN2/P_R, GIN2/Y, BIN2/P_B

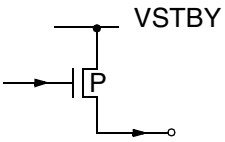


Fig. 4–7: Output pin HOUT

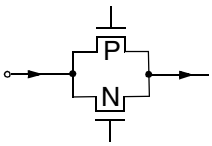


Fig. 4–8: Input pin SENSE

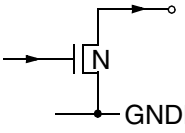


Fig. 4–9: Output pin RSW2

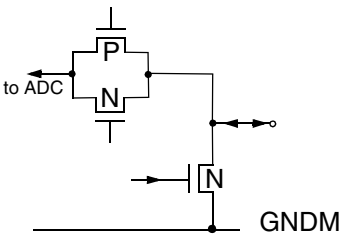


Fig. 4–10: I/O pin RSW1

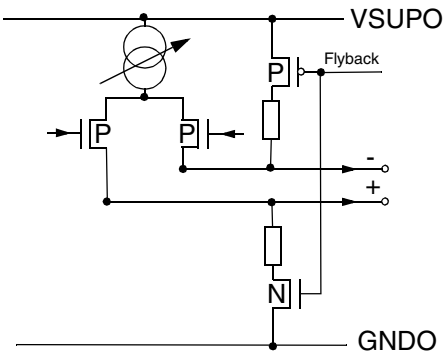


Fig. 4–11: Output pins VERT+, VERT-

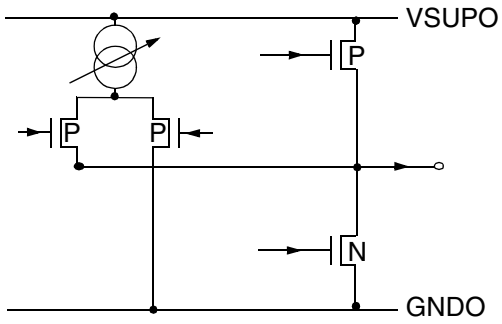


Fig. 4–12: Output pin EW

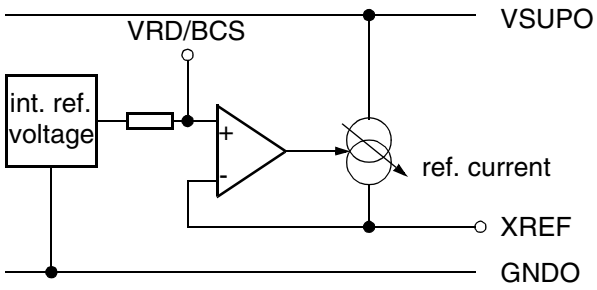


Fig. 4–13: Input pins XREF, VDR/BCS

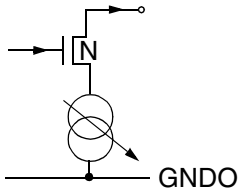


Fig. 4–14: Output pins SVM, ROUT, GOUT, BOUT

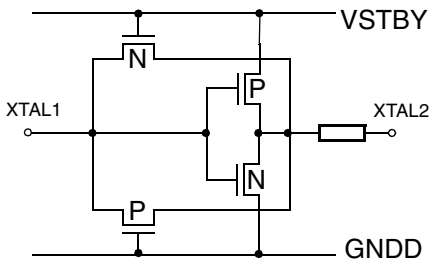


Fig. 4–15: Input pin XTAL1, Output pin XTAL2

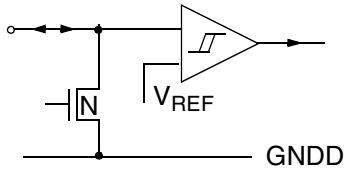


Fig. 4–16: I/O pins SCL, SDA

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-	0	65	°C
T_S	Storage Temperature	-	–40	125	°C
V_{SUP}	Supply Voltage	All Supply Pins	–0.3	6	V
V_I	Input Voltage	RESQ, SDL, SCL	–0.3	6	V
V_I	Input Voltage	All other Inputs	–0.3	$V_{SUP(D/O)}$+0.3	V
V_O	Output Voltage	All Outputs	–0.3	$V_{SUP(P/D/O)}$+0.3	V
V_{GD}	Voltage between different ground pins	All Ground Pins	-	0.3	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature		0	-	65	°C
T_C	Case Temperature		0	-	105	°C
V_{SUPO}	Supply Voltages, all analog Supply Pins	VSUPO	4.75	5.0	5.25	V
V_{SUPP}	Supply Voltages, all Output Pin Drivers	VSUPP VSTBY	3.15	3.3	3.45	V
V_{SUPD}	Supply Voltages, all digital Supply Pins	VSUPD	3.15	3.3	3.45	V
f_{sys}	Clock Frequency with CM0 = CM1 = 656EN = GNDD	LLC2	25	-	29	MHz
f_{sys}	Clock Frequency with CM0 = 656EN = GNDD CM1 = VSUPD	LLC2	29.7	-	34.3	MHz
f_{sys}	Clock Frequency with CM0 = CM1 = GNDD 656EN = VSUPD	LLC2	50	-	57.8	MHz
R_{xref}	RGB - DAC Current defining Resistor	XREF	9.5	10	10.5	kΩ

4.6.3. Recommended Crystal Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
f_P	Parallel Resonance Frequency @ C_L = 16 pF	XTAL1 XTAL2	-	5	-	MHz
R_R	Series Resonance Resistance @ C_L = 16 pF, f_P = 5 MHz		-	-	150	Ω
C_0	Shunt (Parallel) Capacitance		-	-	6	pF
C_{Lext} (see Note!)	External Load Capacitances (from both crystal pins connected to GNDD)		-	27	-	pF

Note: External capacitors at each crystal pin to ground are required. They are necessary to tune the effective load capacitance (including the capacitance of the printed circuit board and the IC package) to the required load capacitance C_L of the crystal. A higher capacitance will result in a lower clock frequency. The exact value of the matching capacitor should be determined in the actual application (PCB layout).
$C_{Lext} = 2 (C_L - C_{PCB} - C_{PACK})$

4.6.4. Characteristics

Min./Max. values at T_A = 0 to 65 °C, $V_{SUP(P/D)}$ = 3.15 to 3.45 V, V_{SUPO} = 4.75 to 5.25 V, f = 27 MHz
Typical values at: T_C = 70 °C, $V_{SUP(P/D)}$ = 3.3 V, V_{SUPO} = 5 V, f = 27 MHz
all values with R_{xref} = 10 kΩ

4.6.4.1. General Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
P_{TOT}	Total Power Dissipation		-	0.750	1.0	W
I_{VSUPO}	Current Consumption Analog Backend	VSUPO	-	100	tbd	mA
I_{VSUPD}	Current Consumption Digital Processing	VSUPD	-	70	tbd	mA
I_{VSUPP}	Current Consumption Output Pin Driver	VSUPP	-	2	tbd	mA
I_{VSTBY}	Current Consumption horizontal drive generation	VSTBY	-	0.4	-	mA
I_L	Input and Output Leakage Current (if not otherwise specified)		1	-	1	µA

4.6.4.2. LLC2: Line-locked Clock Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	LLC2	-	-	0.8	V	
V_{IH}	Input High Voltage		2.0	-	-	V	
t_R, t_F	Clock Rise / Fall Time		-	-	T_{LLC2}/ 4	ns	
C_{IN}	Input Capacitance		-	5	-	pF	
$1/T_{LLC2}$	Clock Frequency		12.5	-	56.7	MHz	
t_{WL2}	Clock Low Time		tbd	-	-	ns	
t_{WH2}	Clock High Time		tbd	-	-	ns	

4.6.4.3. Luma, Chroma Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	Y[0...7] C[0...7] HS VS VS2	-	-	0.8	V	
V_{IH}	Input High Voltage		2.0	-	-	V	
t_{IS}	Input Setup Time		4	-	-	ns	
t_{IH}	Input Hold Time		4	-	-	ns	
C_{IN}	Input Capacitance		-	5	-	pF	

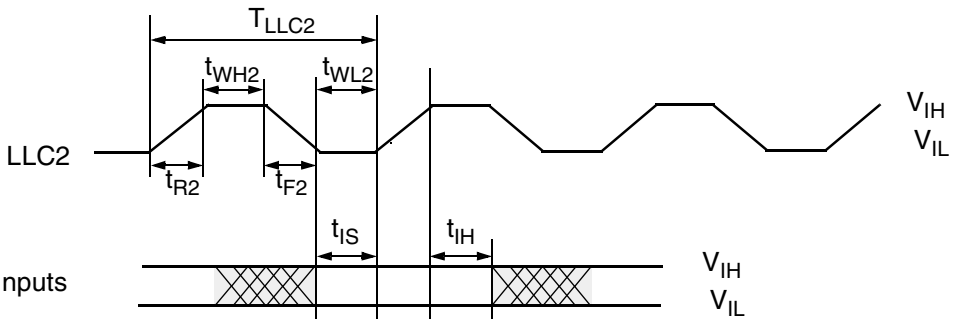


Fig. 4–17: Line-locked clock input pins and luma / chroma bus input timing

4.6.4.4. Digital Inputs, Static Pins

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HCS RESQ TEST	-	-	0.8	V	
V_{IH}	Input High Voltage		2.0	-	-	V	
C_{IN}	Input Capacitance	CM0 CM1 656EN FREQSEL	-	5	-	pF	

4.6.4.5. I²C-Bus Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	SDA SCL	-	-	0.8	V	
V_{IH}	Input High Voltage		2.0	-	-	V	
V_{OL}	Output Low Voltage		-	-	0.6	V	I_{OL} = 6 mA
I_{OL}	Output Low Current		-	-	10	mA	
C_{IN}	Input Capacitance		-	-	5	pF	
t_F	Signal Fall Time		-	-	300	ns	C_L = 400 pF
t_R	Signal Rise Time		-	-	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	-	400	kHz	
t_{LOW}	Low Period of SCL		1.3	-	-	µs	
t_{HIGH}	High Period of SCL		0.6	-	-	µs	
t_{IS}	Input data Set Up Time to SCL high	SDA	55	-	-	ns	
t_{IH}	Input data Hold Time to SCL low		55	-		ns	
t_{OD}	Output data Delay Time to SCL high		tbd	-	-	ns	
t_{OH}	Output data Hold Time to SCL low		15	-	900	ns	

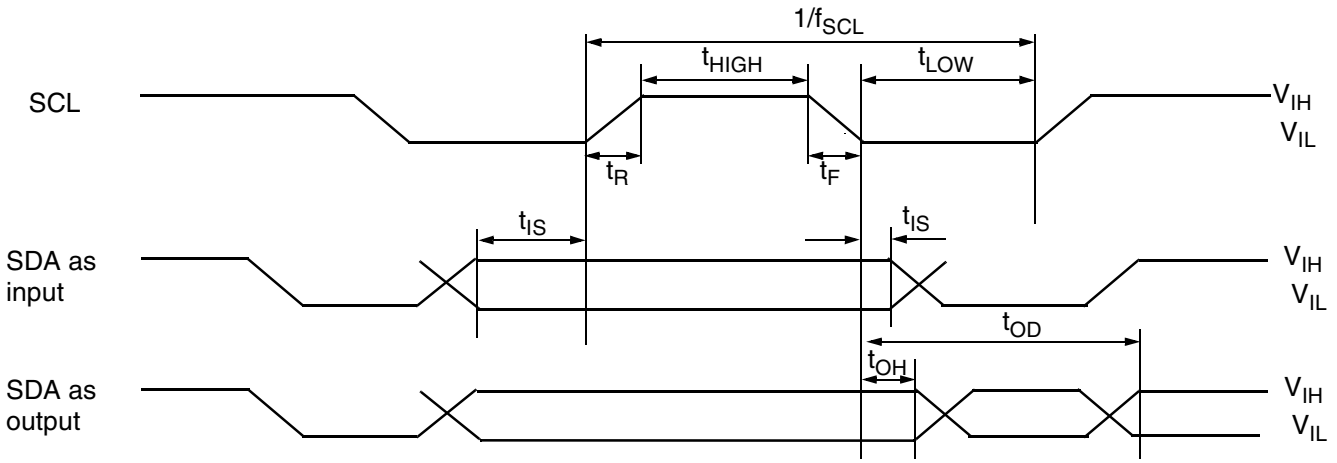


Fig. 4–18: I²C bus timing

4.6.4.6. Horizontal Flyback Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HFLB	-	-	1.9	V	
V_{IH}	Input High Voltage		2.5	-	-	V	
V_{IMAX}	Maximum Input Voltage				V_{SUPO} +0.3	V	maximum clamping current ~10mA average
V_{IHST}	Input Hysteresis			0.2	-	V	

4.6.4.7. Sync Signals and PWM Outputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	FIFORRD FIFORD FIFORWR FIFOWR DFVBL HSYNC VSYNV PWM1 PWM2 PWMV	-	-	0.4	V	I_{OL} = 1.6 mA I^2C[PSTFFC] = 6
V_{OH}	Output High Voltage		VSUPP – 0.4	-	VSUPP	V	$-I_{OL}$ = 1.6 mA I^2C[PSTFFC] = 6
t_{OT}	Output Transition Time		-	10	20	ns	C_{LOAD} = 30 pF I^2C[PSTFFC] = 6
I_{OL}	Output Current		–10	-	10	mA	

4.6.4.8. Horizontal Drive Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	HOUT	-	-	-	V	external pull-down resistor
V_{OH}	Output High Voltage (Open Source Stage)		-	-	VSTBY	V	
t_{OF}	Output Fall Time		-	tbd		ns	C_{LOAD} = 30pF
I_{OH}	Output High Current		-	-	60	mA	

4.6.4.9. Vertical Protection Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IA}	Input Threshold A	VPROT		1.0		V	
V_{IB}	Input Threshold B			1.5		V	
V_{IMAX}	Maximum Input Voltage				V_{SUPO} +0.3	V	maximum clamping current ~10 mA average
V_{IHST}	Input Hysteresis A and B		0.1	-	-	V	

4.6.4.10. Horizontal Safety Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IA}	Input Threshold A	SAFETY		2.2		V	
V_{IB}	Input Threshold B			3.4		V	
V_{IMAX}	Maximum Input Voltage				V_{SUPO} +0.3	V	maximum clamping current ~10 mA average
V_{IHST}	Input Hysteresis A and B		0.1	-	-	V	

4.6.4.11. Vertical and East/West D/A Converter Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
	Resolution	EW VERT+ VERT–	-	15	-	bit	
V_{OMIN}	Minimum Output Voltage		-	0	-	V	R_{load} = 6.8 kΩ R_{xref} = 10 kΩ
V_{OMAX}	Maximum Output Voltage		2.82	3	3.2	V	R_{load} = 6.8 kΩ R_{xref} = 10 kΩ
I_{DACN}	Full scale DAC Output Current		415	440	465	µA	R_{xref} = 10 kΩ
PSRR	Power Supply Rejection Ratio		-	20	-	dB	

4.6.4.12. East/West PWM Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	EW	-	-	0.4	V	I_{OL} = 1.6 mA I^2C[PSTEW] = 6
V_{OH}	Output High Voltage		VSUPO – 0.4	-	VSUPO	V	–IOL = 1.6 mA I2C[PSTPWEW] = 6
t_{OT}	Output Transition Time		-	tbd		ns	CLOAD = 10 pF Rlp = 4.7 kΩ Clp = 100 nF I2C[PSTPEW] = 6

4.6.4.13. Sense A/D Converter Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{I511}	Input Voltage for code 511	SENSE RSW1	-	2.6	-	V	
C_0	Digital Output for zero Input		-	-	16	LSB	
R_I	Input Impedance		1	-	-	MΩ	
Range Switch Outputs							
R_{ON}	Output On Resistance	RSW1 RSW2	-	-	50	Ω	I_{OL} = 10 mA
I_{Max}	Maximum Current		-	-	15	mA	
I_{LEAK}	Leakage Current		-	-	600	nA	RSW High Impedance

4.6.4.14. Analog RGB / YP_BP_R and FB Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$V_{RGBINPP}$	nominal RGB Input Voltage peak-to-peak	RIN1 GIN1 BIN1 RIN2/P_R GIN2/Y BIN2/P_B	0.5	0.7	1.0	V_{PP}	SCART Spec: 0.7 V ±3 dB
I_{LSB}	minimum current step size		3.13	4.4	6.25	µA	
V_{RGBIN}	RGB Input Voltage for Maximum Output Current		-	0.5	-		Contrast setting: tbd
			-	0.7	-		Contrast setting: tbd
			-	1.0	-		Contrast setting: tbd
C_{RGBIN}	External RGB Input Coupling Capacitor		-	15	-	nF	
t_c	Clamp Pulse Width			1.6		µs	
C_{IN}	Input Capacitance				tbd	pF	
I_{IL}	Input Leakage Current		–0.5	-	0.5	µA	Clamping OFF, V_{IN} = –0.3...3.5 V
V_{INOFF}	Offset Voltage		–10	-	10	mV	
$V_{RGBINMAX}$	Absolute Maximum External RGB Input Voltage Range	RIN1 GIN1 BIN1	–0.3	-	1.4	V	at Pin
V_{CLAMP}	Clamp Level at Input			0.2		V	Clamping ON
I_{ICMAX}	Maximum clamp current during t_c		–1.5	-	1.5	mA	Clamping ON
V_{CLIP}	RGB Input Voltage for Clipping Current		-	1.4	-	V	
$V_{RGBINMAX}$	Absolute Maximum External RGB Input Voltage Range	RIN2/P_R GIN2/Y BIN2/P_B	1.6	-	3.5	V	at Pin
V_{CLAMP}	Clamp Level at Input			2.3		V	Clamping ON
I_{ICMAX}	Maximum clamp current during t_c		–3	-	3	mA	Clamping ON
V_{CLIP}	RGB Input Voltage for Clipping Current		-	1.4	-	V	
V_{FBLOFF}	FBLIN Low Level	FBLIN1 FBLIN2	-	-	0.5	V	
V_{FBLON}	FBLIN High Level		0.9	-	-	V	
$V_{FBLTRIG}$	Fast Blanking Trigger Level typical		-	0.7	-		
t_{PID}	Delay Fast Blanking to RGB_{OUT} from midst of FBLIN-transition to 90% of RGB_{OUT}- transition		-	8	15	ns	Internal RGB = 3.75 mA Full Scale Int. Brightness = 0 External Brightness = 1.5 mA (Full Scale) RGBin = 0 V_{FBLOFF} = 0.4 V V_{FBLON} = 1.0 V Rise and fall time = 2 ns
	Difference of Internal Delay to External RGBin Delay		–5	-	+5	ns	
	Switch-Over-Glitch		-	0.5	-	pAs	Switch from 3.75 mA (int) to 1.5 mA (ext)

4.6.4.15. Analog RGB Outputs, D/A Converters

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Internal RGB Signal D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	-	10	-	bit	
I_{FS}	Full Scale Output Current		3.6	3.75	3.9	mA	R_{ref} = 10 kΩ
DNL	Differential Nonlinearity		-	-	1	LSB	
INL	Integral Nonlinearity		-	-	2	LSB	
t_{rs}	Rise and Fall Time		-	3	-	ns	10% to 90%, 90% to 10%
SNR	Signal to Noise		+50	-	-	dB	Signal: 1 MHz full scale Bandwidth: 10 MHz
	RGB Gain Match		–2	-	2	%	R-G, R-B, G-B
	R/B/G Crosstalk from any 2 to the 3rd		-	-	–46	dB	Passive channel: I_{OUT} = 1.88 mA Crosstalk-Signal: 7 MHz, 3 mA_{PP}
	Crosstalk from external RGB to main RGB from any 3 to the 4th		-	-	–50	dB	
Internal RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	-	9	-	bit	
I_{FS}	Full Scale Output Current relative		39.2	40	40.8	%	Ref to max. digital RGB
I_{FS}	Full Scale Output Current absolute		-	1.5	-	mA	
DNL	Differential Nonlinearity		-	-	1	LSB	
INL	Integral Nonlinearity		-	-	2	LSB	
	RGB Gain Match		–2	-	2	%	R-G, R-B, G-B
	External RGB gain match to main RGB		–2	-	2	%	R-R, G-G, B-B
RGB Output Cutoff D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	-	9	-	bit	
I_{FS}	Full Scale Output Current relative		58.8	60	61.2	%	Ref to max. digital RGB
I_{FS}	Full Scale Output Current absolute		-	2.25	-	mA	
DNL	Differential nonlinearity		-	-	1	LSB	
INL	Integral nonlinearity		-	-	2	LSB	
	External RGB gain match to main RGB		–2	-	2	%	R-R, G-G, B-B

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
RGB Output Ultrablack D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	-	1	-	bit	
I_{FS}	Full Scale Output Current relative		19.6	20	20.4	%	Ref to max. digital RGB
	Full Scale Output Current absolute		-	0.75	-	mA	
External RGB / YP_BP_R Voltage/Current Converter Characteristics							
	Resolution	ROUT GOUT BOUT	-	11	-	bit	
I_{FS}	Full Scale Output Current relative		96	100	104	%	Ref. to max. Digital RGB V_{IN} = 0.7 V_{PP}, contrast = 1800
	Full Scale Output Current absolute		-	3.75	-	mA	Ref. to max. Digital RGB V_{IN} = 0.7 V_{PP}, contrast = 1800
CR	Contrast Adjust Range			0:2047	-		
	RGB Gain Match		–2	-	2	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 1800
	R/B/G Crosstalk from any 2 to the 3rd		-	-	–46	dB	Passive channel: V_{IN} = 0.7 V, contrast = 1800 Crosstalk signal: 7 MHz, 3 mA_{PP}
	RGB Crosstalk from main RGB from any 3 to the 4th		-	-	–50	dB	
	RGB Input Noise and Distortion		-	-	–50	dB	V_{IN} = 0.7 V_{PP} at 7 MHz Bandwidth: 10 MHz
	RGB Input Bandwidth –3dB		25		-	MHz	V_{IN} = 0.7 V_{PP},
	RGB Input THD		- -		–50 –40	dB dB	Input signal 1 MHz Input signal 7 MHz V_{IN} = 0.7 V_{PP}
	Differential Nonlinearity of Contrast Adjust		-	-	1.0	LSB	V_{IN} = 0.7 V
	Integral Nonlinearity of Contrast Adjust		-	-	7	LSB	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
External RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	-	9	-	bit	
I_{EXBR}	Full Scale Output Current relative		39.2	40	40.8	%	Ref to max. digital RGB
	Full Scale Output Current absolute		-	1.5	-	mA	
	Differential Nonlinearity		-	-	1	LSB	
	Integral Nonlinearity		-	-	2	LSB	
	RGB Gain Match		–2	-	2	%	R-G, R-B, G-B
Analog RGB output Pins							
V_{RGBO}	R,G,B Output Voltage	ROUT GOUT BOUT	–1.0	-	0.3	V	Referred to V_{SUPO}
I_{MAX}	Maximum output current			8.25		mA	All DAC with full scale

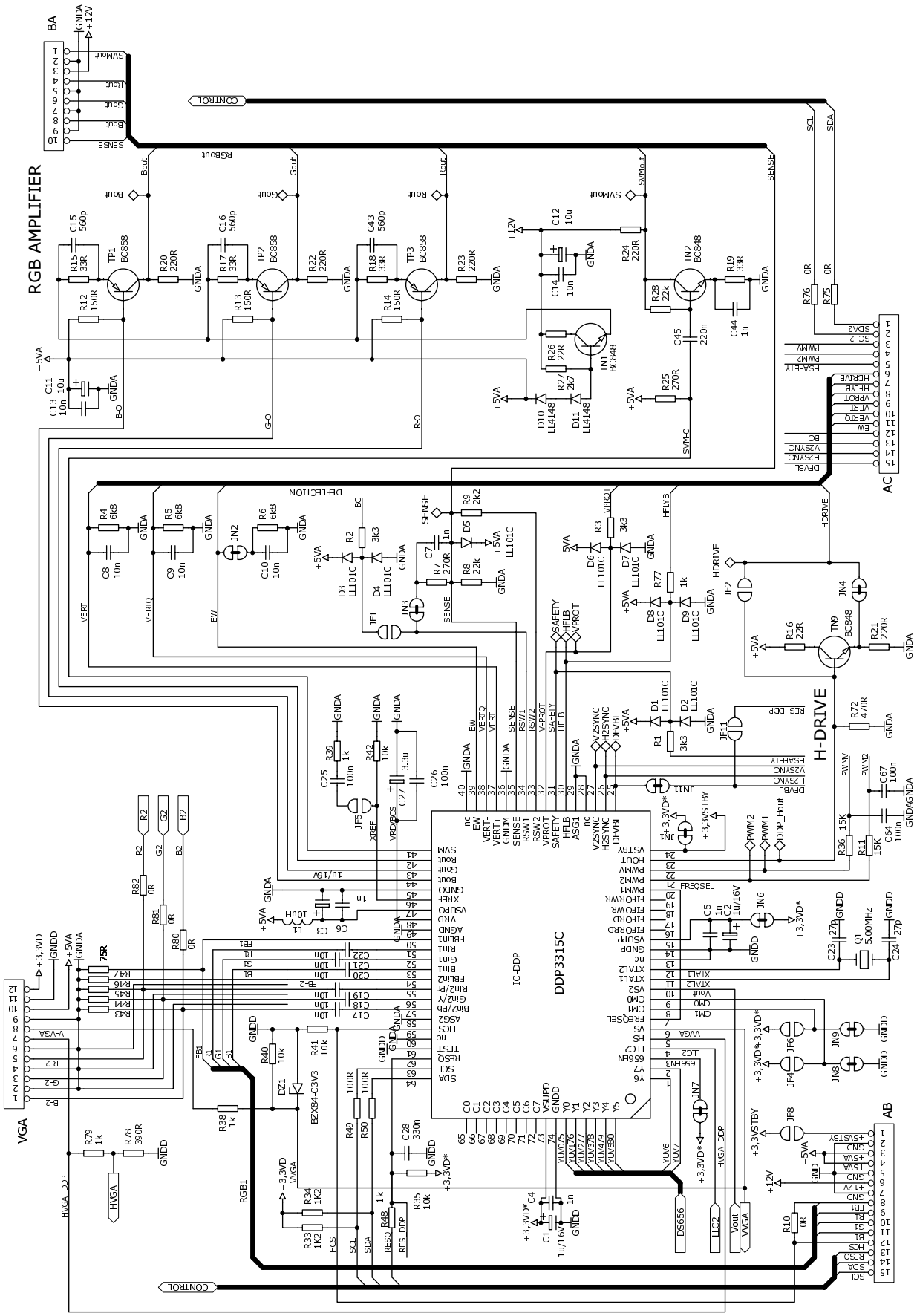
4.6.4.16. Scan Velocity Modulation Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
	Resolution	SVMOUT	-	8	-	bit	
I_{OUT}	Full Scale Output Current		1.55	1.875	2.25	mA	
I_{OUT}	Differential Nonlinearity		-	-	0.5	LSB	
I_{OUT}	Integral Nonlinearity		-	-	1	LSB	
I_{OUT}	Glitch Pulse Charge		-	0.5	-	pAs	Ramp, output line is terminated on both ends with 50 Ω
I_{OUT}	Rise and Fall Time		-	3	-	ns	10% to 90%, 90% to 10%

4.6.4.17. DAC Reference, Beam Current Safety

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{DACREF}	DAC-Ref. Voltage	VRD/BCS	2.38	2.50	2.67	V	
	DAC-Ref. Output resistance	VRD/BCS	18	25	32	kΩ	
V_{XREF}	DAC-Ref. Voltage Bias Current Generation	XREF	2.3	2.5	2.7	V	R_{xref} = 10 kΩ

5. Application Circuit



6. Data Sheet History

1. Advance Information: “DDP 3315C Display and Deflection Processor”, Dec. 5, 2001, 6251-521-1AI. First release of the advance information.

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