

SERIAL ACCESS CMOS 1K (128 x 8) EEPROMs

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
 - 4.5V to 5.5V for ST24C01 version
 - 3V to 5.5V for ST24x01C versions
 - 2.5V to 5.5V for ST25C01, ST25x01C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W01C and ST25W01C
- TWO WIRE SERIAL INTERFACE, FULLY I²C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES FOR "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C01C and ST24/25W01C

DESCRIPTION

This specification covers a range of 1K bits I²C bus EEPROM products, the ST24/25C01, the ST24/25C01C and the ST24/25W01C. In the text, products are referred to as ST24/25x01C, where

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
\overline{WC}	Write Control (W version)
V _{cc}	Supply Voltage
V _{ss}	Ground

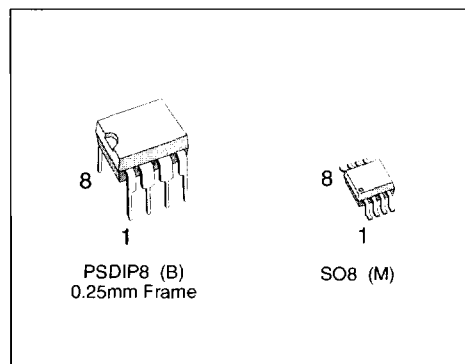
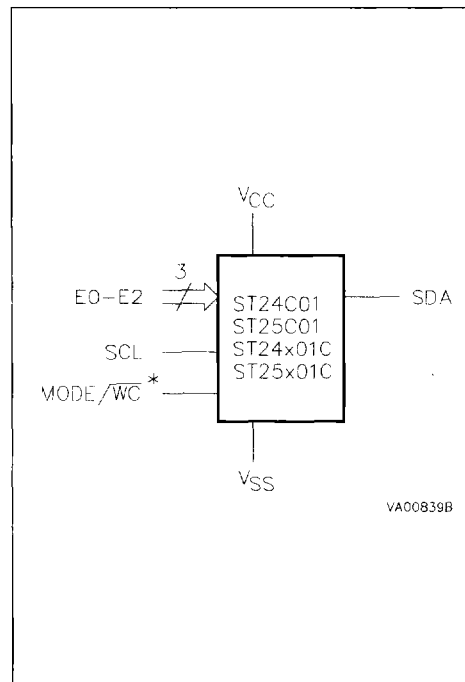


Figure 1. Logic Diagram



Note: WC signal is only available for ST24/25W01C products.

Figure 2A. DIP Pin Connections

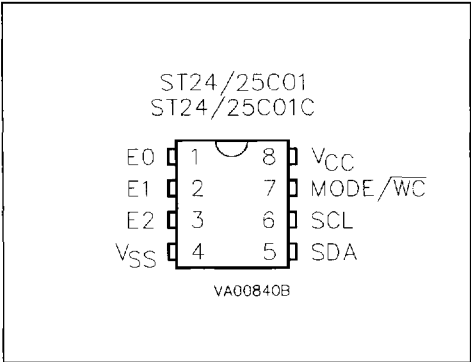


Figure 2B. SO Pin Connections

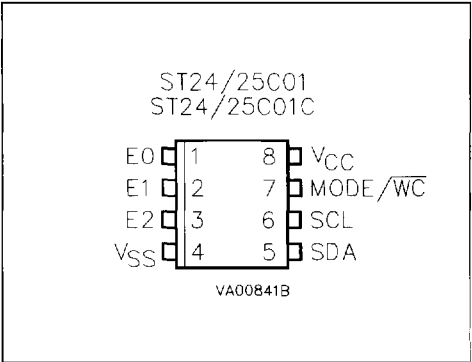


Table 2. Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter		Value	Unit
T _A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 -40 to 125 -40 to 85	°C
T _{STG}	Storage Temperature		-65 to 150	°C
T _{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V _O	Output Voltage	ST24/25C01 ST24/25x01C	-0.3 to V _{CC} +0.6 -0.3 to 6.5	V
V _I	Input Voltage		-0.3 to 6.5	V
V _{CC}	Supply Voltage		-0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ⁽²⁾	ST24/25C01 ST24/25x01C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) ⁽³⁾	ST24/25C01 ST24/25x01C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x01C are 1K bit electrically erasable programmable memories (EEPROM), organized as 128 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I²C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I²C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 1K devices may be attached to the I²C bus and selected individually. The memories behave as a slave device in the I²C protocol with all memory operations synchronized

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes ⁽¹⁾

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X		START, Device Select, RW = '0', Address
	'1'	X	1	reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write ⁽²⁾	'0'	V _{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V _{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}

2. Multibyte Write not available in ST24/25W01C versions.

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24C01, ST25C01	1,000,000	10
ST24C01C, ST25C01C ST24W01C, ST25W01C	1,000,000	10

by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

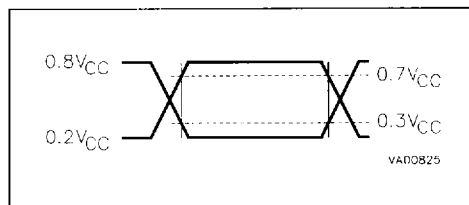
When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: Vcc lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the Vcc voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when Vcc drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable Vcc must be applied before applying any logic signal.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	$\leq 50\text{ns}$
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed

with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also \overline{WC} feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control (\overline{WC}). An hardware Write Control feature (\overline{WC}) is offered only for ST24W01C and ST25W01C versions on pin 7. This feature is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC} = V_{IH}$) or disable ($\overline{WC} = V_{IL}$) the internal write protection. When unconnected, the \overline{WC} input is internally read as V_{IL} . The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

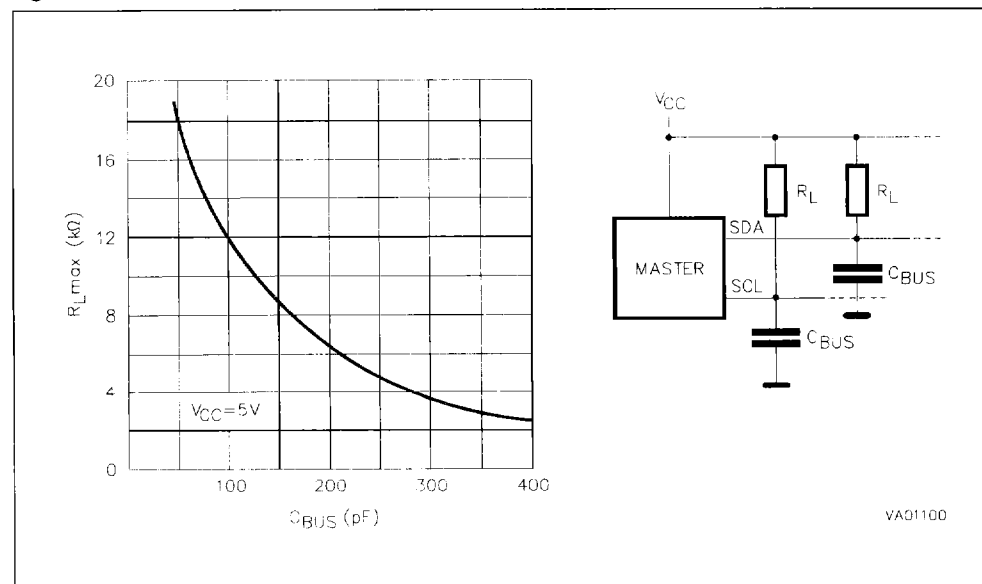
Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

Table 6. Capacitance ⁽¹⁾ ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 100\text{ kHz}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	\overline{WC} Input Impedance	$V_{IN} \leq 0.3 V_{CC}$	5	20	k Ω
Z_{WCH}	\overline{WC} Input Impedance	$V_{IN} \geq 0.7 V_{CC}$	500		k Ω

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characteristics

($T_A = 0\text{ to }70\text{ }^{\circ}\text{C}$, $-40\text{ to }85\text{ }^{\circ}\text{C}$ or $-40\text{ to }125\text{ }^{\circ}\text{C}$; $V_{CC} = 3\text{V to }5.5\text{V}$ or $2.5\text{V to }5.5\text{V}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		± 2	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		± 2	μA
I_{CC}	Supply Current	$V_{CC} = 5V$, $f_C = 100\text{kHz}$ (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	$V_{CC} = 2.5V$, $f_C = 100\text{kHz}$		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5V$		100	μA
		$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5V$, $f_C = 100\text{kHz}$		300	μA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5V$		5	μA
		$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5V$, $f_C = 100\text{kHz}$		50	μA
V_{IL}	Input Low Voltage (SCL, SDA)		-0.3	$0.3 V_{CC}$	V
V_{IH}	Input High Voltage (SCL, SDA)		$0.7 V_{CC}$	$V_{CC} + 1$	V
V_{IL}	Input Low Voltage (E0 - E2, MODE, WC)		-0.3	0.5	V
V_{IH}	Input High Voltage (E0 - E2, MODE, WC)		$V_{CC} - 0.5$	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3\text{mA}$, $V_{CC} = 5V$		0.4	V
	Output Low Voltage (ST25 series)	$I_{OL} = 2.1\text{mA}$, $V_{CC} = 2.5V$		0.4	V
$V_{POR}^{(1)}$	Power On Reset Threshold (ST25 series)		1.5	2.4	V
$V_{CC\text{ Read}}^{(1)}$	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
$V_{CC\text{ Write}}$	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25x01C, was not yet sufficient to guarantee a $V_{CC\text{ Read}} = 2V$. For the latest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics(T_A = 0 to 70 °C, -40 to 85 °C or -40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t _{CH1CH2}	t _R	Clock Rise Time		1	μs
t _{CL1CL2}	t _F	Clock Fall Time		300	ns
t _{DH1DH2}	t _R	Input Rise Time		1	μs
t _{DL1DL1}	t _F	Input Fall Time		300	ns
t _{CHDX} ⁽¹⁾	t _{SU:STA}	Clock High to Input Transition	4.7		μs
t _{CHCL}	t _{HIGH}	Clock Pulse Width High	4		μs
t _{DLCL}	t _{HD:STA}	Input Low to Clock Low (START)	4		μs
t _{CLDX}	t _{HD:DAT}	Clock Low to Input Transition	0		μs
t _{CLCH}	t _{LOW}	Clock Pulse Width Low	4.7		μs
t _{DXCX}	t _{SU:DAT}	Input Transition to Clock Transition	250		ns
t _{CHDH}	t _{SU:STO}	Clock High to Input High (STOP)	4.7		μs
t _{DHDL}	t _{BUF}	Input High to Input Low (Bus Free)	4.7		μs
t _{CLQV}	t _{AA}	Clock Low to Data Out Valid	0.3	3.5	μs
t _{CLQX}	t _{DH}	Clock Low to Data Out Transition	300		ns
f _C	f _{SCL}	Clock Frequency		100	kHz
t _{NS}	T _I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t _W ⁽²⁾	t _{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.

2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

DEVICE OPERATION

I²C Bus Background

The ST24/25x01C support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x01C are always slave devices in all communications.

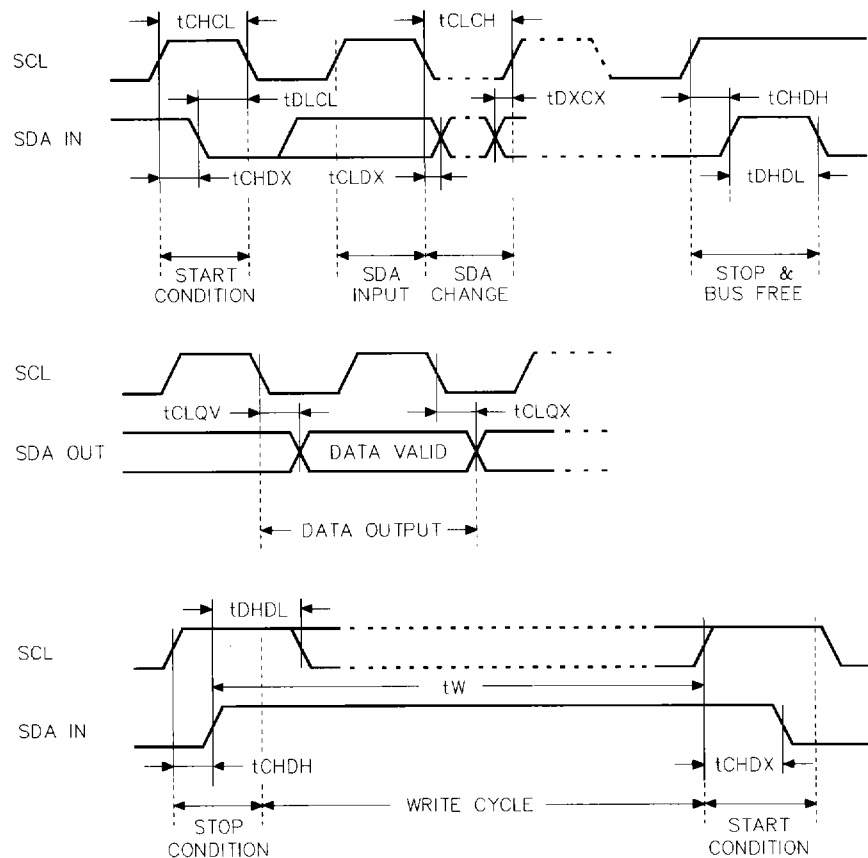
Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x01C continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x01C and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x01C sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Figure 5. AC Waveforms



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DEVICE OPERATION (cont'd)

Memory Addressing. To start communication between the bus master and the slave ST24/25x01C, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

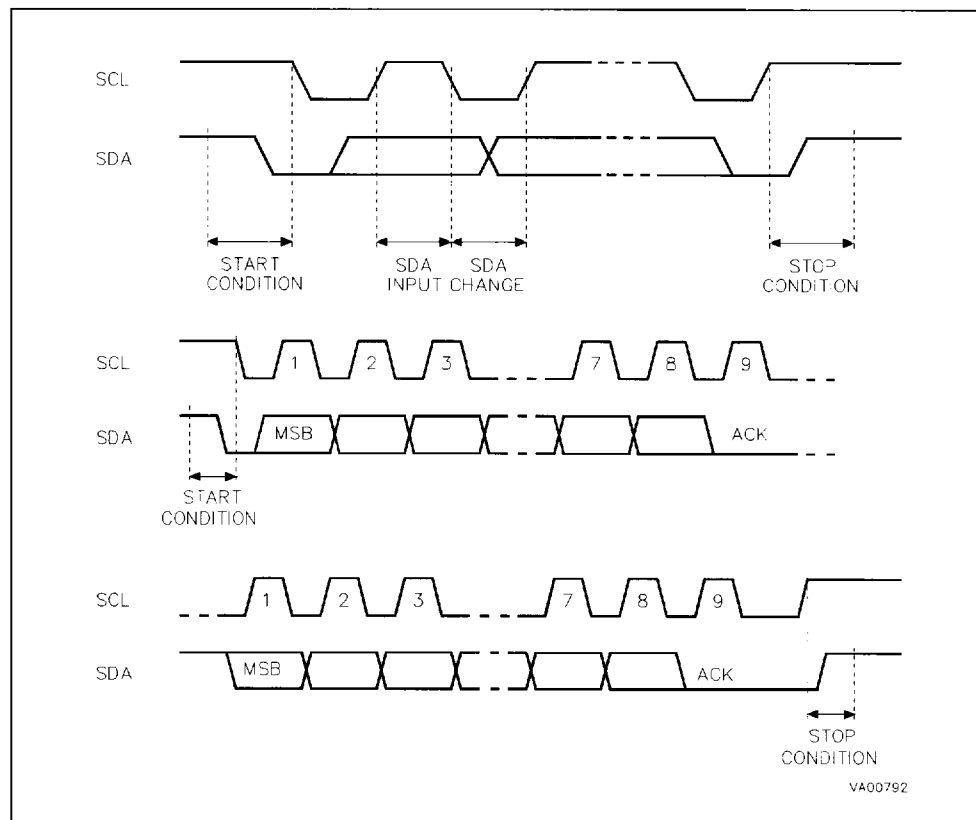
The 4 most significant bits of the device select code are the device type identifier, corresponding to the I²C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 1K memories can be connected on the same bus giving a memory capacity total of 8K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit (\overline{RW}), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Multibyte Write mode (only available on the ST24/25C01 and ST24/25C01C versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL} . The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the \overline{RW} bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 7 bits (the Most Significant Bit is ignored) provides access to any of the 128 bytes of the memory. After receipt of the

Figure 6. I²C Bus Protocol

byte address the device again responds with an acknowledge.

For the ST24/25W01C versions, any write command with $WC = 1$ (during a period of time from the START condition until the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL} to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH} . The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is $t_W = 10ms$ maximum except when bytes are accessed on 2 rows (that is have different values for the 5 most significant address bits A6-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL} . The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transferred, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK.

During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all '1's' (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the RW bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the RW bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the

DEVICE OPERATION (cont'd)

memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a

count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x01C wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x01C terminate the data transfer and switches to a standby state.

Figure 7. Write Cycle Polling using ACK

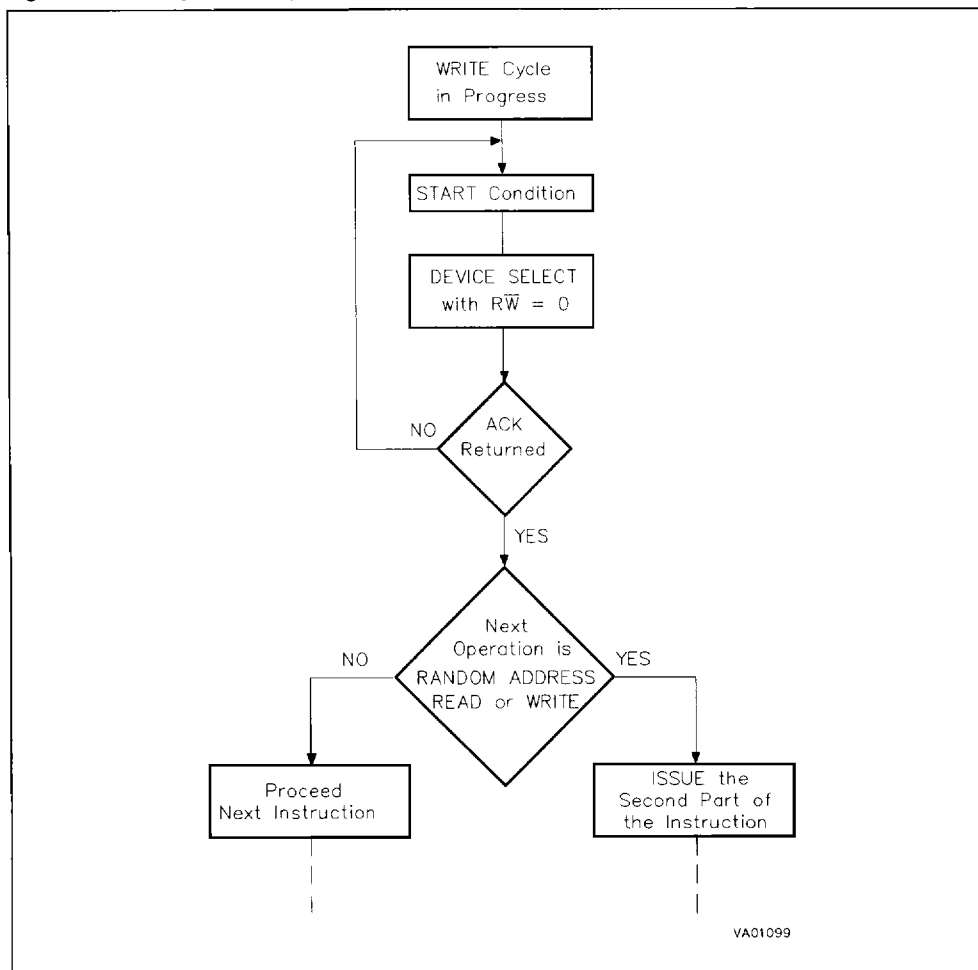


Figure 8. Write Modes Sequence (ST24/25C01, ST24/25C01C)

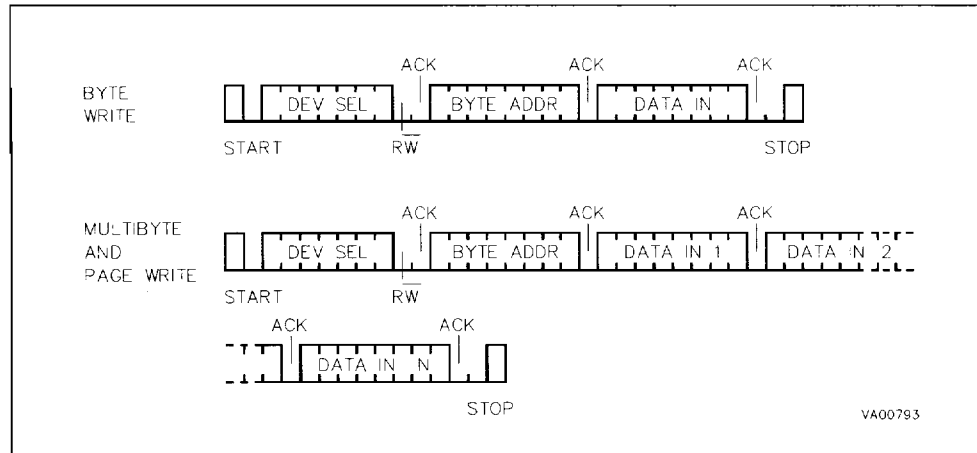


Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W01C)

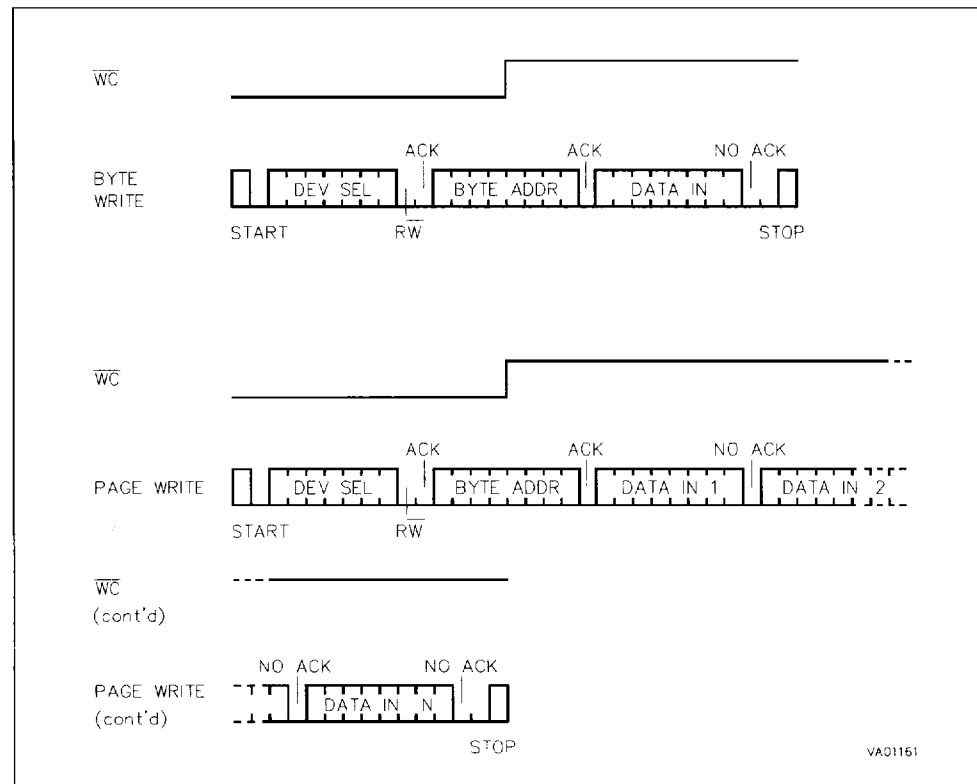
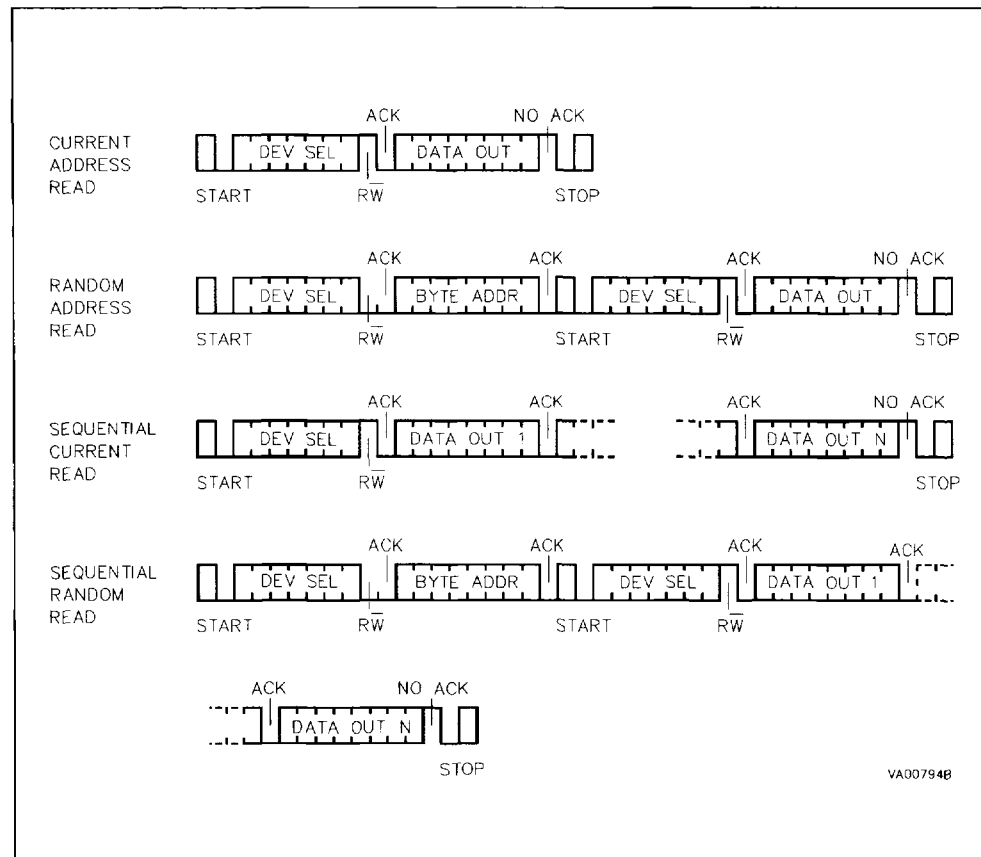
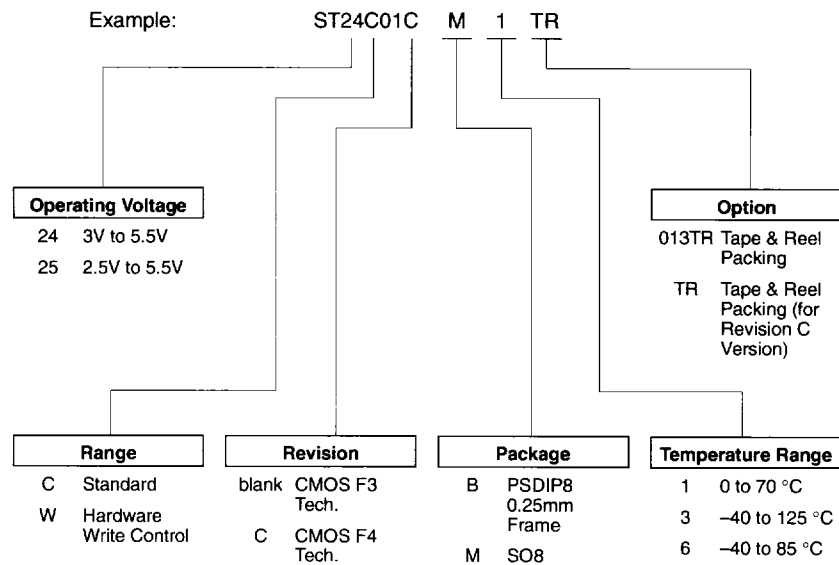


Figure 10. Read Modes Sequence



ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.