

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

August 1997

10-Bit, 12-Bit, Multiplying D/A Converters

Features

- **AD7520/AD7530, 10-Bit Resolution; 8-Bit, 9-Bit and 10-Bit Linearity**
- **AD7521/AD7531, 12-Bit Resolution; 8-Bit, 9-Bit and 10-Bit Linearity**
- **Low Power Dissipation (Max) 20mW**
- **Low Nonlinearity Tempco at 2ppm of FSR/°C**
- **Current Settling Time to 0.05% of FSR 1.0μs**
- **Supply Voltage Range ±5V to +15V**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

Description

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Harris' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

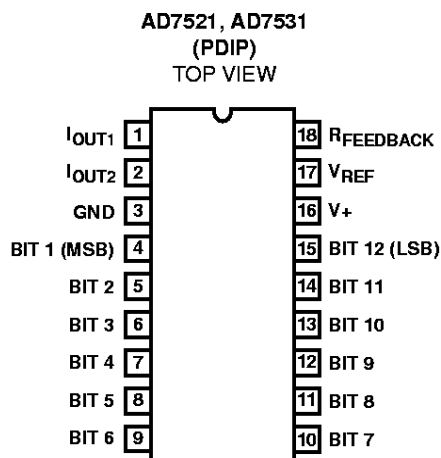
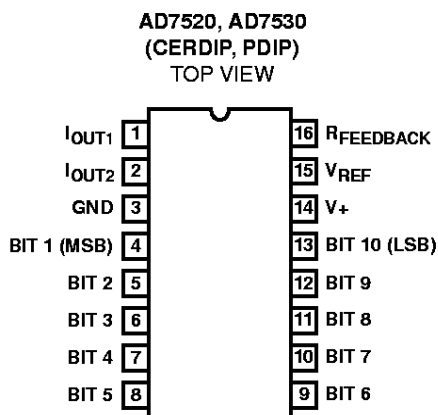
Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7520JN, AD7530JN	0.2% (8-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7520KN, AD7530KN	0.1% (9-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7521JN, AD7531JN	0.2% (8-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7521KN, AD7531KN	0.1% (9-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7520LN, AD7530LN	0.05% (10-Bit)	-40 to 85	16 Ld PDIP	E16.3
AD7521LN, AD7531LN	0.05% (10-Bit)	-40 to 85	18 Ld PDIP	E18.3
AD7520JD	0.2% (8-Bit)	-25 to 85	16 Ld Cerdip	F16.3
AD7520KD	0.1% (9-Bit)	-25 to 85	16 Ld Cerdip	F16.3
AD7520LD	0.05% (10-Bit)	-25 to 85	16 Ld Cerdip	F16.3
AD7520SD, AD7520SD/883B	0.2% (8-Bit)	-55 to 125	16 Ld Cerdip	F16.3
AD7520UD, AD7520UD/883B	0.05% (10-Bit)	-55 to 125	16 Ld Cerdip	F16.3

Pinouts



AD7520, AD7530, AD7521, AD7531

Absolute Maximum Ratings

Supply Voltage (V+ to GND)	+17V
V _{REF}	±25V
Digital Input Voltage Range	V+ to GND
Output Voltage Compliance	-100mV to V+

Operating Conditions

Temperature Ranges

JN, KN, LN Versions	0°C to 70°C
JD, KD, LD Versions	-25°C to 85°C
SD, UD Versions	-55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FEEDBACK}.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld PDIP Package	100	N/A
18 Ld PDIP Package	90	N/A
CERDIP Package	75	20
Maximum Junction Temperature (Hermetic Package)	175°C	
Maximum Junction Temperature (Plastic Packages)	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	

Electrical Specifications V+ = +15V, V_{REF} = +10V, T_A = 25°C Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE (Note 2)									
Resolution			10	10	10	12	12	12	Bits
Nonlinearity	J, S	S Over -55°C to 125°C (Notes 2, 5) (Figure 3)	-	-	±0.2 (8-Bit)	-	-	±0.2 (8-Bit)	% of FSR
	K	T Over -55°C to 125°C (Figure 2)	-	-	±0.1 (9-Bit)	-	-	±0.1 (9-Bit)	% of FSR
	L, U	-10V ≤ V _{REF} ≤ +10V U Over -55°C to 125°C (Figure 2)	-	-	±0.05 (10-Bit)	-	-	±0.05 (10-Bit)	% of FSR
Nonlinearity Tempco		-10V ≤ V _{REF} ≤ +10V (Notes 3, 4)	-	-	±2	-	-	±2	ppm of FSR/°C
Gain Error			-	±0.3	-	-	±0.3	-	% of FSR
Gain Error Tempco			-	-	±10	-	-	±10	ppm of FSR/°C
Output Leakage Current (Either Output)		Over the Specified Temperature Range	-	-	±200 (±300)	-	-	±200 (±300)	nA
DYNAMIC CHARACTERISTICS									
Output Current Settling Time		To 0.05% of FSR (All Digital Inputs Low To High And High To Low) (Note 4) (Figure 7)	-	1.0	-	-	1.0	-	μs
Feedthrough Error		V _{REF} = 20V _{P-P} , 10kHz (50kHz) All Digital Inputs Low (Note 4) (Figure 6)	-	-	10	-	-	10	mV _{P-P}
REFERENCE INPUT									
Input Resistance		All Digital Inputs High I _{OUT1} at Ground	5	10	20	5	10	20	kΩ
ANALOG OUTPUT									
Output Capacitance	I _{OUT1}	All Digital Inputs High (Note 4) (Figure 5)	-	200	-	-	200	-	pF
	I _{OUT2}		-	75	-	-	75	-	pF
	I _{OUT1}	All Digital Inputs Low (Note 4) (Figure 5)	-	75	-	-	75	-	pF
	I _{OUT2}		-	200	-	-	200	-	pF

AD7520, AD7530, AD7521, AD7531

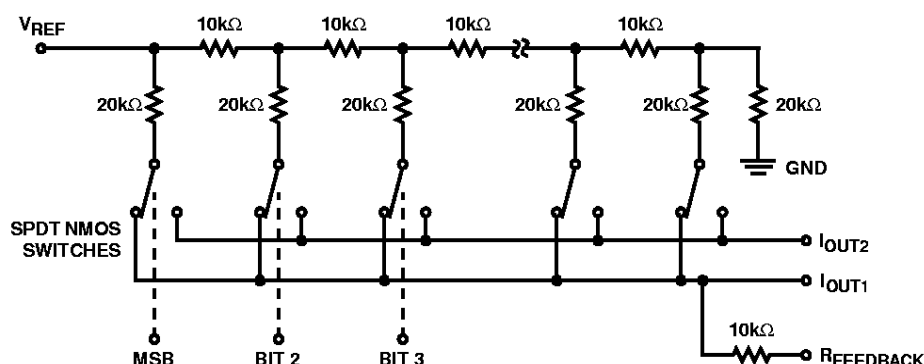
Electrical Specifications $V_+ = +15V$, $V_{REF} = +10V$, $T_A = 25^\circ C$ Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Noise	Both Outputs (Note 4) (Figure 4)	-	Equivalent to 10kΩ	-	-	Equivalent to 10kΩ	-	Johnson Noise
DIGITAL INPUTS								
Low State Threshold, V _{IL}	Over the Specified Temperature Range V _{IN} = 0V or +15V	-	-	0.8	-	-	0.8	V
High State Threshold, V _{IH}		2.4	-	-	2.4	-	-	V
Input Current, I _{IL} , I _{IH}		-	-	±1	-	-	±1	μA
Input Coding	See Tables 1 and 2	Binary/Offset Binary						
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection	V+ = 14.5V to 15.5V (Note 3) (Figure 3)	-	±0.005	-	-	±0.005	-	% FSR/ % ΔV+
Power Supply Voltage Range		+5 to +15			+5 to +15			V
I+	All Digital Inputs at 0V or V+ Excluding Ladder Network	-	±1	-	-	±1	-	μA
	All Digital Inputs High or Low Excluding Ladder Network	-	-	2	-	-	2	mA
Total Power Dissipation	Including the Ladder Network	-	20	-	-	20	-	mW

NOTES:

- Full scale range (FSR) is 10V for Unipolar and $\pm 10V$ for Bipolar modes.
- Using internal feedback resistor $R_{FEEDBACK}$.
- Guaranteed by design, or characterization and not production tested.
- Accuracy not guaranteed unless outputs at GND potential.
- Accuracy is tested and guaranteed at $V_+ = 15V$ only.

Functional Diagram



NOTES:

- Switches shown for Digital Inputs "High".
Resistor values are typical.

Pin Descriptions

AD7520/30	AD7521/31	PIN NAME	DESCRIPTION
1	1	IOUT1	Current Out summing junction of the R2R ladder network.
2	2	IOUT2	Current Out virtual ground, return path for the R2R ladder network.
3	3	GND	Digital Ground. Ground potential for digital side of D/A.
4	4	Bits 1(MSB)	Most Significant Digital Data Bit.
5	5	Bit 2	Digital Bit 2.
6	6	Bit 3	Digital Bit 3.
7	7	Bit 4	Digital Bit 4.
8	8	Bit 5	Digital Bit 5.
9	9	Bit 6	Digital Bit 6.
10	10	Bit 7	Digital Bit 7.
11	11	Bit 8	Digital Bit 8.
12	12	Bit 9	Digital Bit 9.
13	13	Bit 10	Digital Bit 10 (AD7521/31). Least Significant Digital Data Bit (AD7520/30).
-	14	Bit 11	Digital Bit 11 (AD7521/31).
-	15	Bit 12	Least Significant Digital Data Bit (AD7521/31).
14	16	V+	Power Supply +5V to +15V.
15	17	VREF	Voltage Reference Input to set the output range. Supplies the R2R resistor ladder.
16	18	RFEEDBACK	Feedback resistor used for the current to voltage conversion when using an external Op Amp.

Definition of Terms

Nonlinearity: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

Resolution: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-N} of the full-scale range, e.g., $2^{-N} V_{REF}$ for a unipolar conversion. Resolution by no means implies linearity.

Settling Time: Time required for the output of a DAC to settle to within specified error band around its final value (e.g., $1/2$ LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

Gain Error: The difference between actual and ideal analog output values at full scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

Output Capacitance: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

Output Leakage Current: Current which appears on I_{OUT1} terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

Detailed Description

The AD7520, AD7530, AD7521 and AD7531 are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage

or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in the Functional Diagram. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduce offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with positive feedback from the output of the second to the first, see Figure 1. This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binary weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

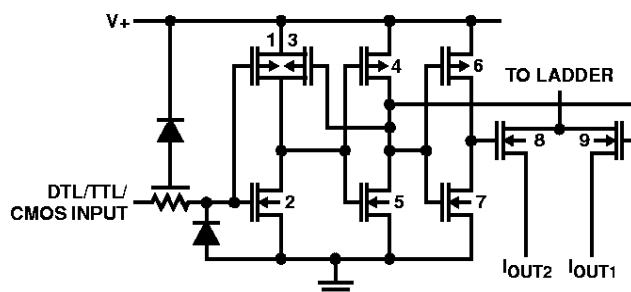


FIGURE 1. CMOS SWITCH