

# Dual/Quad Low Noise, High Speed Precision Op Amps

## FEATURES

- 100% Tested Low Voltage Noise:  $2.7\text{nV}/\sqrt{\text{Hz}}$  Typ  
 $4.2\text{nV}/\sqrt{\text{Hz}}$  Max
- Slew Rate:  $4.5\text{V}/\mu\text{s}$  Typ
- Gain Bandwidth Product:  $12.5\text{MHz}$  Typ
- Offset Voltage, Prime Grade:  $70\mu\text{V}$  Max  
Low Grade:  $100\mu\text{V}$  Max
- High Voltage Gain: 5 Million Min
- Supply Current Per Amplifier:  $2.75\text{mA}$  Max
- Common Mode Rejection:  $112\text{dB}$  Min
- Power Supply Rejection:  $116\text{dB}$  Min
- Available in 8-Pin SO Package

## APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Infrared Detectors

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## DESCRIPTION

The LT<sup>®</sup>1124 dual and LT1125 quad are high performance op amps that offer higher gain, slew rate and bandwidth than the industry standard OP-27 and competing OP-270/OP-470 op amps. In addition, the LT1124/LT1125 have lower  $I_B$  and  $I_{OS}$  than the OP-27; lower  $V_{OS}$  and noise than the OP-270/OP-470.

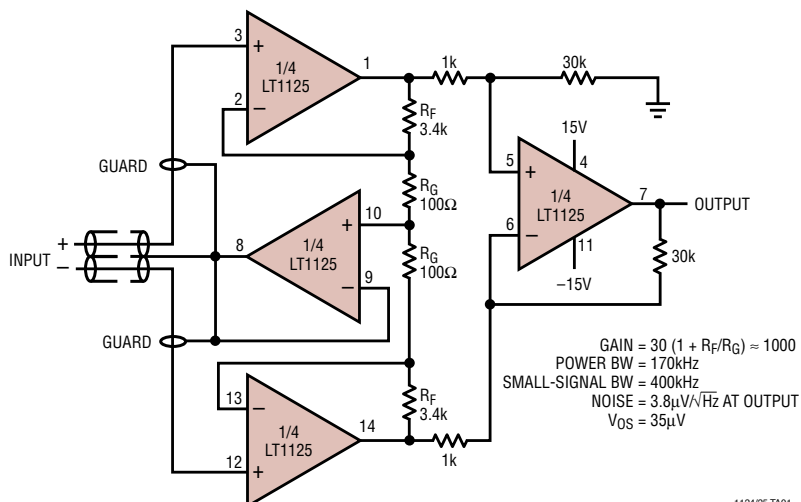
In the design, processing and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Slew rate, gain bandwidth and  $1\text{kHz}$  noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the LT1124C and the LT1125C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

Power consumption of the LT1124 is one half of two OP-27s. Low power and high performance in an 8-pin SO package make the LT1124 a first choice for surface mounted systems and where board space is restricted.

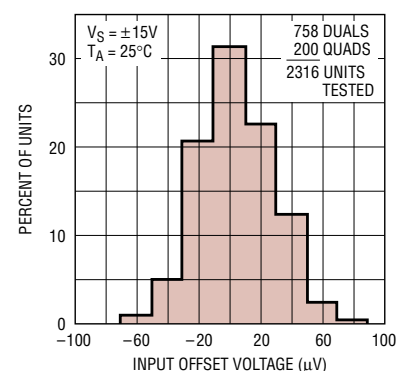
For a decompensated version of these devices, with three times higher slew rate and bandwidth, please see the LT1126/LT1127 data sheet.

## TYPICAL APPLICATION

Instrumentation Amplifier with Shield Driver



Input Offset Voltage Distribution (All Packages, LT1124 and LT1125)



1124/25 TA01

1124/25 TA02

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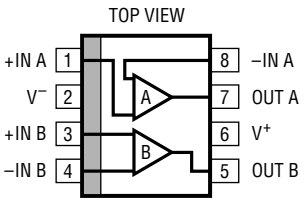
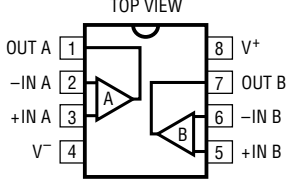
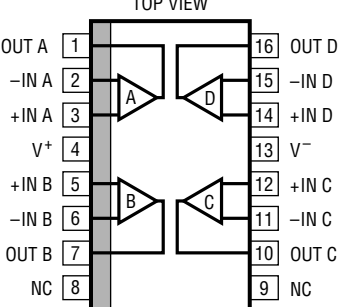
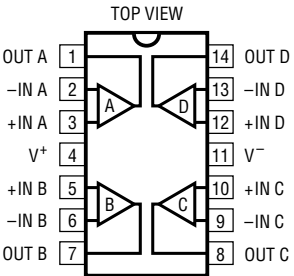
# LT1124/LT1125

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .....  $\pm 22\text{V}$   
 Input Voltages ..... Equal to Supply Voltage  
 Output Short-Circuit Duration ..... Indefinite  
 Differential Input Current (Note 6) .....  $\pm 25\text{mA}$   
 Lead Temperature (Soldering, 10 sec) .....  $300^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $150^\circ\text{C}$

Operating Temperature Range  
 LT1124AC/LT1124C  
 LT1125AC/LT1125C (Note 10) .....  $-40^\circ\text{C}$  to  $85^\circ\text{C}$   
 LT1124AI/LT1124I .....  $-40^\circ\text{C}$  to  $85^\circ\text{C}$   
 LT1124AM/LT1124M  
 LT1125AM/LT1125M **OBSOLETE** ....  $-55^\circ\text{C}$  to  $125^\circ\text{C}$

## PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p>1 +IN A, 2 V<sup>-</sup>, 3 +IN B, 4 -IN B, 5 OUT B, 6 V<sup>+</sup>, 7 OUT A, 8 -IN A</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 140^\circ\text{C}</math>, <math>\theta_{JA} = 190^\circ\text{C/W}</math></p> <p>NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN PDIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE PIN LOCATIONS</p>	<p>ORDER PART NUMBER</p> <p>LT1124CS8 LT1124AIS8 LT1124IS8</p> <p>S8 PART MARKING</p> <p>1124 1124AI 1124I</p>	 <p>TOP VIEW</p> <p>1 OUT A, 2 -IN A, 3 +IN A, 4 V<sup>-</sup>, 5 +IN B, 6 -IN B, 7 OUT B, 8 V<sup>+</sup></p> <p>N8 PACKAGE 8-LEAD PDIP <math>T_{JMAX} = 140^\circ\text{C}</math>, <math>\theta_{JA} = 130^\circ\text{C/W}</math></p> <p>J8 PACKAGE 8-LEAD CERAMIC DIP <math>T_{JMAX} = 160^\circ\text{C}</math>, <math>\theta_{JA} = 100^\circ\text{C/W}</math>  <b>OBSOLETE PACKAGE</b>                  Consider the N8 for Alternative Source</p>	<p>ORDER PART NUMBER</p> <p>LT1124ACN8 LT1124CN8</p> <p>LT1124CJ8 LT1124AMJ8 LT1124MJ8</p>
 <p>TOP VIEW</p> <p>1 OUT A, 2 -IN A, 3 +IN A, 4 V<sup>+</sup>, 5 +IN B, 6 -IN B, 7 OUT B, 8 NC, 9 NC, 10 OUT C, 11 -IN C, 12 +IN C, 13 V<sup>-</sup>, 14 +IN D, 15 -IN D, 16 OUT D</p> <p>SW PACKAGE 16-LEAD PLASTIC SO WIDE <math>T_{JMAX} = 140^\circ\text{C}</math>, <math>\theta_{JA} = 130^\circ\text{C/W}</math></p>	<p>LT1125CSW</p>	 <p>TOP VIEW</p> <p>1 OUT A, 2 -IN A, 3 +IN A, 4 V<sup>+</sup>, 5 +IN B, 6 -IN B, 7 OUT B, 8 OUT C, 9 -IN C, 10 +IN C, 11 V<sup>-</sup>, 12 +IN D, 13 -IN D, 14 OUT D</p> <p>N PACKAGE 14-LEAD PDIP <math>T_{JMAX} = 140^\circ\text{C}</math>, <math>\theta_{JA} = 110^\circ\text{C/W}</math> (N)</p> <p>J PACKAGE 14-LEAD CERAMIC DIP <math>T_{JMAX} = 160^\circ\text{C}</math>, <math>\theta_{JA} = 80^\circ\text{C/W}</math>  <b>OBSOLETE PACKAGE</b>                  Consider the N for Alternative Source</p>	<p>LT1125ACN LT1125CN</p> <p>LT1125CJ LT1125AMJ LT1125MJ</p>
<p><b>Order Options</b> Tape and Reel: Add #TR                  Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF                  Lead Free Part Marking: <a href="http://www.linear.com/leadfree/">http://www.linear.com/leadfree/</a></p>			

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1124AC/AI/AM LT1125AC/AM			LT1124C/I/M LT1125C/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1124	20	70		25	100	$\mu\text{V}$	
		LT1125	25	90		30	140	$\mu\text{V}$	
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long-Term Input Offset Voltage Stability		0.3			0.3		$\mu\text{V}/\text{Mo}$	
$I_{OS}$	Input Offset Current	LT1124	5	15		6	20	nA	
		LT1125	6	20		7	30	nA	
$I_B$	Input Bias Current		$\pm 7$	$\pm 20$		$\pm 8$	$\pm 30$	nA	
$e_n$	Input Noise Voltage	0.1Hz to 10Hz (Notes 8, 9)	70	200		70		nV <sub>p-p</sub>	
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Note 5)	3.0	5.5		3.0	5.5	nV/ $\sqrt{\text{Hz}}$	
		$f_0 = 1000\text{Hz}$ (Note 3)	2.7	4.2		2.7	4.2	nV/ $\sqrt{\text{Hz}}$	
$i_n$	Input Noise Current Density	$f_0 = 10\text{Hz}$	1.3			1.3		pA/ $\sqrt{\text{Hz}}$	
		$f_0 = 1000\text{Hz}$	0.3			0.3		pA/ $\sqrt{\text{Hz}}$	
$V_{CM}$	Input Voltage Range		$\pm 12$	$\pm 12.8$		$\pm 12$	$\pm 12.8$	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	112	126		106	124	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	116	126		110	124	dB	
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 10\text{k}$ , $V_{OUT} = \pm 10\text{V}$	5	17		3.0	15	V/ $\mu\text{V}$	
		$R_L \geq 2\text{k}$ , $V_{OUT} = \pm 10\text{V}$	2	4		1.5	3	V/ $\mu\text{V}$	
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	$\pm 13$	$\pm 13.8$		$\pm 12.5$	$\pm 13.8$	V	
SR	Slew Rate	$R_L \geq 2\text{k}$ (Notes 3, 7)	3	4.5		2.7	4.5	V/ $\mu\text{s}$	
GBW	Gain Bandwidth Product	$f_0 = 100\text{kHz}$ (Note 3)	9	12.5		8	12.5	MHz	
$Z_0$	Open-Loop Output Resistance	$V_{OUT} = 0$ , $I_{OUT} = 0$	75			75		$\Omega$	
$I_S$	Supply Current per Amplifier		2.3	2.75		2.3	2.75	mA	
		Channel Separation	$f \leq 10\text{Hz}$ (Note 9) $V_{OUT} = \pm 10\text{V}$ , $R_L = 2\text{k}$	134	150		130	150	dB

The ● denotes the specifications which apply over the  $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$  temperature range,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1124AM LT1125AM			LT1124M LT1125M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1124	●	50	170		60	250	$\mu\text{V}$
		LT1125	●	55	190		70	290	$\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 5)	●	0.3	1.0		0.4	1.5	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current	LT1124	●	18	45		20	60	nA
		LT1125	●	18	55		20	70	nA
$I_B$	Input Bias Current		●	$\pm 18$	$\pm 55$		$\pm 20$	$\pm 70$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.3$	$\pm 12$		$\pm 11.3$	$\pm 12$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.3\text{V}$	●	106	122		100	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	●	110	122		104	120	dB
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 10\text{k}$ , $V_{OUT} = \pm 10\text{V}$	●	3	10		2.0	10	V/ $\mu\text{V}$
		$R_L \geq 2\text{k}$ , $V_{OUT} = \pm 10\text{V}$	●	1	3		0.7	2	V/ $\mu\text{V}$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	●	$\pm 12.5$	$\pm 13.6$		$\pm 12$	$\pm 13.6$	V
SR	Slew Rate	$R_L \geq 2\text{k}$ (Notes 3, 7)	●	2.3	3.8		2	3.8	V/ $\mu\text{s}$
$I_S$	Supply Current per Amplifier		●	2.5	3.25		2.5	3.25	mA

# LT1124/LT1125

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$  temperature range,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1124AC LT1125AC			LT1124C LT1125C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1124 LT1125	● ●		35	120		45	170	$\mu\text{V}$
					40	140		50	210	$\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 5)	●		0.3	1		0.4	1.5	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current	LT1124 LT1125	● ●		6	25		7	35	nA
					7	35		8	45	nA
$I_B$	Input Bias Current		●		$\pm 8$	$\pm 35$		$\pm 9$	$\pm 45$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.5$	$\pm 12.4$		$\pm 11.5$	$\pm 12.4$		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.5\text{V}$	●	109	125		102	122		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	●	112	125		107	122		dB
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 10\text{k}$ , $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{k}$ , $V_{OUT} = \pm 10\text{V}$	● ●		4.0	15		2.5	14	$\text{V}/\mu\text{V}$
					1.5	3.5		1.0	2.5	$\text{V}/\mu\text{V}$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	●	$\pm 12.5$	$\pm 13.7$		$\pm 12$	$\pm 13.7$		V
SR	Slew Rate	$R_L \geq 2\text{k}$ (Notes 3, 7)	●	2.6	4		2.4	4		$\text{V}/\mu\text{s}$
$I_S$	Supply Current per Amplifier		●		2.4	3		2.4	3	mA

The ● denotes the specifications which apply over the  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  temperature range,  $V_S = \pm 15\text{V}$ , unless otherwise noted. (Note 10)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1124AC/AI LT1125AC			LT1124C/I LT1125C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1124 LT1125	● ●		40	140		50	200	$\mu\text{V}$
					45	160		55	240	$\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 5)	●		0.3	1		0.4	1.5	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current	LT1124 LT1125	● ●		15	40		17	55	nA
					15	50		17	65	nA
$I_B$	Input Bias Current		●		$\pm 15$	$\pm 50$		$\pm 17$	$\pm 65$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.4$	$\pm 12.2$		$\pm 11.4$	$\pm 12.2$		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.4\text{V}$	●	107	124		101	121		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	●	111	124		106	121		dB
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 10\text{k}$ , $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{k}$ , $V_{OUT} = \pm 10\text{V}$	● ●		3.5	12		2.2	12	$\text{V}/\mu\text{V}$
					1.2	3.2		0.8	2.3	$\text{V}/\mu\text{V}$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	●	$\pm 12.5$	$\pm 13.6$		$\pm 12$	$\pm 13.6$		V
SR	Slew Rate	$R_L \geq 2\text{k}$ (Notes 3, 7)	●	2.4	3.9		2.1	3.9		$\text{V}/\mu\text{s}$
$I_S$	Supply Current per Amplifier		●		2.4	3.25		2.4	3.25	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1125s (or 100 LT1124s) typically 240 op amps (or 120) will be better than the indicated specification.

**Note 3:** This parameter is 100% tested for each individual amplifier.

**Note 4:** This parameter is sample tested only.

**Note 5:** This parameter is not 100% tested.

**Note 6:** The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds  $\pm 1.4\text{V}$ , the input current should be limited to 25mA.

**Note 7:** Slew rate is measured in  $A_V = -1$ ; input signal is  $\pm 7.5\text{V}$ , output measured at  $\pm 2.5\text{V}$ .

**Note 8:** 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 data sheets.

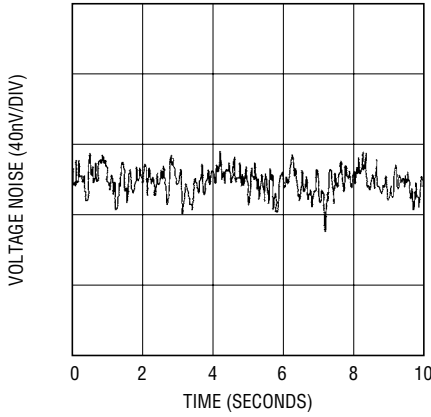
**Note 9:** This parameter is guaranteed but not tested.

**Note 10:** The LT1124C/LT1125C and LT1124AC/LT1125AC are guaranteed to meet specified performance from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  and are designed, characterized and expected to meet these extended temperature limits, but are not tested at  $-40^{\circ}\text{C}$  and  $85^{\circ}\text{C}$ . The LT1124AI and LT1124I are guaranteed to meet the extended temperature limits.

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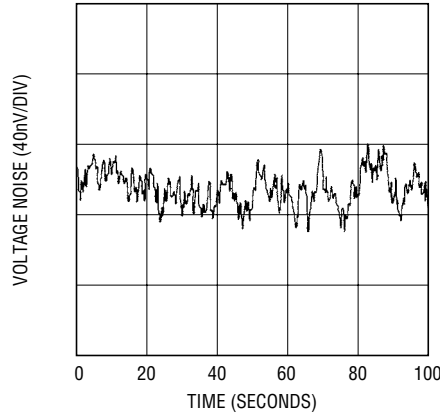
# TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Voltage Noise



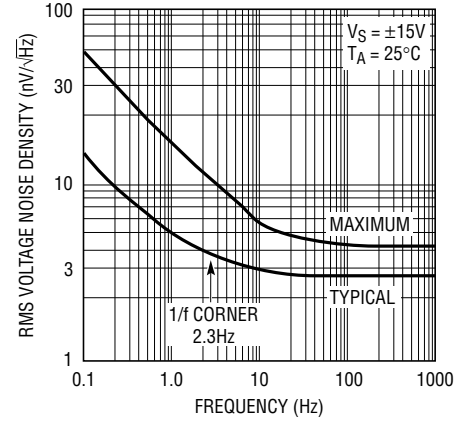
1124/25 G01

0.01Hz to 1Hz Voltage Noise



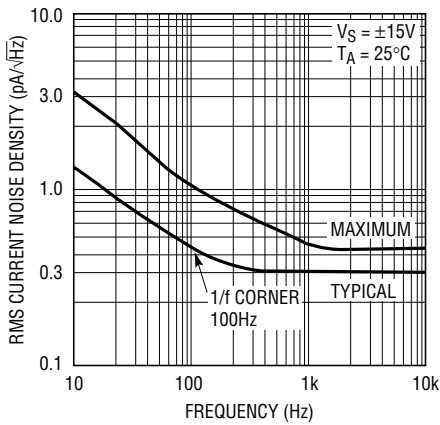
1124/25 G02

Voltage Noise vs Frequency



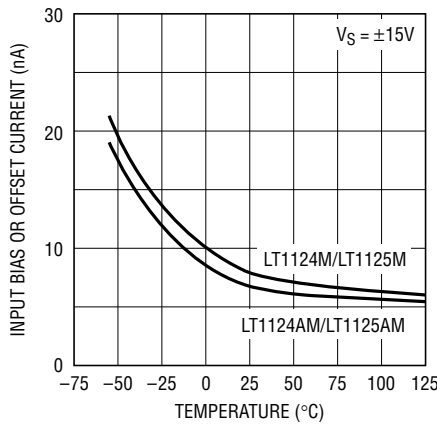
1124/25 G03

Current Noise vs Frequency



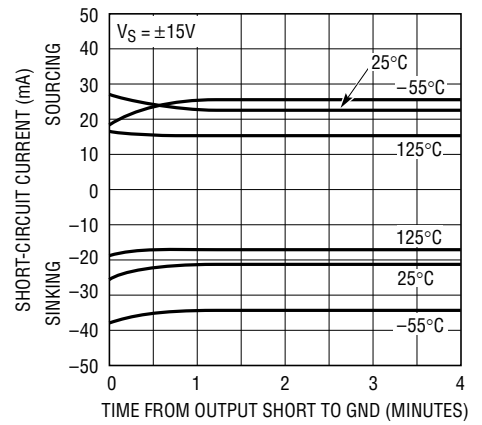
1124 G04

Input Bias or Offset Current vs Temperature



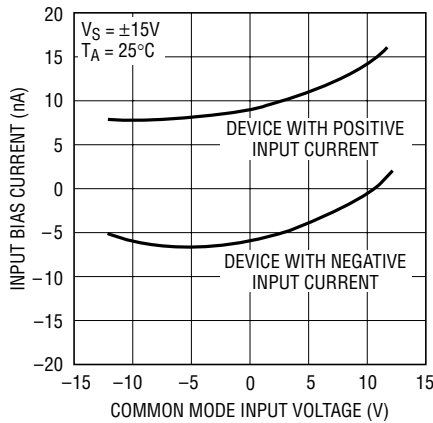
1124/25 G05

Output Short-Circuit Current vs Time



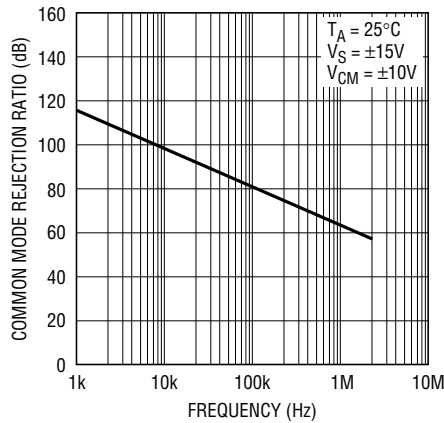
LT1124 G06

Input Bias Current Over the Common Mode Range



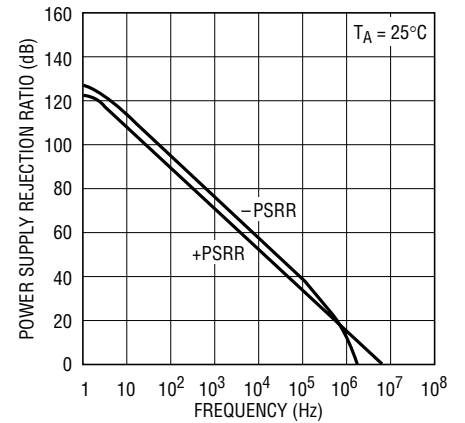
1124/25 G07

Common Mode Rejection Ratio vs Frequency



1124/25 G08

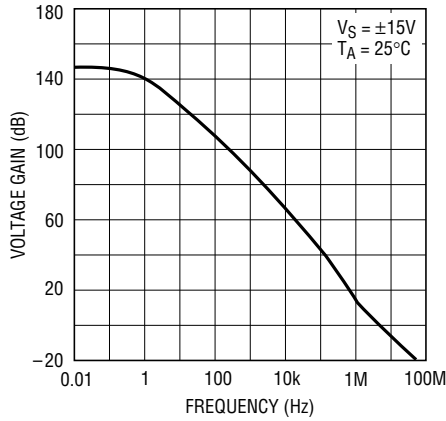
Power Supply Rejection Ratio vs Frequency



1124/25 G09

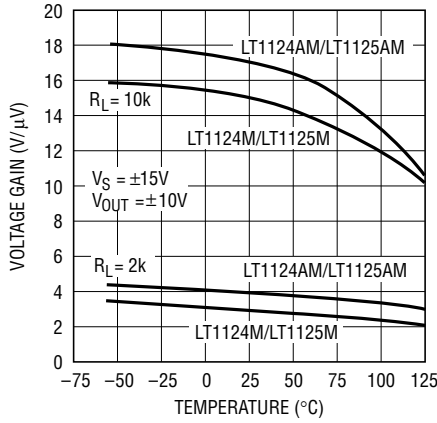
# TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain vs Frequency



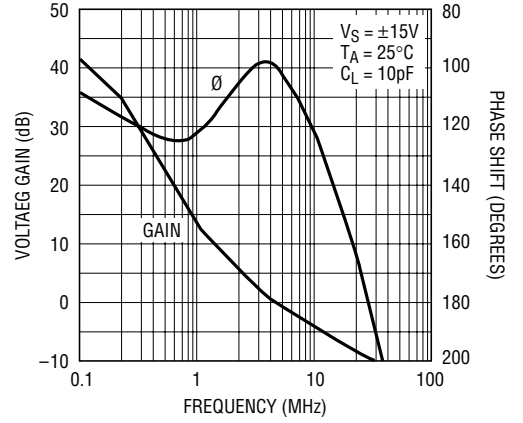
1124/25 G10

Voltage Gain vs Temperature



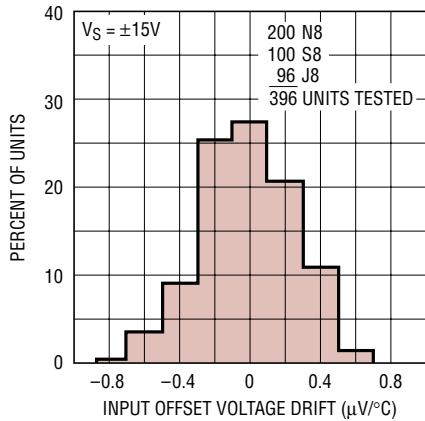
1124/25 G11

Gain, Phase Shift vs Frequency



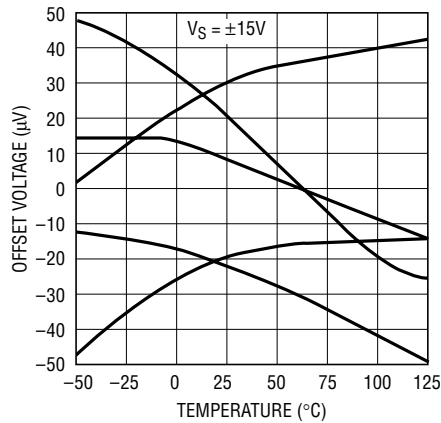
1124/25 G12

Input Offset Voltage Drift Distribution



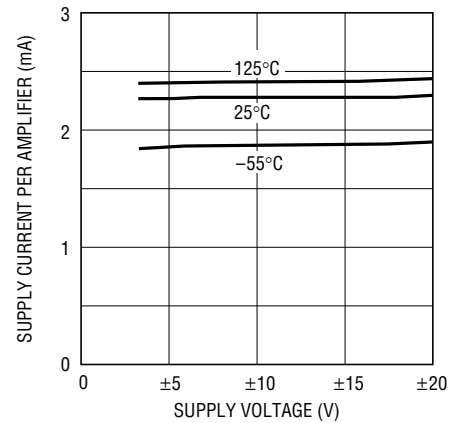
1124/25 G13

Offset Voltage Drift with Temperature of Representative Units



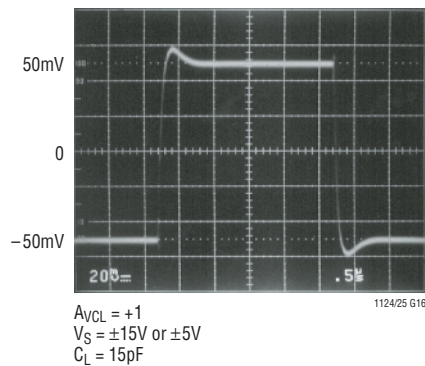
1124/25 G14

Supply Current vs Supply Voltage



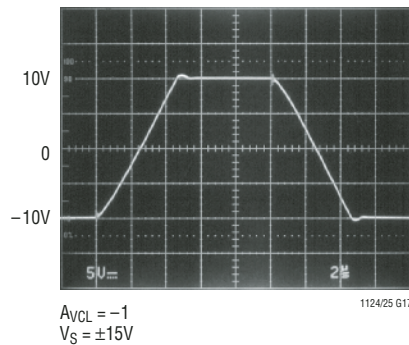
1124/25 G15

Small-Signal Transient Response



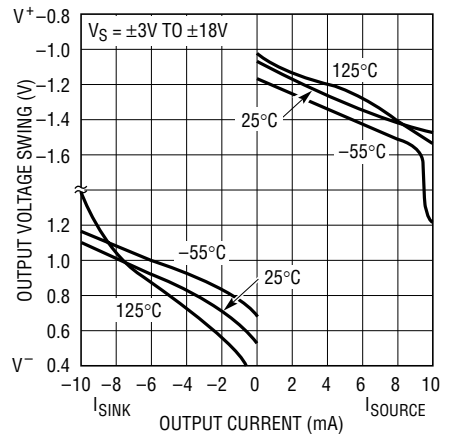
1124/25 G16

Large-Signal Transient Response



1124/25 G17

Output Voltage Swing vs Load Current

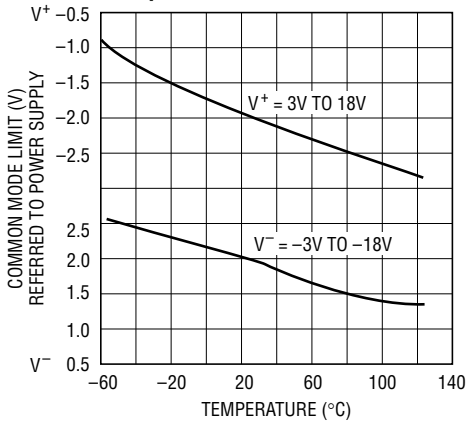


1124/25 G18

11245fb

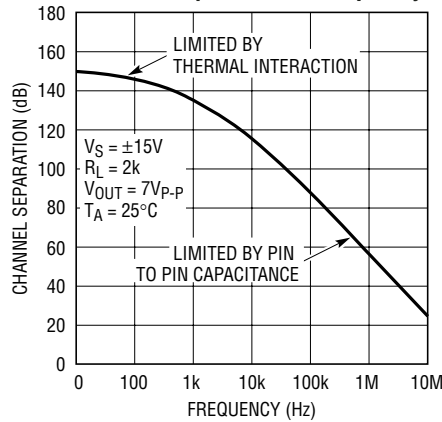
# TYPICAL PERFORMANCE CHARACTERISTICS

**Common Mode Limit vs Temperature**



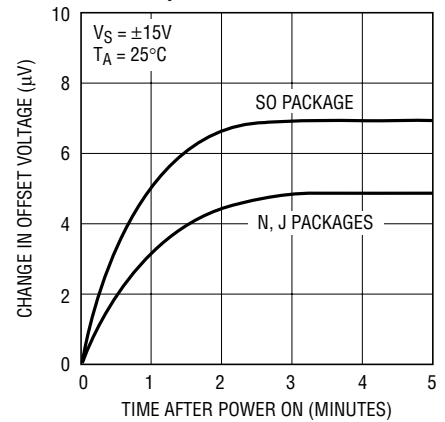
1124/25 G19

**Channel Separation vs Frequency**



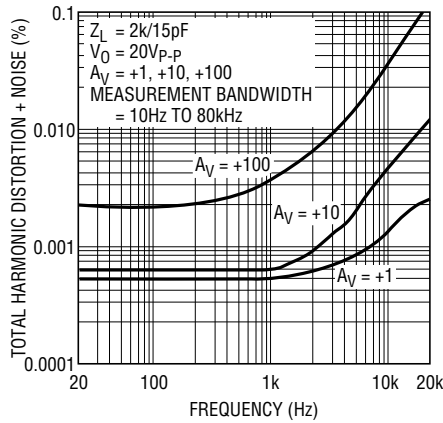
1124/25 G20

**Warm-Up Drift**



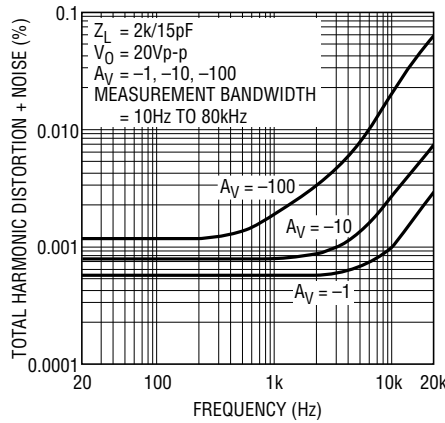
1124/25 G21

**Total Harmonic Distortion and Noise vs Frequency for Noninverting Gain**



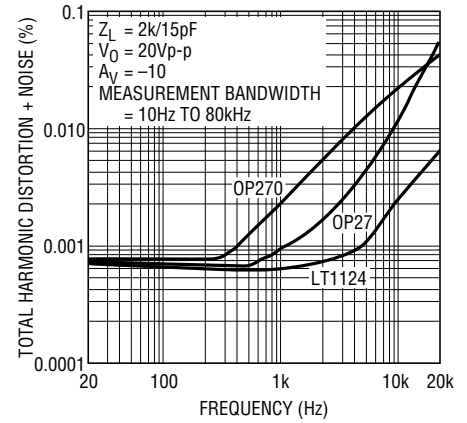
1124/25 G22

**Total Harmonic Distortion and Noise vs Frequency for Inverting Gain**



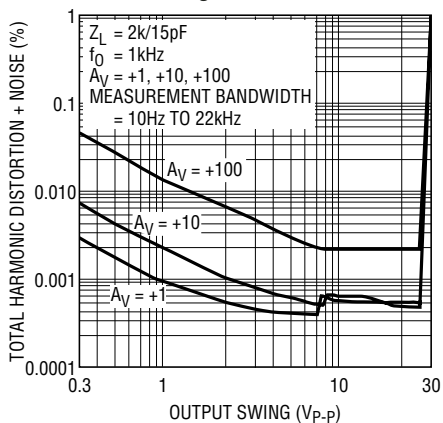
1124/25 G23

**Total Harmonic Distortion and Noise vs Frequency for Competitive Devices**



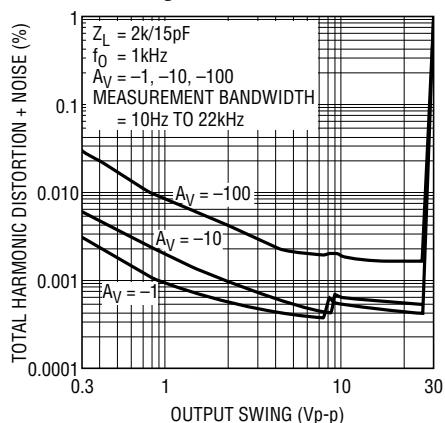
1124/25 G24

**Total Harmonic Distortion and Noise vs Output Amplitude for Noninverting Gain**



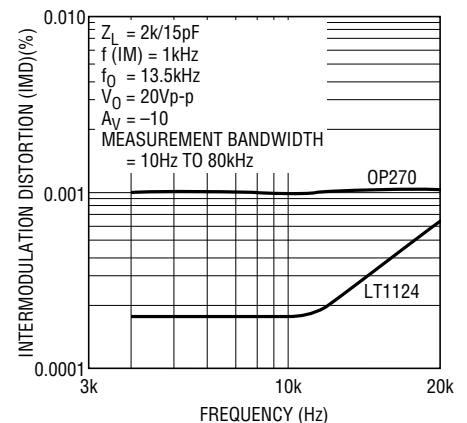
1124/25 G25

**Total Harmonic Distortion and Noise vs Output Amplitude for Inverting Gain**



1124/25 G26

**Intermodulation Distortion (CCIF Method)\* vs Frequency LT1124 and OP270**



1124/25 G27

\*See LT1115 data sheet for definition of CCIF testing

## APPLICATIONS INFORMATION

The LT1124 may be inserted directly into OP-270 sockets. The LT1125 plugs into OP-470 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

### Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1124/LT1125.

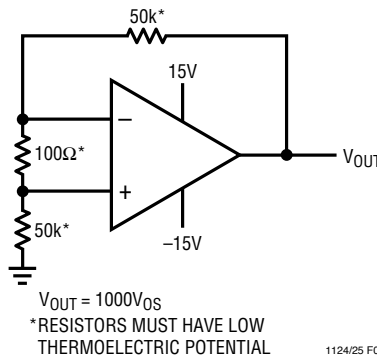
Some specifications are guaranteed by definition. For example, 70 $\mu$ V maximum offset voltage implies that mismatch cannot be more than 140 $\mu$ V. 112dB (= 2.5 $\mu$ V/V) CMRR means that worst case CMRR match is 106dB

(5 $\mu$ V/V). However, Table 1 can be used to estimate the expected matching performance between the two sides of the LT1124, and between amplifiers A and D, and between amplifiers B and C of the LT1125.

### Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown in Figure 1 to measure offset voltage is also used as the burn-in configuration for the LT1124/LT1125, with the supply voltages increased to  $\pm 16$ V.



**Figure 1. Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature**

**Table 1. Expected Match**

PARAMETER		LT1124AC/AM LT1125AC/AM		LT1124C/M LT1125C/M		UNITS
		50% YIELD	98% YIELD	50% YIELD	98% YIELD	
$V_{OS}$ Match, $\Delta V_{OS}$	LT1124	20	110	30	130	$\mu$ V
	LT1125	30	150	50	180	$\mu$ V
Temperature Coefficient Match		0.35	1.0	0.5	1.5	$\mu$ V/ $^{\circ}$ C
Average Noninverting $I_B$		6	18	7	25	nA
Match of Noninverting $I_B$		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB



## APPLICATIONS INFORMATION

### High Speed Operation

When the feedback around the op amp is resistive ( $R_F$ ), a pole will be created with  $R_F$ , the source resistance and capacitance ( $R_S$ ,  $C_S$ ), and the amplifier input capacitance ( $C_{IN} \approx 2\text{pF}$ ). In low closed loop gain configurations and with  $R_S$  and  $R_F$  in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor ( $C_F$ ) in parallel with  $R_F$  eliminates this problem (see Figure 2). With  $R_S (C_S + C_{IN}) = R_F C_F$ , the effect of the feedback pole is completely removed.

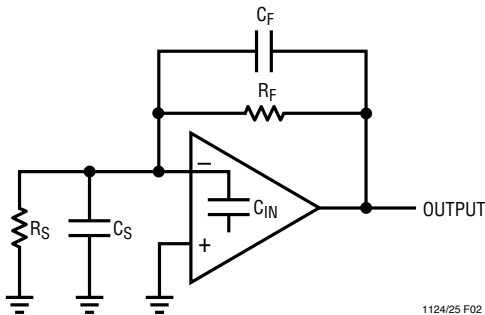


Figure 2. High Speed Operation

### Unity Gain Buffer Applications

When  $R_F \leq 100\Omega$  and the input is driven with a fast, large signal pulse ( $>1\text{V}$ ), the output waveform will look as shown in Figure 3.

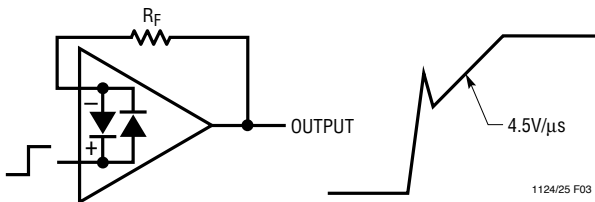


Figure 3. Unity-Gain Buffer Applications

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With  $R_F \geq 500\Omega$ , the output is capable of handling the current requirements ( $I_L \leq 20\text{mA}$  at  $10\text{V}$ ) and the amplifier stays in its active mode and a smooth transition will occur.

### Noise Testing

Each individual amplifier is tested to  $4.2\text{nV}/\sqrt{\text{Hz}}$  voltage noise; i.e., for the LT1124 two tests, for the LT1125 four tests are performed. Noise testing for competing multiple op amps, if done at all, may be sample tested or tested using the circuit shown in Figure 4.

$$e_{n\text{ OUT}} = \sqrt{(e_{nA})^2 + (e_{nB})^2 + (e_{nC})^2 + (e_{nD})^2}$$

If the LT1125 were tested this way, the noise limit would be  $\sqrt{4 \cdot (4.2\text{nV}/\sqrt{\text{Hz}})^2} = 8.4\text{nV}/\sqrt{\text{Hz}}$ . But is this an effective screen? What if three of the four amplifiers are at a typical  $2.7\text{nV}/\sqrt{\text{Hz}}$ , and the fourth one was contaminated and has  $6.9\text{nV}/\sqrt{\text{Hz}}$  noise?

$$\text{RMS Sum} = \sqrt{(2.7)^2 + (2.7)^2 + (2.7)^2 + (6.9)^2} = 8.33\text{nV}/\sqrt{\text{Hz}}$$

This passes an  $8.4\text{nV}/\sqrt{\text{Hz}}$  spec, yet one of the amplifiers is 64% over the LT1125 spec limit. Clearly, for proper noise measurement, the op amps have to be tested individually.

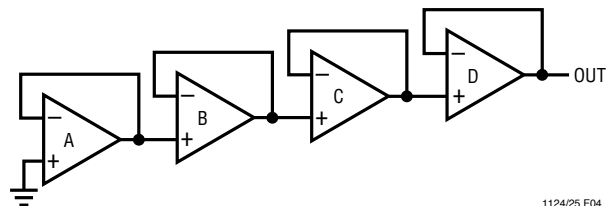


Figure 4. Competing Quad Op Amp Noise Test Method

## PERFORMANCE COMPARISON

Table 2 summarizes the performance of the LT1124/LT1125 compared to the low cost grades of alternate approaches.

but in most cases are superior. Normally dual and quad performance is degraded when compared to singles, for the LT1124/LT1125 this is not the case.

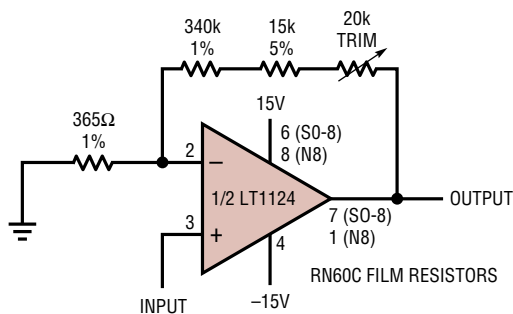
The comparison shows how the specs of the LT1124/LT1125 not only stand up to the industry standard OP-27,

**Table 2. Guaranteed Performance,  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , Low Cost Devices**

PARAMETER/UNITS		LT1124CN8 LT1125CN	OP-27 GP	OP-270 GP	OP-470 GP	UNITS
Voltage Noise, 1kHz		4.2 100% Tested	4.5 Sample Tested	– No Limit	5.0 Sample Tested	$nV/\sqrt{Hz}$
Slew Rate		2.7 100% Tested	1.7 Not Tested	1.7	1.4	$V/\mu s$
Gain Bandwidth Product		8.0 100% Tested	5.0 Not Tested	– No Limit	– No Limit	MHz
Offset Voltage	LT1124	100	100	250	–	$\mu V$
	LT1125	140	–	–	1000	$\mu V$
Offset Current	LT1124	20	75	20	–	nA
	LT1125	30	–	–	30	nA
Bias Current		30	80	60	60	nA
Supply Current/Amp		2.75	5.67	3.25	2.75	mA
Voltage Gain, $R_L = 2k$		1.5	0.7	0.35	0.4	$V/\mu V$
Common Mode Rejection Ratio		106	100	90	100	dB
Power Supply Rejection Ratio		110	94	104	105	dB
SO-8 Package		Yes - LT1124	Yes	No	–	

## TYPICAL APPLICATIONS

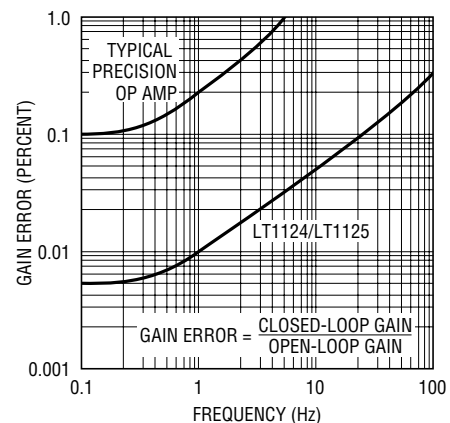
**Gain 1000 Amplifier with 0.01% Accuracy, DC to 1Hz**



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1124/LT1125, IS USEFUL IN LOW FREQUENCY HIGH CLOSED-LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN-LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1124/LT1125 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 75 TIMES HIGHER, AS SHOWN.

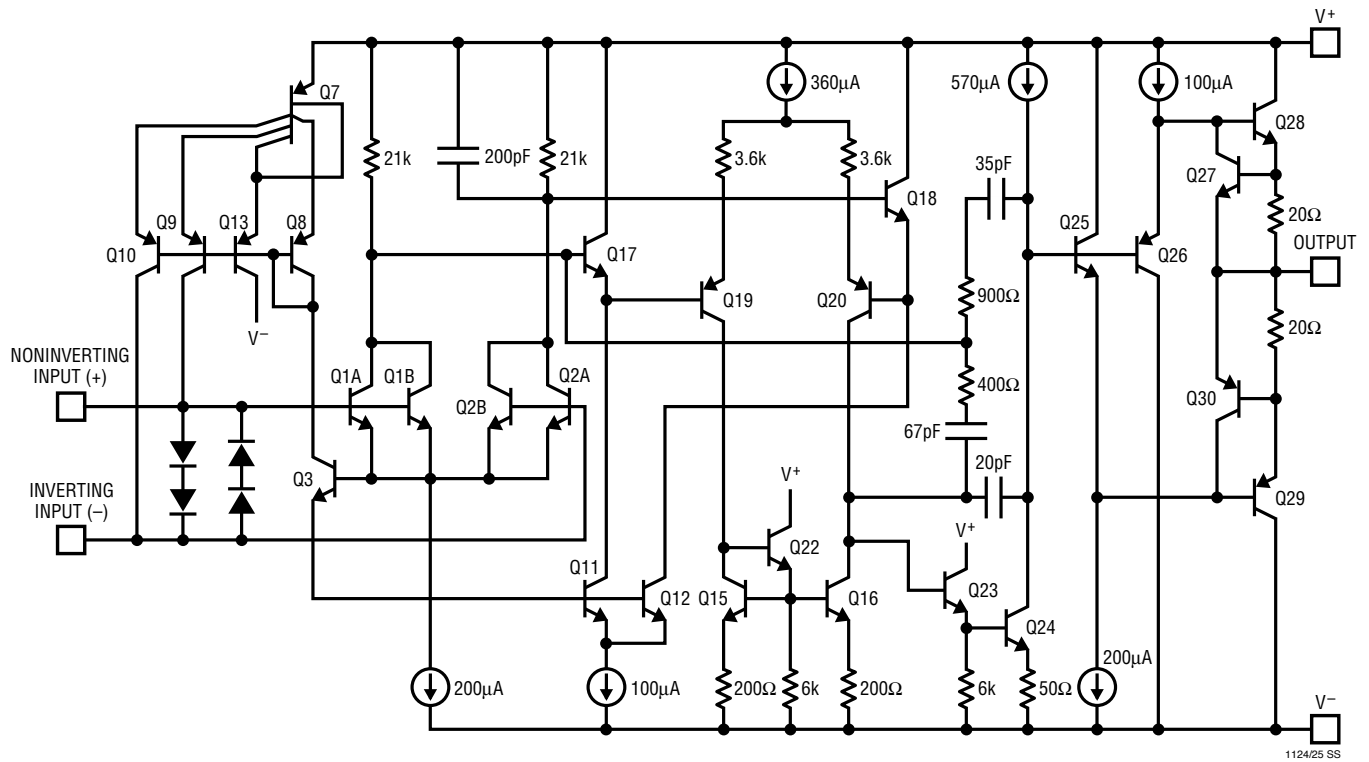
1124/25 TA03

**Gain Error vs Frequency Closed-Loop Gain = 1000**



1124/25 TA04

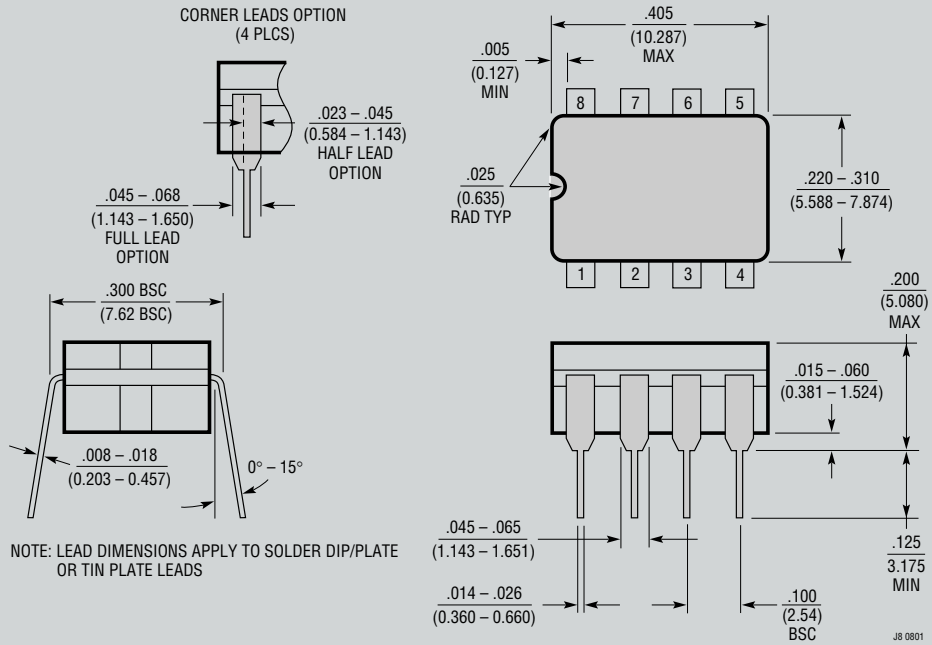
**SCHEMATIC DIAGRAM** (1/2 LT1124, 1/4 LT1125)



1124/25 SS

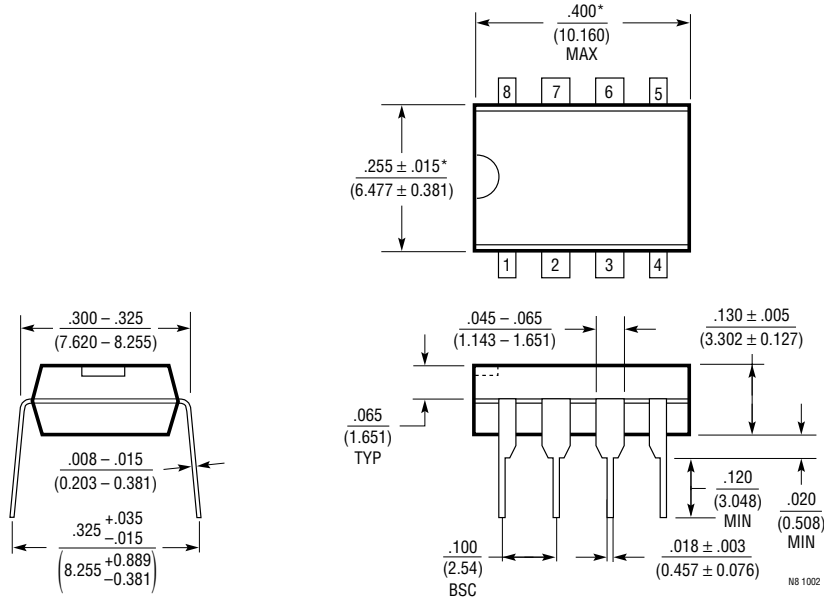
**PACKAGE DESCRIPTION**

**J8 Package**  
**8-Lead CERDIP (Narrow 0.300, Hermetic)**  
 (LTC DWG # 05-08-1110)



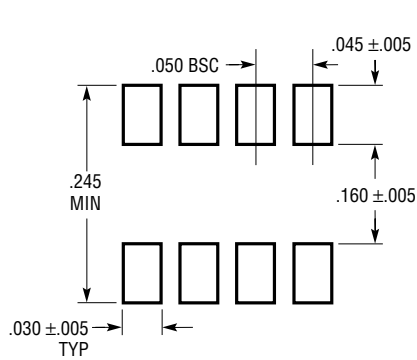
**OBsolete PACKAGE**

**N8 Package**  
**8-Lead PDIP (Narrow 0.300)**  
 (LTC DWG # 05-08-1510)

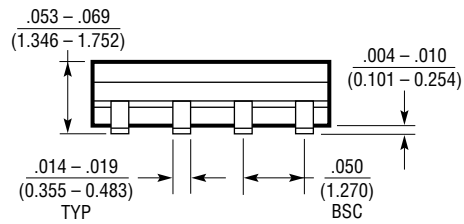
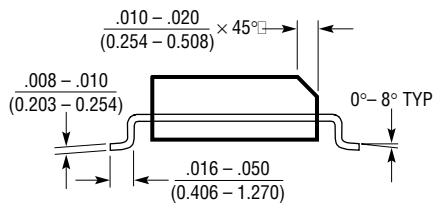
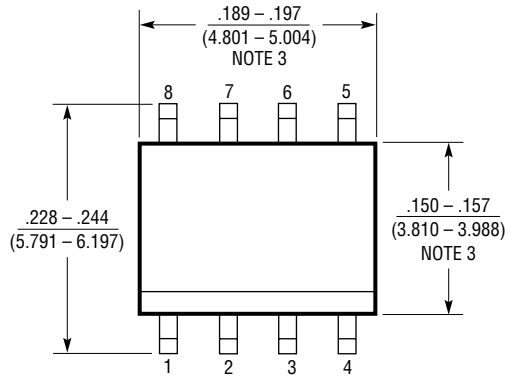


**PACKAGE DESCRIPTION**

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow 0.150)**  
 (LTC DWG # 05-08-1610)



RECOMMENDED SOLDER PAD LAYOUT

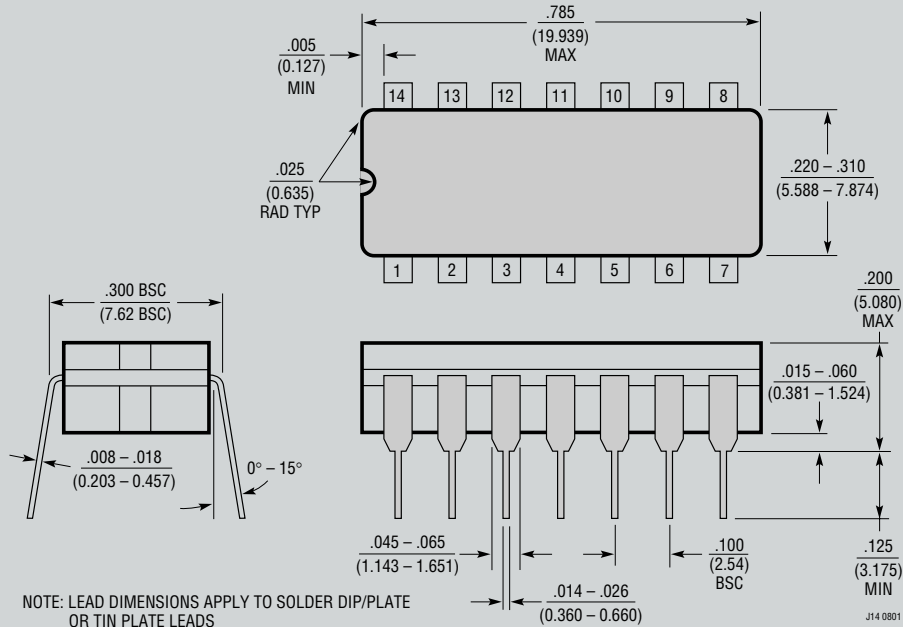


- NOTE:  
 1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 2. DRAWING NOT TO SCALE  
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

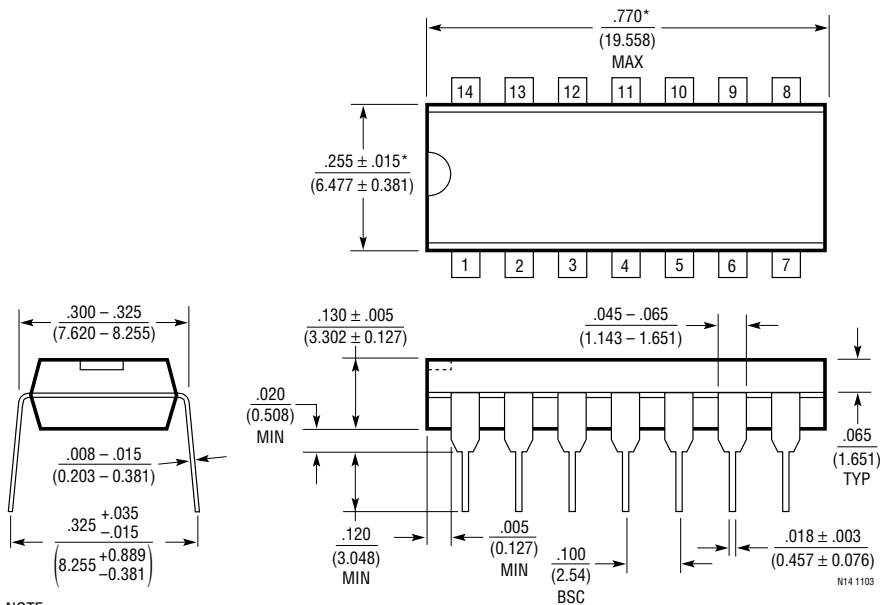
**PACKAGE DESCRIPTION**

**J Package**  
**14-Lead CERDIP (Narrow 0.300, Hermetic)**  
 (LTC DWG # 05-08-1110)



**OBsolete PACKAGE**

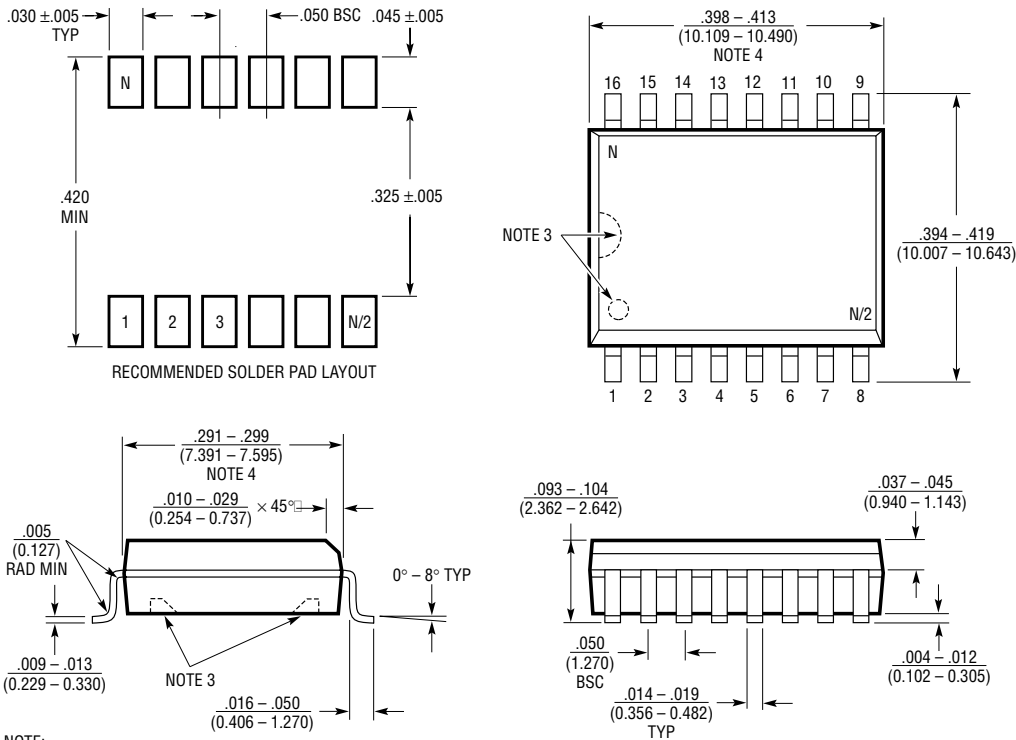
**N Package**  
**14-Lead PDIP (Narrow 0.300)**  
 (LTC DWG # 05-08-1510)



NOTE:  
 1. DIMENSIONS ARE INCHES / MILLIMETERS  
 \*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

**PACKAGE DESCRIPTION**

**SW Package**  
**16-Lead Plastic Small Outline (Wide 0.300)**  
 (LTC DWG # 05-08-1620)

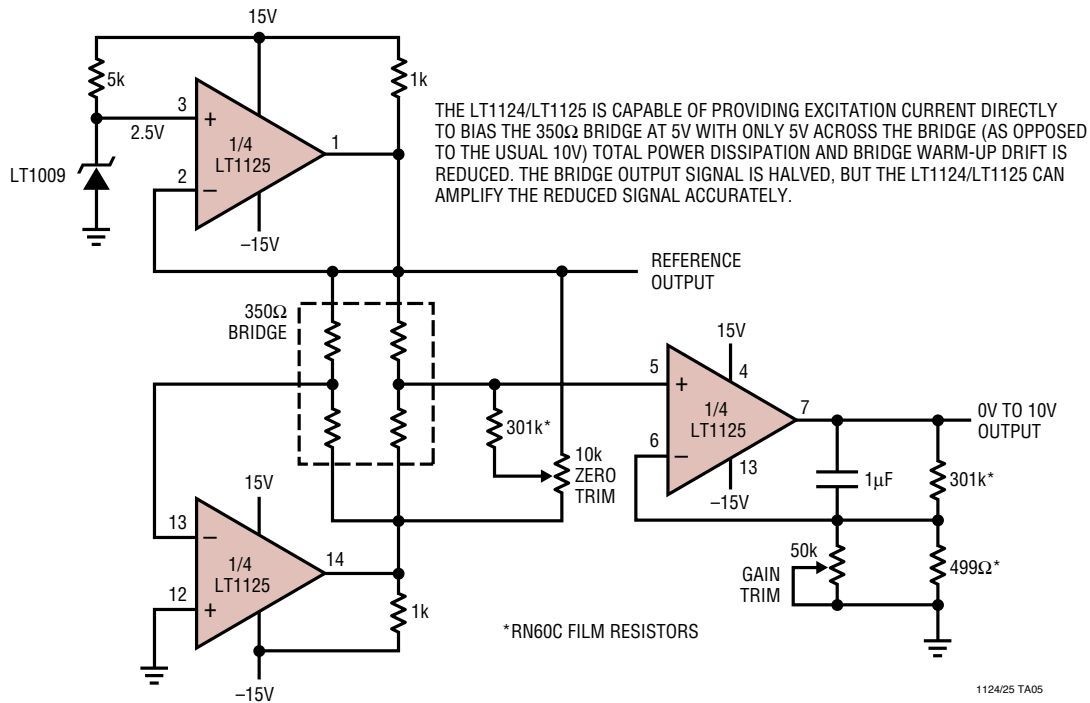


- NOTE:
1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
  2. DRAWING NOT TO SCALE
  3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
  4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $.006''$  (0.15mm)

S16 (WIDE) 0502

# TYPICAL APPLICATION

## Strain Gauge Signal Conditioner with Bridge Excitation



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1007	Single Low Noise, Precision Op Amp	2.5nV/√Hz 1kHz Voltage Noise
LT1028/LT1128	Single Low Noise, Precision Op Amps	0.85nV/√Hz Voltage Noise
LT1112/LT1114	Dual/Quad Precision Picoamp Input	250pA Max I <sub>B</sub>
LT1113	Dual Low Noise JFET Op Amp	4.5nV/√Hz Voltage Noise, 10fA/√Hz Current Noise
LT1126/LT1127	Decompensated LT1124/LT1125	11V/μs Slew Rate
LT1169	Dual Low Noise JFET Op Amp	6nV/√Hz Voltage Noise, 1fA/√Hz Current Noise, 10pA Max I <sub>B</sub>
LT1792	Single LT1113	4.2nV/√Hz Voltage Noise, 10fA/√Hz Current Noise
LT1793	Single LT1169	6nV/√Hz Voltage Noise, 1fA/√Hz Current Noise, 10pA Max I <sub>B</sub>