4.3inch 480x272 Touch LCD (B)

User Manual

Chinese website: www.waveshare.net
English Website: www.wvshare.com
Data download: www.waveshare.net/wiki

目录

1. Overview

Module Type	TFT
Interfaces	LCD: 24-bit parallel RGA data input; Touch panel: 4-wire resistive touch screen
Backlight	LED
Response time (ms)	30
Contrast	500:1
Brightness(cd/m)	280
Display area(mm)	95.04(W)×53.86(H)
Dot pitch (mm)	0.006(W)×0.198(H)
Chromatic index	16,777,216
Aspect ratio	16:9
Resolution	480 X 272 (Pixel)
Power Dissipation	56mW
Back facet current	20mA
Operating temperature(℃)	-20 ~ +70

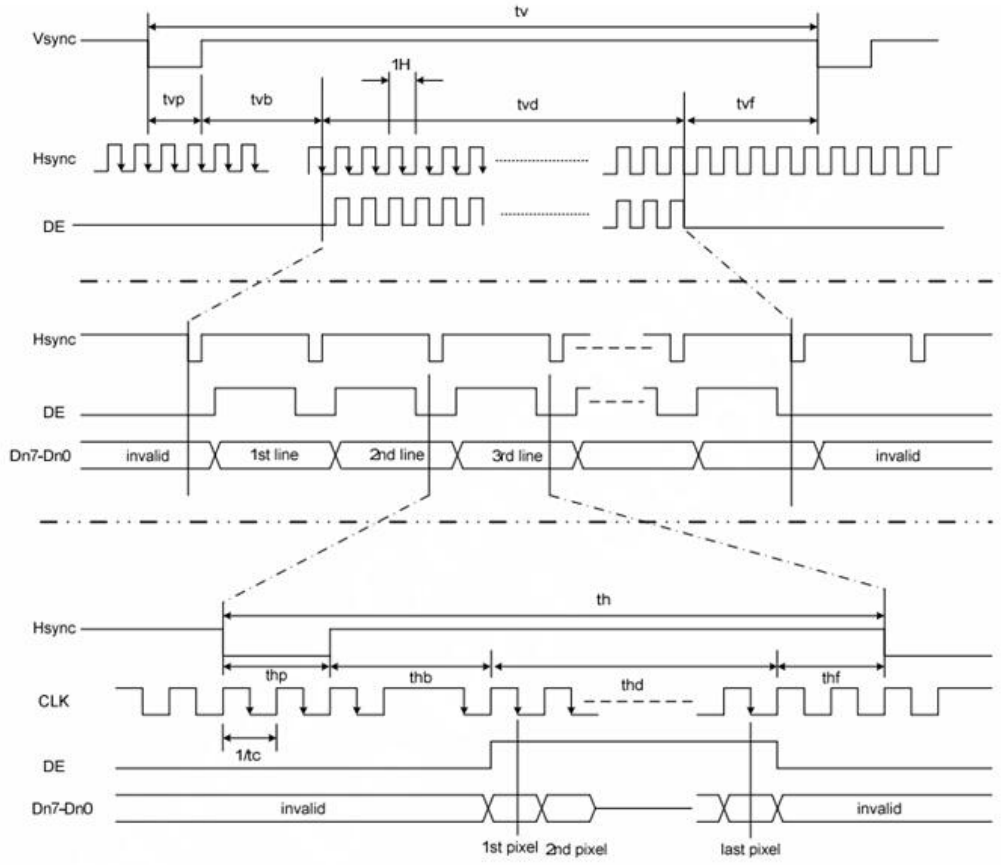
2. Chips on Board

2.1 HX8257-A

HX8257-A is a TFT LCD single chip digital driver with features below:

- Support 480RGBx272 or 480RGBx240 graphics display TFT LCD panel;
- Support 8-bit serial RGB data and 24-bit parallel RGB data input;
- Power supply VDD: 1.8V~3.6V;
- 720-channel source outputs and 544-channel gate outputs;
- PWM control function to generate power for backlight.

When applying HX8257-A, a MCU with LCD controller is required, since the LCD controller is not included in this LCD. Here is the basic sequence of HX8257-A:



The meanings of the main signals in the sequence diagram above are listed as follow:

Symbol	Description
Vsync	Vertical sync signal, which indicates the starting to scan a new frame. One frame refers to one picture shown in the LCD
Hsync	Horizontal sync signal, which indicates the starting to scan a new line
DE	Input data enable control
CLK	LCD clock
Dn7-Dn0	Parallel data

Here are the meanings of other symbols in the sequence diagram:

Symbol	Description	Reference			Unit
		Min.	Typ.	Max.	
fclk	LCD clock cycle	-	9	15	MHz
Horizontal signal					
th	Horizontal cycle	525	525	605	$CLK_{(1)}$
thd	Horizontal display period	480	480	480	$CLK_{(1)}$
thf	Horizontal front	2	2	82	$CLK_{(1)}$

	porch				
thp(2)	Horizontal pulse width	2	41	41	CLK(1)
thb(2)	Horizontal back porch	2	2	41	CLK(1)
Vertical signal					
tv	Vertical cycle	285	286	399	H (1)
tvd	Vertical display period	272	272	272	H (1)
tvf	Vertical front porch	1	2	227	H (1)
tvp (2)	Vertical pulse width	1	10	11	H (1)
tvb (2)	Vertical back porch	1	2	11	H (1)

Remarks:

1) Unit: CLK=1/fCLK, it is the duration for scanning a pixel; H=th, it is the duration for scanning a line;
2) It is necessary to keep tvp+tvb=12 and thp+thb=43 in sync mode. DE mode is unnecessary to keep it.

From the figure above, we can learn that:

The total time for scanning a line is: th = thp + thb + thd + thf; in the period of thd, when a clock plus comes, a pixel data will be transmitted via the parallel data interface. And there are 480 pixels each line for this LCD, so thd=480;

The duration for scanning a frame is: tv = tvp + tvb + tvd + tvf; Hsync can be regarded as the clock of vertical signals. A clock cycle of Hsync refers to the duration for LCD displaying a line. When a falling edge comes in Hsync, a new line will be displayed in the LCD. However, the actual data transmission only occurs in the period of tvd. And the LCD will display the new line in this case. There are 272 lines for this LCD, so tvd = 272.

Other parameters can be modified as required, according to the specifications listed in the tables above.

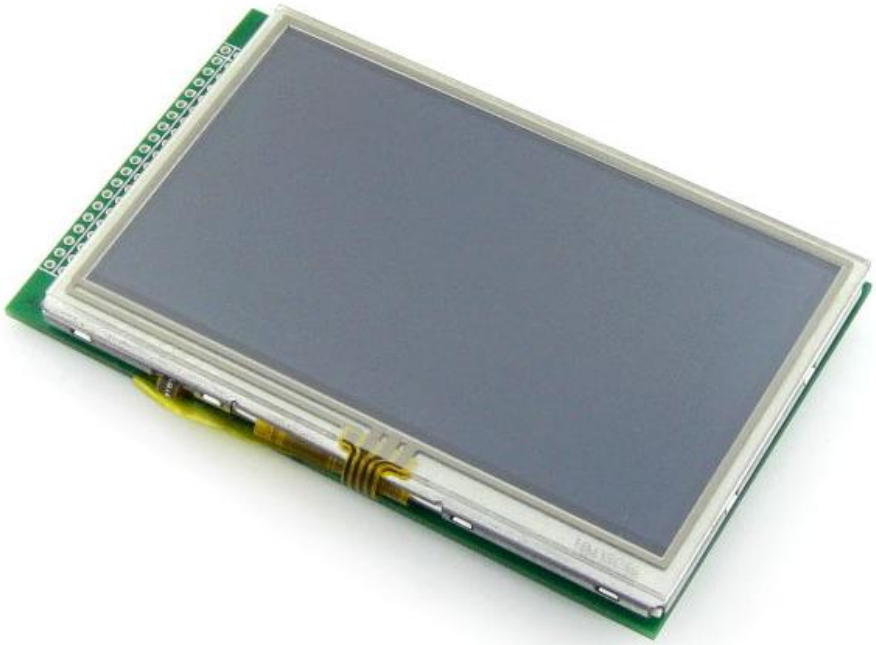
2.2 XPT2046

XPT2046 is a 4-wire resistive touch screen controller with features below:

- A 12-bit 125 kHz sampling SAR type A/D converter;
- Support digital I/O interface voltage from 1.5V to 5V;
- Enable to detect the pressed screen location by performing two A/D conversions, and measure touch screen pressure as well;
- An on-chip temperature sensor.

For more detailed information, please refer to XPT2046 data sheet.

3. Pin description



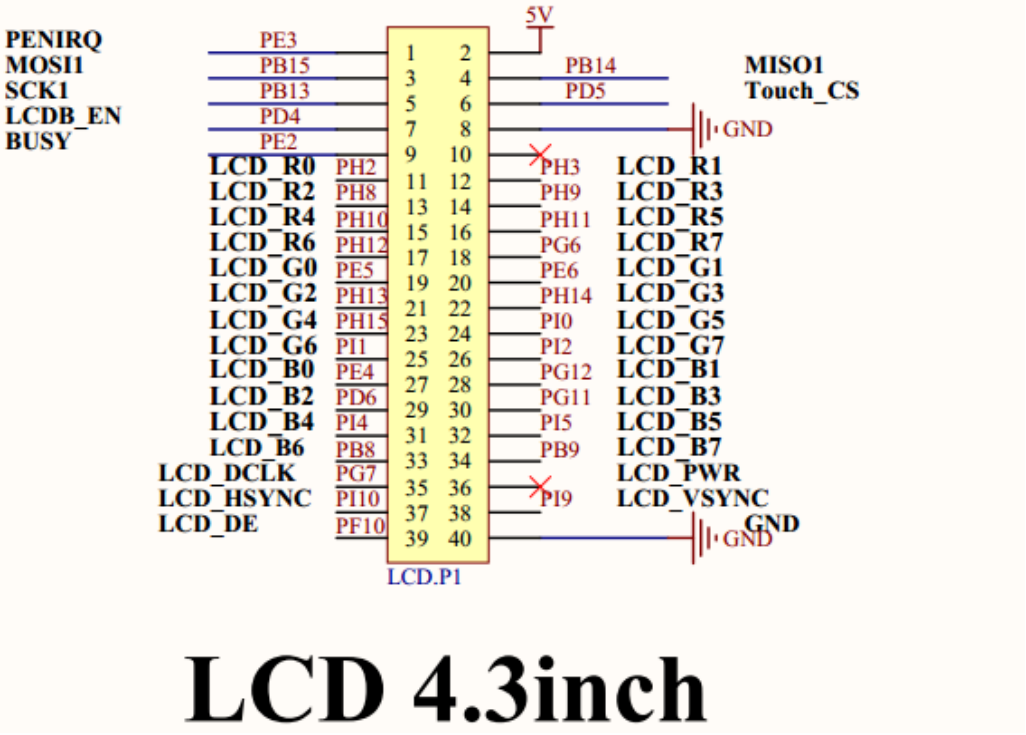
Pin No.	Symbol	Descriptions	I/O	Functions
1	IRQ	Touch screen interrupt	O	When detected the screen is pressed, it is pulled LOW
2	5V	5V power supply	I	Supply 5V power voltage
3	MOSI	Touch screen SPI data input	I	Connected to the MOSI of SPI
4	MISO	Touch screen SPI data output	O	Connected to the MOSO of SPI
5	SCK	Touch screen SPI clock signal	I	Connected to the SCK of SPI
6	SSEL	Touch screen chip select input	I	When selected touch screen, it is pulled LOW
7	PWM	Backlight brightness control	I	Signal line for PWM control backlight
8	GND	Ground	I	GND
9	BUSY	Touch screen busy output	O	
10	NC			
11	R0	Data line	I	Red pallet data line
12	R1			
13	R2			
14	R3			
15	R4			

16	R5			
17	R6			
18	R7			
19	G0	Data line	I	Green pallet data line
20	G1			
21	G2			
22	G3			
23	G4			
24	G5			
25	G6			
26	G7			
27	B0	Data line	I	Blue pallet data line
28	B1			
29	B2			
30	B3			
31	B4			
32	B5			
33	B6			
34	B7			
35	DCLK	LCD clock	I	LCD clock signal source
36	DSIP	NC		
37	HSYNC	Horizontal synchronization	I	Horizontal sync signal input
38	VSYNC	Vertical synchronization	I	Vertical sync signal input
39	DE	Input data enable control	I	DE=0:SYNC mode
DE=1:DE mode				
40	GND	Ground	I	GND

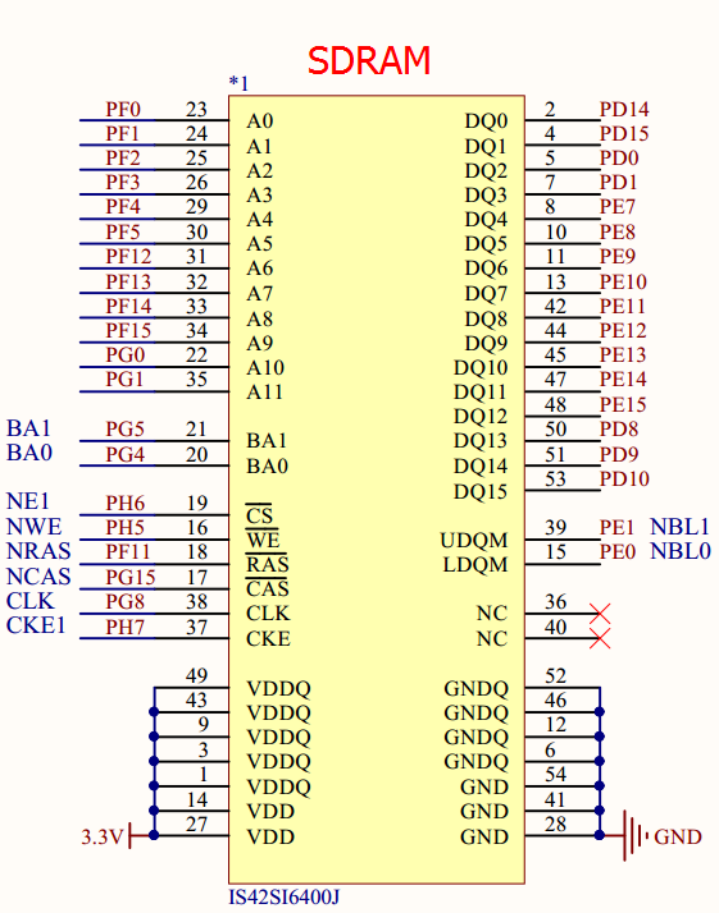
4. Demos

In this document, we will illustrate the basic usage of this 4.3 inch 480×272 touch LCD (B) by using a development board with STM32F407IGT6 as main control chip. Of course, you can apply other similar development boards for development as well.

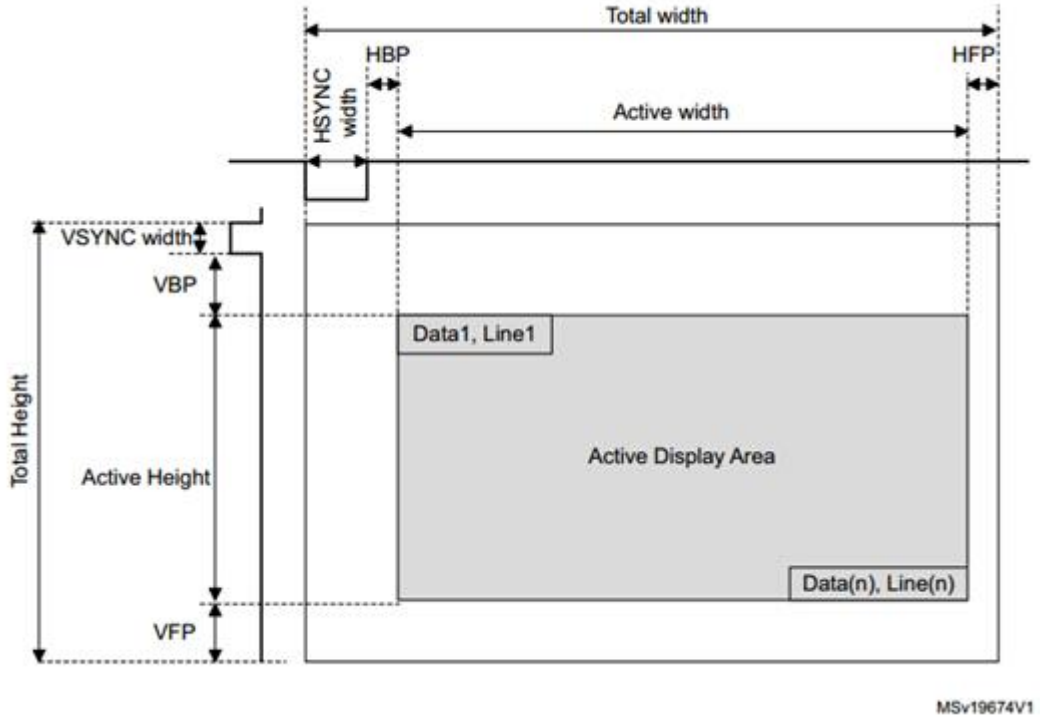
The following figures show how to connect the 4.3 inch 480x272 Touch LCD (B) to STM32F407IGT6.



LCD 4.3inch



The controller integrated in STM32F429IGT6 is as the figure below shows.



The meanings of the symbols in the figure above are listed as follow:

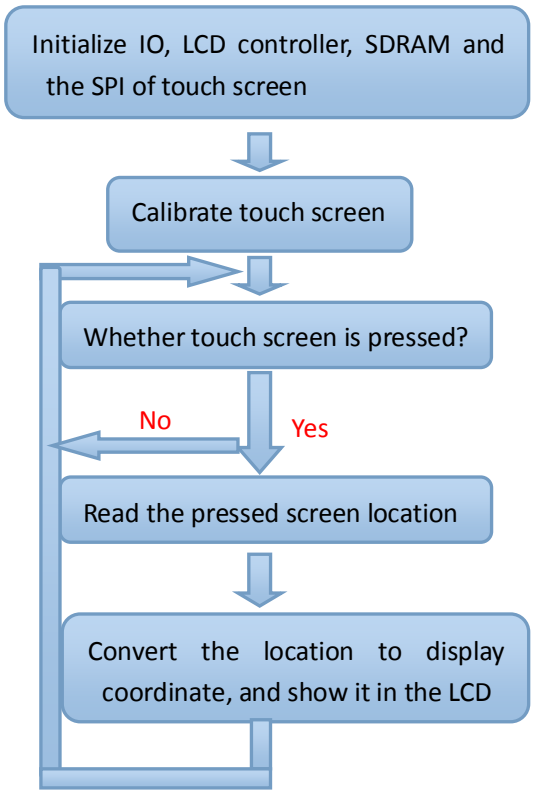
VBP is for vertical back porch and VFP is for horizontal back porch.
- HSYNC Width and VSYNC Height: HSYNC Width is for Horizontal Synchronization Width and VSYNC Height is Vertical Synchronization Height. They can be set by the bits HSW(LTDC_SSCR[27:16]) and VSH(LTDC_SSCR[10:0]) of LTDC_SSCR register, where HSW= HSYNC Width – 1, and VSH = VSYNC Height – 1.

- HBP and VBP can be set by the bits AHBP(LTDC_BPCR[27:16]) and AVBP(LTDC_BPCR[10:0]) of LTDC_BPCR register, where AHBP= HSYNC Width + HBP – 1, and AVBP= VSYNC Height + VBP – 1.

- Active Width and Active Height can be set by the bits AAW(LTDC_AWCR[27:16]) and AAH(LTDC_AWCR[10:0]) of LTDC_AWCR register, where AAW= HSYNC Width + HBP+ Active Width – 1, and AAH= VSYNC Height + VBP+ Active Height – 1.

- Total Width and Total Height can be set by the bits TOTALW(LTDC_TWCR[27:16]) and TOTALH(LTDC_TWCR[10:0]) of LTDC_TWCR register, where TOTALW= HSYNC Width + HBP+ Active Width +HFP – 1, and TOTALH= VSYNC Height + VBP+ Active Height +VFP – 1.

Program flow chart:



5. Test result

6. Dimensions