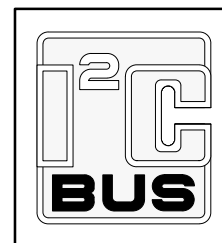


# DATA SHEET



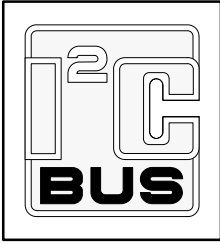
## **P82B715** I<sup>2</sup>C bus extender

Product data  
Supersedes data of 2001 Mar 06

2003 Feb 20

I<sup>2</sup>C bus extender

## P82B715



## DESCRIPTION

The P82B715 is a bipolar integrated circuit intended for application in I<sup>2</sup>C bus systems.

While retaining all the operating modes and features of the I<sup>2</sup>C system it permits extension of the practical separation distance between components on the I<sup>2</sup>C bus by buffering both the data (SDA) and the clock (SCL) lines.

The I<sup>2</sup>C bus capacitance limit of 400 pF restricts practical communication distances to a few meters. Using one P82B715 at each end of longer cables reduces the cable loading capacitance on the I<sup>2</sup>C bus by a factor of 10 times and may allow the use of low cost general purpose wiring to extend bus lengths.

## FEATURES

- Dual, bi-directional, unity voltage gain buffer
- I<sup>2</sup>C bus compatible
- Logic signal levels may include both supply and ground
- X10 impedance transformation
- Supply voltage range of 4.5 to 12 V
- 100 kHz operation
- ESD protection exceeds 2500 V HBM per Mil. Std 883C-3015.7
- Latch-up free (bipolar process with no latching structures)

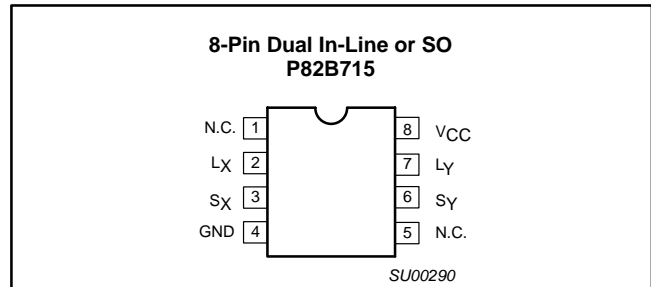
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic dual In-line package	-40 to +85 °C	P82B715PN	P82B715PN	SOT97-1
8-pin plastic small outline package	-40 to +85 °C	P82B715TD	P82B715	SOT96-1

## NOTES:

1. For applications requiring lower voltage operation, or additional buffer performance, see AN255 I<sup>2</sup>C and SMBus Repeaters, Hubs and Expanders Application Note.
2. Standard packing quantities and other packaging data are available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

## PIN CONFIGURATIONS

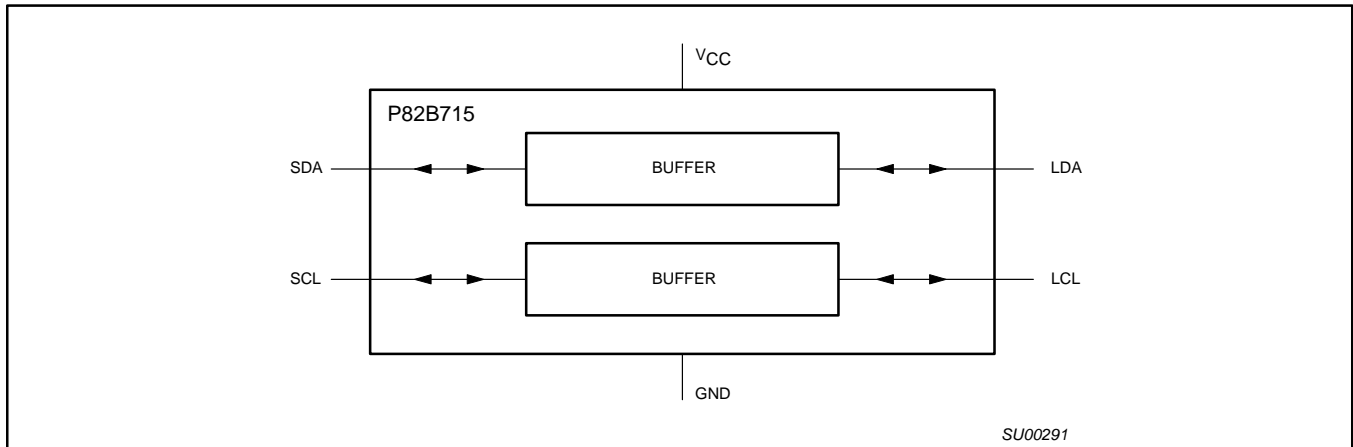


## PINNING

PIN	SYMBOL	FUNCTION
1	N.C.	No connect
2	L <sub>X</sub>	Buffered Bus, LDA or LCL
3	S <sub>X</sub>	I <sup>2</sup> C Bus, SDA or SCL
4	GND	Negative Supply
5	N.C.	No connect
6	S <sub>Y</sub>	I <sup>2</sup> C Bus, SCL or SDA
7	L <sub>Y</sub>	Buffered Bus, LCL or LDA
8	V <sub>CC</sub>	Positive Supply

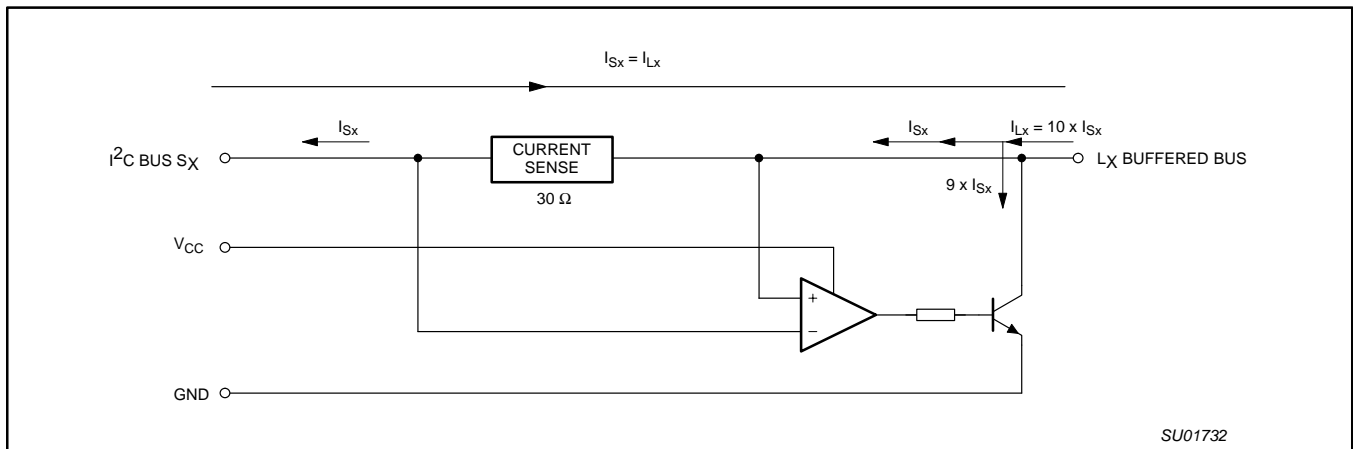
I<sup>2</sup>C bus extender

P82B715



SU00291

Figure 1. Block Diagram: P82B715



SU01732

Figure 2. Equivalent Circuit: One Half P82B715

**S<sub>x</sub>, S<sub>y</sub>, I<sup>2</sup>C Bus, SDA or SCL**

On the normal side, because the two buffer circuits in the P82B715 are identical, either the S<sub>x</sub> or S<sub>y</sub> input pins can be used as the I<sup>2</sup>C Bus SDA data line, or the SCL clock line.

**L<sub>x</sub>, L<sub>y</sub>, Buffered Bus, LDA or LCL**

On the special low impedance or buffered line side, the corresponding output becomes the LDA data line or LCL clock line.

**V<sub>CC</sub>, GND — Positive and Negative Supply Pins**

In normal use the power supply voltages at each end of the low impedance buffered bus line should be the same. If these differ by a significant amount, noise margin is sacrificed.

# I<sup>2</sup>C bus extender

# P82B715

## FUNCTIONAL DESCRIPTION

The P82B715 bipolar integrated circuit is a dual bi-directional logic signal driver that increases the allowable total I<sup>2</sup>C system wiring capacitance. It contains identical circuits, one for each bus signal, and requires no external directional control. It uses unidirectional analog current amplification to increase the current sink capability of I<sup>2</sup>C chips by a factor 10 and to change the 400 pF I<sup>2</sup>C bus specification limit into a 4nF bus wiring capacitance limit. This allows I<sup>2</sup>C, or similar bus systems, to be extended over long distances without degradation of system performance or the use of special cables.

P82B715 provides current amplification from its I<sup>2</sup>C bus to its low impedance or buffered bus. Whenever current is flowing out of Sx, into an I<sup>2</sup>C chip driving the I<sup>2</sup>C bus low, its amplifier will sink ten times that current into Lx to drive the buffered bus low (see Figure 2).

To minimize interference and ensure stability, the current rise and fall times of the Lx drive amplifier are internally controlled.

The P82B715 does not amplify signal currents flowing into Sx on the I<sup>2</sup>C bus, driven by currents flowing out of Lx on the buffered side. A buffered bus logic low signal at Lx passes via the internal 30 Ω resistor to drive the I<sup>2</sup>C bus low.

This signal current amplification, dependent on its direction, preserves the multi-master, bi-directional, open-collector/open-drain, characteristic of any connected I<sup>2</sup>C bus lines and the new low impedance bus. Bus logic signal voltage levels will be clamped at (Vcc + 0.7 V) but otherwise are independent of the supply voltage Vcc.

## APPLICATION NOTES

By using two (or more) P82B715 ICs, a sub-system can be built that retains the interface characteristics of a normal I<sup>2</sup>C device so that the sub-system may be included in, or added onto, any I<sup>2</sup>C or related system.

The sub-system features a low impedance or buffered bus, capable of driving large wiring capacitance (see Figure 3).

The P82B715 will operate with a supply voltage from 3 V to 12.5 V but the logic signal levels at Sx/Lx are independent of the chip's supply. They remain at the levels presented to the chip by the attached ICs. The maximum static I<sup>2</sup>C bus sink current, 3 mA, flowing in either direction in the internal current sense resistor, causes a difference less than 100 mV in the bus logic low levels at Sx and Lx. This makes P82B715 fully compatible with all logic signal drivers, including TTL. The P82B715 cannot modify the bus logic signal voltage levels but it contains internal diodes connected between Lx/Sx and Vcc that will conduct and limit the logic signal swing if the applied logic levels would have exceeded the supply voltage by more than 0.7 V.

In normal applications external pull-up resistors will pull the connected buses up to the desired voltage high level. Usually this will be the chip supply, Vcc, but for very low logic voltages it is necessary to use a Vcc of at least 3.3 V and preferably higher. Note that full performance over temperature is only guaranteed from 4.5 V. Specification de-ratings that apply when its supply voltage is reduced below 4.5 V are given in Appendix 3 of AN255-02 I<sup>2</sup>C and SMBus Repeaters, Hubs and Expanders Application Note. The absolute minimum Vcc is 3 V.

## I<sup>2</sup>C Systems

As in standard I<sup>2</sup>C systems, pull-up resistors are required to provide the logic high levels on the buffered bus. (The standard open-collector configuration is retained). The size and number of pull-up resistors depends on the system.

If P82B715 ICs are to be permanently connected into a system, the circuit may be configured with only one pull-up resistor on the buffered bus and none on the I<sup>2</sup>C buses, but the system design will be simplified and performance improved by fitting separate pull-ups on each section of the bus. When a sub-system using P82B715 may be optionally connected to an existing I<sup>2</sup>C system that already has a pull-up then the effects of the sub-system pull-ups acting in parallel with the existing I<sup>2</sup>C bus pull-up must be considered.

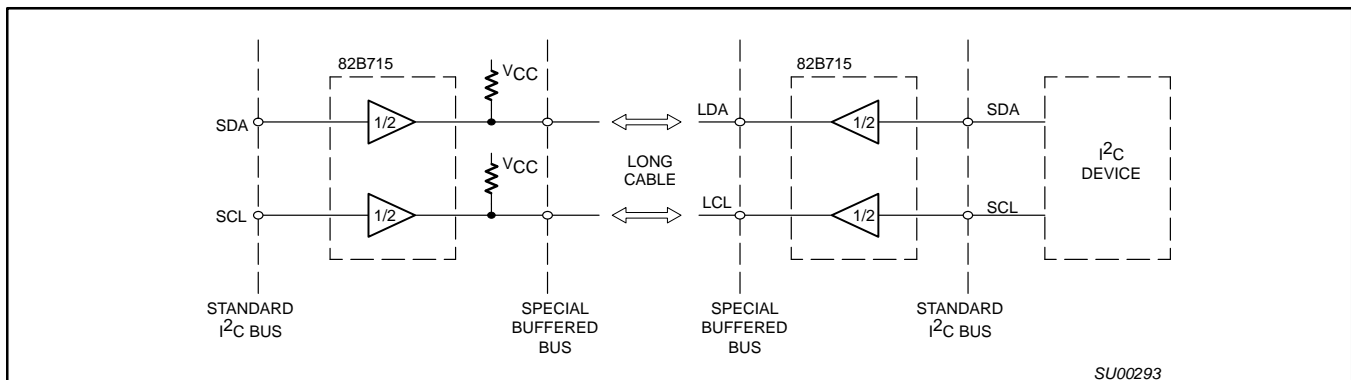


Figure 3. Minimum Sub-System with P82B715

## Pull-Up Resistance Calculation

When calculating the pull-up resistance values the gain of the buffer introduces scaling factors which must be applied to the system components. In practical systems the pull-up resistance value is calculated to meet the rise time limit for I<sup>2</sup>C systems. As an approximation, this limit will be satisfied in a 100 kHz system if the

time constant of the total system (product of the net resistance and net capacitance) is set to 1 microsecond or less.

In systems using the P82B715 it is convenient to set the total system time constant by considering each bus node separately (i.e., the I<sup>2</sup>C nodes and the buffered bus node) and selecting a

# I<sup>2</sup>C bus extender

# P82B715

separate pull-up resistor for each node to provide time constants of less than 1 microsecond. If each node complies then the system requirement is also met.

This arrangement, using multiple pull-ups as in Fig 4, provides the best system performance and allows stand-alone operation of individual I<sup>2</sup>C buses if parts of the extended system are disconnected or re-connected. For each bus section the pull-up resistor is calculated as follows:

$$R = \frac{1\mu s}{C_{\text{device}} + C_{\text{wiring}}}$$

Where: C device = sum of any connected device capacitances, and C wiring = total wiring and stray capacitance on the bus section.

[The 1 μs is an approximation, with a safety factor, to the theoretical time-constant necessary to meet the specified 1 μs bus rise-time specification in a system with variable logic thresholds where the CMOS limits of 30% and 70% of V<sub>CC</sub> apply. The calculated value is 1.18 μs.]

If these capacitances cannot be measured or calculated then an approximation can be made by assuming that each device presents 10 pF of load capacitance and 10 pF of trace capacitance and that cables range from 50 to 100 pF per metre.

If only a single pull-up must be used then it must be placed on the buffered bus (as R2 in Fig 4) and the associated total system capacitance calculated by combining the individual bus capacitances into an equivalent capacitive loading on the buffered bus.

This equivalent capacitance is the sum of the capacitance on the buffered bus plus 10 times the sum of the capacitances on all the connected I<sup>2</sup>C nodes. The calculated value should not exceed 4 nF. The single buffered bus pull-up resistor is then calculated to achieve the 1 μs risetime and it then provides the pull-up for the buffered bus and for all other connected I<sup>2</sup>C bus nodes included in the calculation.

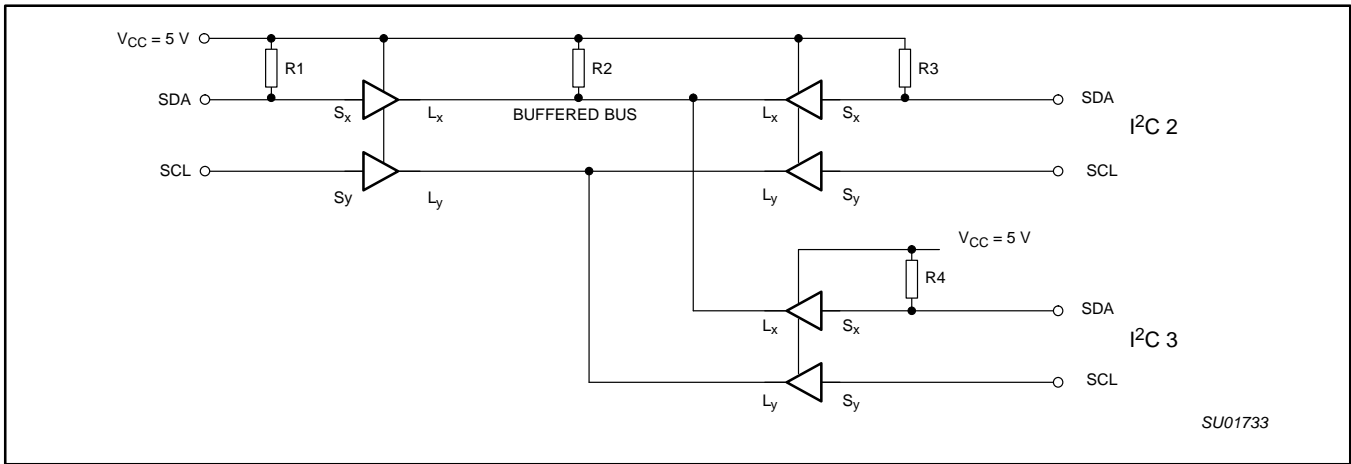


Figure 4. Single Pull-up Buffered Bus

### Calculating bus drive currents

Figure 4 shows three P82B715s connected to a common buffered bus. The associated bus capacitances are omitted for clarity but assume the resistors have been selected to give R-C products of less than 1 μs so the bus rise time requirement is satisfied. An I<sup>2</sup>C chip connected at I<sup>2</sup>C 1 and holding the SDA bus low must sink the current flowing in its local pull-up R1 plus, with assistance from the P82B715, the currents in R2, R3 and R4. Because the resistors R3 and R4 act to pull the bus nodes I<sup>2</sup>C 2 and I<sup>2</sup>C 3, and their corresponding Sx pins, to a voltage higher than the voltage at the Lx pins their buffer amplifiers will be inactive. The SDA at Sx of I<sup>2</sup>C 2 and I<sup>2</sup>C 3 is pulled low by the low at Lx via the internal 30 ohm resistor that links Lx to Sx. So the effective current that must be sunk by the P82B715 buffer on I<sup>2</sup>C 1, at its Lx pin, is the sum of the currents in R2, R3 and R4. The Sx current that must be sunk by an I<sup>2</sup>C chip at I<sup>2</sup>C 1, due to the buffer gain action, is 1/10 of the Lx current. So the effective pull-up, determining the current to be sunk by an I<sup>2</sup>C chip at I<sup>2</sup>C 1, is R1 in parallel with resistors 10 times the values of R2, R3 and R4. If R1 = R3 = R4 = 10k, and R2 = 1k, the effective pull-up load at I<sup>2</sup>C 1 is 10k||10k||100k||100k = 4.55 k ohms

The same calculation applies for I<sup>2</sup>C 2 or I<sup>2</sup>C 3.

To calculate the current sunk by the Lx pin of the buffer at I<sup>2</sup>C 1 note that the current in R1 is sunk directly by the IC at I<sup>2</sup>C 1. The buffer therefore sinks only the currents flowing in R2, R3, and R4 so the effective pull-up is R2 in parallel with R3 and R4.

In this example that's 1k||10k||10k = 833 ohms. For a 5.5 V supply and 0.4 V low that means the buffer is sinking 16.3 mA.

The P82B715 has a static sink rating of 30 mA at Lx. The requirement is that the pull-up on the buffered bus, in parallel with all other pull-ups that it is indirectly pulling low on Sx pins of other P82B715 ICs, will not cause this 30 mA limit to be exceeded.

The minimum pull-up resistance in a 5 V +/-10% system is 170 ohms.

The general requirement is:

$$\frac{V_{CC \text{ max}} - 0.4}{R_P} < 30 \text{ mA}$$

Where: R<sub>p</sub> = parallel combination of all pull-up resistors driven by the Lx pin of the P82B715.

Figure 5 shows calculations for an expanded I<sup>2</sup>C bus with 3 nF of cable capacitance.

# I<sup>2</sup>C bus extender

# P82B715

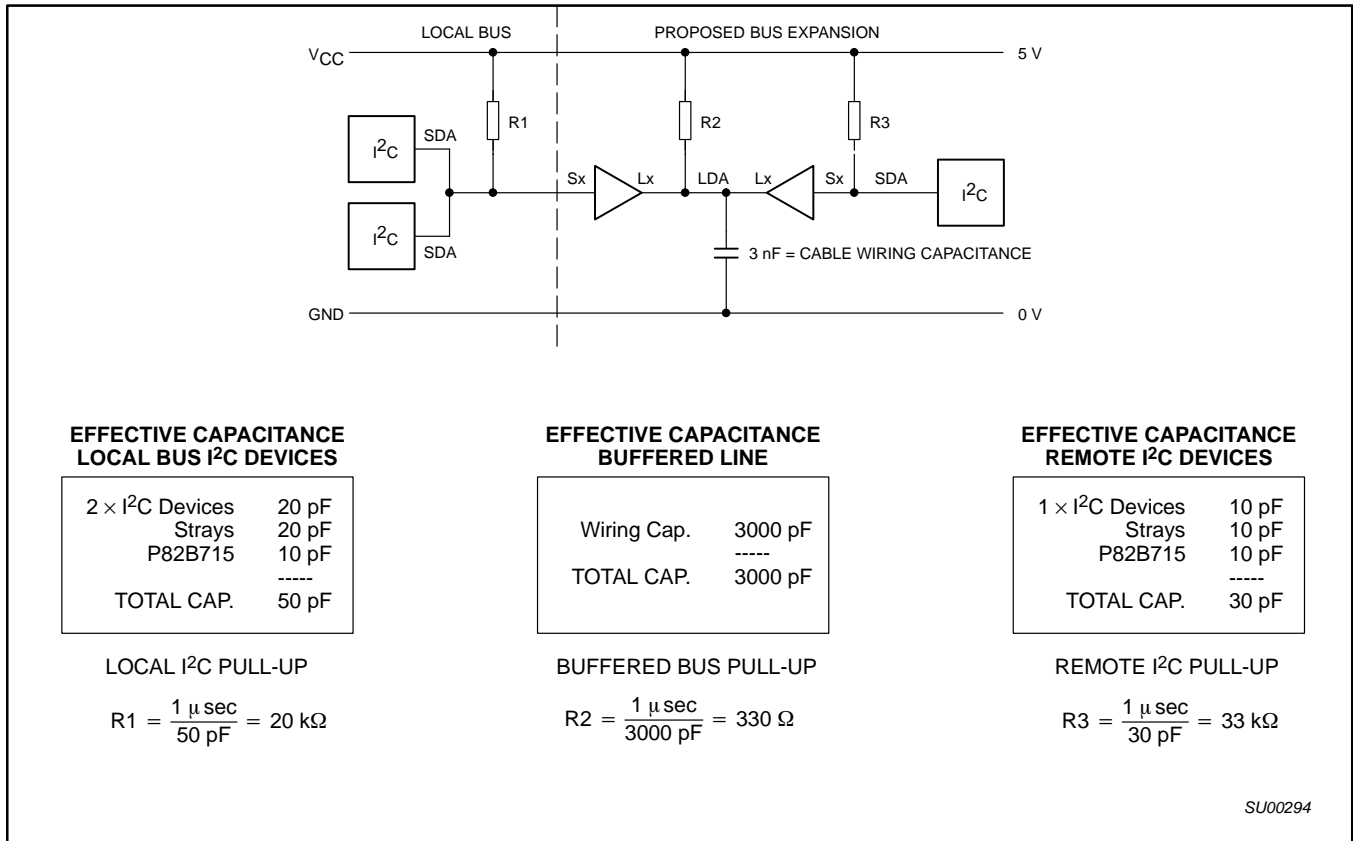


Figure 5. Typical Loading Calculation: Adding An Extension Bus with P82B715

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134). Voltages with respect to pin GND (DIL-8 pin 4).

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V <sub>CC</sub> to GND	Supply voltage range V <sub>CC</sub>	-0.3	+12	V
V <sub>bus</sub>	Voltage range I <sup>2</sup> C Bus, SCL or SDA	0	V <sub>CC</sub>	V
V <sub>buff</sub>	Voltage range Buffered Bus	0	V <sub>CC</sub>	V
I	DC current (any pin)	—	60	mA
P <sub>tot</sub>	Power dissipation	—	300	mW
T <sub>stg</sub>	Storage temperature range	-55	+125	°C
T <sub>amb</sub>	Operating ambient temperature range	-40	+85	°C

I<sup>2</sup>C bus extender

P82B715

**CHARACTERISTICS**At T<sub>amb</sub> = +25 °C and V<sub>CC</sub> = 5 Volts, unless otherwise specified.

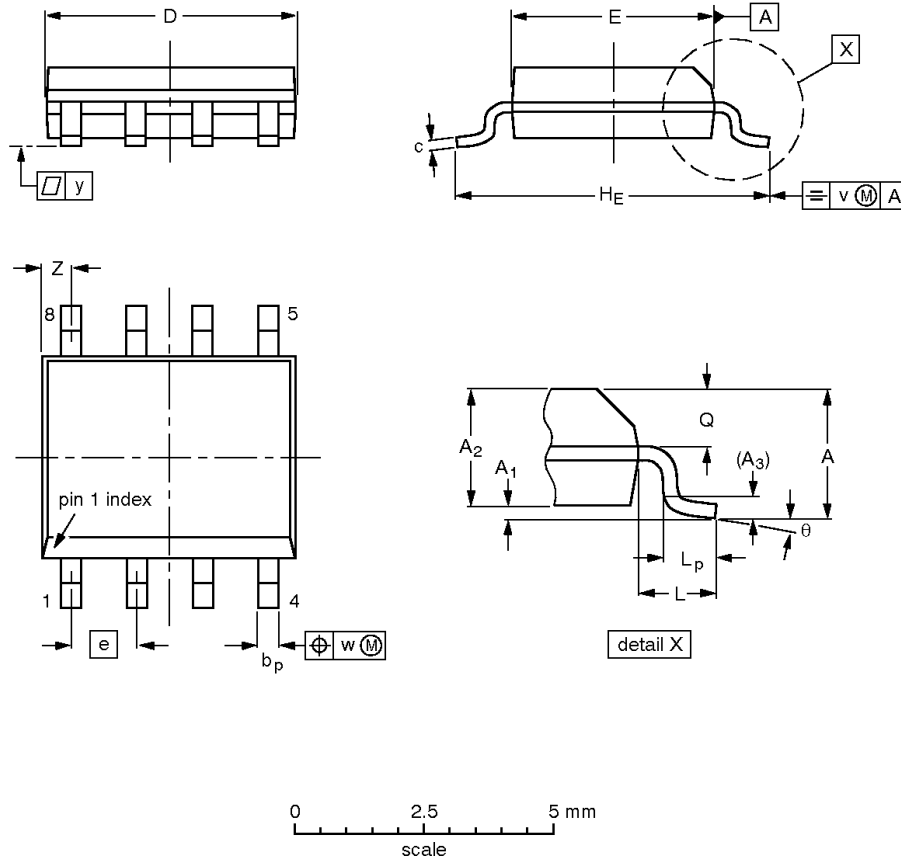
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
<b>Power Supply</b>					
V <sub>CC</sub>	Supply voltage (operating)	4.5	—	12	V
I <sub>CC</sub>	Supply current	—	16	—	mA
I <sub>CC</sub>	Supply current at V <sub>CC</sub> = 12 V	—	22	—	mA
I <sub>CC</sub>	Supply current, both I <sup>2</sup> C inputs LOW, both buffered outputs sinking 30 mA.	—	28	—	mA
<b>Drive Currents</b>					
I <sub>Sx</sub> , I <sub>Sy</sub>	Output sink on I <sup>2</sup> C bus V <sub>Sx</sub> , V <sub>Sy</sub> LOW = 0.4 V V <sub>Lx</sub> , V <sub>Ly</sub> LOW on Buffered bus = 0.3 V	3	—	—	mA
I <sub>Lx</sub> , I <sub>Ly</sub>	Output sink on Buffered bus V <sub>Lx</sub> , V <sub>Ly</sub> LOW = 0.4 V V <sub>Sx</sub> , V <sub>Sy</sub> LOW on I <sup>2</sup> C bus = 0.3 V	30	—	—	mA
<b>Input Currents</b>					
I <sub>Sx</sub> , I <sub>Sy</sub>	Input current from I <sup>2</sup> C bus when I <sub>Lx</sub> , I <sub>Ly</sub> sink on Buffered bus = 30 mA	—	—	3	mA
I <sub>Lx</sub> , I <sub>Ly</sub>	Input current from Buffered bus when I <sub>Sx</sub> , I <sub>Sy</sub> sink on I <sup>2</sup> C bus = 3 mA	—	—	3	mA
I <sub>Lx</sub> , I <sub>Ly</sub>	Leakage current on Buffered bus V <sub>Lx</sub> , V <sub>Ly</sub> = V <sub>CC</sub> , and V <sub>Sx</sub> , V <sub>Sy</sub> = V <sub>CC</sub>	—	—	200	μA
<b>Impedance Transformation</b>					
Z <sub>in</sub> /Z <sub>out</sub>	Input/Output impedance	8	10	13	

# I<sup>2</sup>C bus extender

# P82B715

**SO8: plastic small outline package; 8 leads; body width 3.9 mm**

**SOT96-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22 99-12-27

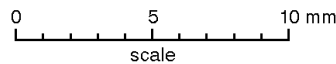
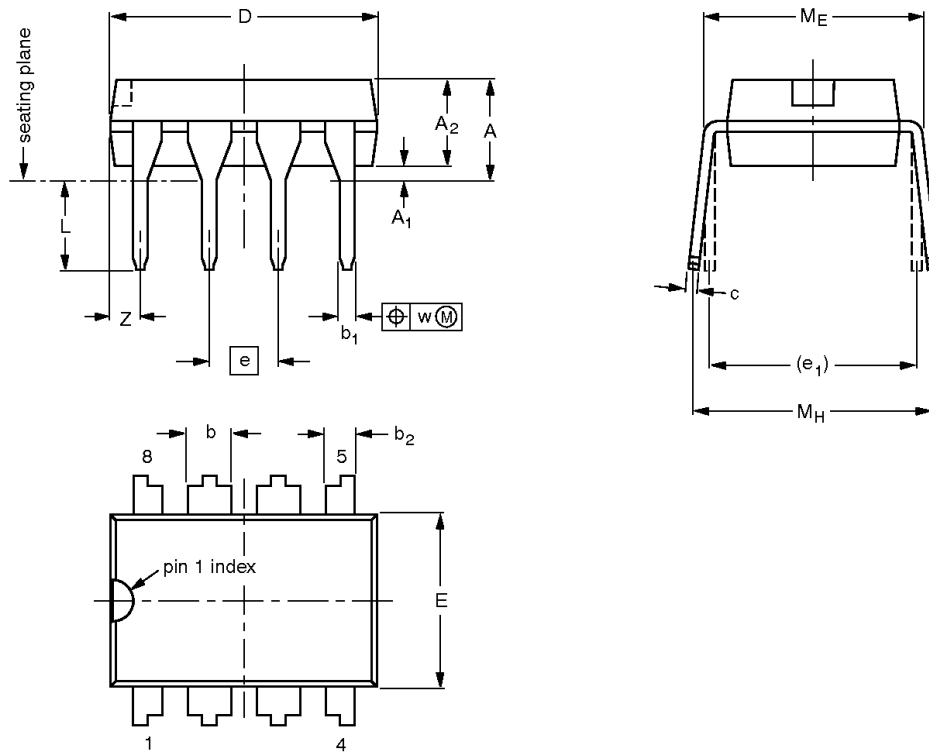


I<sup>2</sup>C bus extender

P82B715

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			95-02-04 99-12-27

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**I<sup>2</sup>C bus extender****P82B715**

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**REVISION HISTORY**

<b>Rev</b>	<b>Date</b>	<b>Description</b>
_5	20030220	<b>Product data (9397 750 11094); ECN 853-2240 29410 of 22 January 2003; supersedes data of 2001 Mar 06 (9397 750 08163).</b> Modifications: <ul style="list-style-type: none"><li>• Pin capacitance added</li></ul>
_4	20010306	<b>Product data (9397 750 08163); ECN 853-2240 25757 of 2001 Mar 06.</b>

I<sup>2</sup>C bus extender

P82B715



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 02-03

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Document order number:

9397 750 11094

*Let's make things better.*