ULTRA-SMALL SUPPLY VOLTAGE SUPERVISORS

FEATURES

- **Small, 5-Pin SC-70 (SOT-323) Package**
- **Supply Current of 9 µA**
- **Power-On Reset Generator With Fixed Delay Time**
  - **– TPS3800 = 100 ms**
  - **– TPS3801 = 200 ms**
  - **– TPS3802 = 400 ms**
- **Precision Supply Voltage Monitor 1.8 V, 2.5 V, 2.7 V, 3 V, 3.3 V, 5 V, and Adjustable**
- **Manual Reset Input (Except TPS3801-01)**
- **Temperature Range: -40°C to 85°C**

APPLICATIONS

- **Applications Using DSPs, Microcontrollers, or Microprocessors**
- **Wireless Communication Systems**
- **Portable/Battery-Powered Equipment**
- **Programmable Controls**
- **Intelligent Instruments**
- **Industrial Equipment**
- **Notebook/Desktop Computers**
- **Automotive Systems**

DESCRIPTION

The TPS380x family of supervisory circuits monitor supply voltages to provide circuit initialization and timing supervision, primarily for DSPs and other processor-based systems.

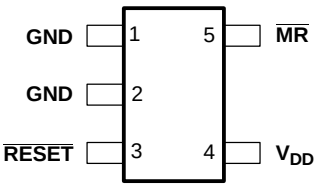
These devices assert a push-pull $\overline{\text{RESET}}$ signal when the SENSE (adjustable version) or V_{DD} (fixed version) drops below a preset threshold. The $\overline{\text{RESET}}$ output remains asserted for the factory programmed delay time after the SENSE or V_{DD} return above its threshold.

The TPS380x devices, except the TPS3801-01, incorporate a manual reset input ($\overline{\text{MR}}$). A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active.

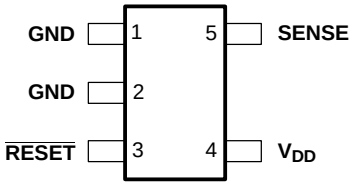
The TPS380x uses a precision reference to achieve an overall threshold accuracy of 2% - 2.5%. These devices are available in a 5-pin SC-70 package, which is only about half the size of a 5-pin SOT-23 package.

The TPS380x devices are fully specified over a temperature range of -40°C to 85°C.

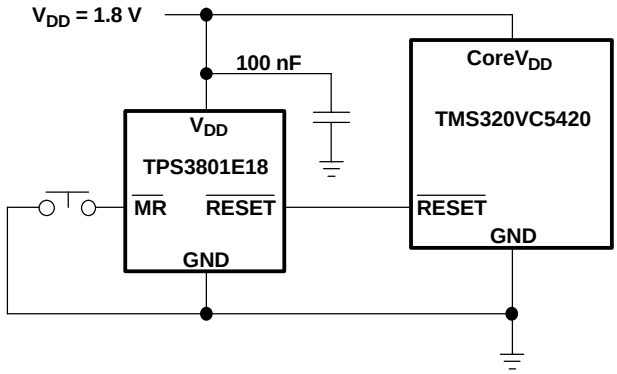
TPS380x . . . DCK PACKAGE
(TOP VIEW)



TPS3801−01. . . DCK PACKAGE
(TOP VIEW)



typical applications



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	Device name	THRESHOLD VOLTAGE	TYP DELAY TIME	MARKING
-40°C to 85°C	TPS3801-01DCK	Adjustable (V_{ref} = 1.14 V)	200 ms	ARF
	TPS3801E18DCK	1.71 V	200 ms	ARE
	TPS3801J25DCK	2.25 V	200 ms	NJA
	TPS3800G27DCK	2.5 V	95 ms	ARI
	TPS3801L30DCK	2.64 V	200 ms	NPA
	TPS3801K33DCK	2.93 V	200 ms	NWA
	TPS3802L30DCK	2.64 V	380 ms	ASA
	TPS3802K33DCK	2.93 V	380 ms	ARK
	TPS3801T50DCK	4.00 V	25 ms	AVI
	TPS3801I50DCK	4.55 V	200 ms	NSA

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

	UNIT
Supply voltage, V_{DD}	7 V
All other pins	-0.3 V to 7 V
Maximum low-output current, I_{OL}	5 mA
Maximum high-output current, I_{OH}	-5 mA
Input-clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±20 mA
Output-clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±20 mA
Operating junction temperature range, T_J (3)	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Soldering temperature (3 seconds)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation, the device should not be operated at 7 V for more than t=1000h continuously.

(3) Due to the low dissipation power of this device, it is assumed that $T_J = T_A$.

RECOMMENDED OPERATING CONDITIONS

		min	max	unit
Supply voltage, V_{DD}	TPS3801J25, TPS3801L30, TPS3801K33, TPS3801I50, TPS3801T50	2	6	V
	All other devices	1.6	4	
Input voltage, V_I		0	V_{DD}+0.3	V
High-level input voltage, V_{IH}		0.7×V_{DD}		V
Low-level input voltage, V_{IL}			0.3×V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A		-40	85	°C

ELECTRICAL CHARACTERISTICS

over -40°C to 85°C free-air temperature range (unless otherwise noted)

parameter			test conditions	min	typ	max	unit
V_{OH}	High-level output voltage ($\overline{RESET}$)		V_{DD} = 1.6 V to 6 V I_{OH} = -500 µA	V_{DD} -0.2			V
			V_{DD} = 3.3 V I_{OH} = -2 mA	V_{DD} -0.4			
			V_{DD} = 6 V I_{OH} = -4 mA (1)	V_{DD} -0.4			
V_{OL}	Low-level output voltage ($\overline{RESET}$)		V_{DD} = 1.6 V to 6 V, I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA (1)			0.4	
	Power-up reset voltage (2)		$V_{DD} \geq$ 1.1 V, I_{OL} = 50 µA			0.2	V
V_{IT-}	Negative-going input threshold voltage (3)	TPS380x-01	T_A = -40°C to 85°C	1.117	1.14	1.163	V
		TPS380xE18		1.67	1.71	1.75	
		TPS380xJ25		2.2	2.25	2.3	
		TPS380xG27		2.45	2.5	2.55	
		TPS380xL30		2.58	2.64	2.7	
		TPS380xK33		2.87	2.93	2.99	
		TPS380xI50		4.45	4.55	4.65	
		TPS380xT50		3.92	4	4.08	
V_{hys}	Threshold hysteresis	TPS380x-01			15		mV
		TPS380xx18			25		
		TPS380xx25			30		
		TPS380xx27			35		
		TPS380xx30			35		
		TPS380xx33			40		
		TPS380xx50			60		
I_{IH}	High-level input current ($\overline{MR}$)		$\overline{MR}$ = 0.7×V_{DD}, V_{DD} = 6 V	-40	-60	-100	µA
I_{IL}	Low-level input current ($\overline{MR}$)		$\overline{MR}$ = 0 V, V_{DD} = 6 V	-130	-200	-340	
I_I	Input current (SENSE)			-25		25	nA
I_{DD}	Supply current	TPS3801J25, TPS3801L30, TPS3801K33, TPS3801I50, TPS3801T50	V_{DD} = 2 V, $\overline{MR}$ and output unconnected		9	12	µA
			V_{DD} = 6 V, $\overline{MR}$ and output unconnected		20	25	
		TPS3801-01	V_{DD} = 1.6 V, SENSE = 0 V to V_{DD}, output unconnected		7	10	
			V_{DD} = 4 V, SENSE = 0 V to V_{DD}, output unconnected		9	12	
		TPS3801E18, TPS3800G27, TPS3802K33, TPS3802L30	V_{DD} = 1.6 V, $\overline{MR}$ and output unconnected		8	11	
			V_{DD} = 4 V, $\overline{MR}$ and output unconnected		13	18	
C_i	Input capacitance		V_I = 0 V to V_{DD}		5		pF

(1) Only valid for the TPS3801J25, TPS3801L30, TPS3801K33, TPS3801I50, and TPS3801T50.
(2) The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,\ VDD} \geq$ 15 µs/V.
(3) To ensure the best stability of the threshold voltage, a bypass capacitor (0.1-µF ceramic) should be placed near the supply terminals.

TIMING REQUIREMENTS
at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

parameter		TEST CONDITIONS	min	TYP	max	unit
t_w Pulse width	at SENSE	V_{DD} = 1.6 V,V_{IH} = 1.1 × V_{IT-}, V_{IL} = 0.9 × V_{IT-}	1			µs
	at V_{DD}	V_{DD} = V_{IT-} + 0.2 V, V_{DD} = V_{IT-} -0.2 V	3			
	at $\overline{MR}$	$V_{DD} \geq V_{IT-}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	100			ns

SWITCHING CHARACTERISTICS

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

parameter		TEST CONDITIONS	min	TYP	max	unit
t_d $\overline{RESET}$ recovery delay time	TPS3801T50	$V_{DD} \geq V_{IT-}$ + 0.2 V, $\overline{MR} \geq$ 0.7 × V_{DD} See timing diagram	15	25	35	ms
	TPS3800		60	95	140	
	TPS3801		120	200	280	
	TPS3802		240	380	560	
t_{PHL} Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay	$V_{DD} \geq V_{IT-}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		15		ns
	V_{DD} to $\overline{RESET}$ delay	V_{IL} = V_{IT-} - 0.2 V, V_{IH} = V_{IT-} + 0.2 V		1		µs
	SENSE to $\overline{RESET}$					

FUNCTIONAL BLOCK DIAGRAM

FUNCTION/TRUTH TABLE, TPS380x

$\overline{MR}$	V_{DD}>V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

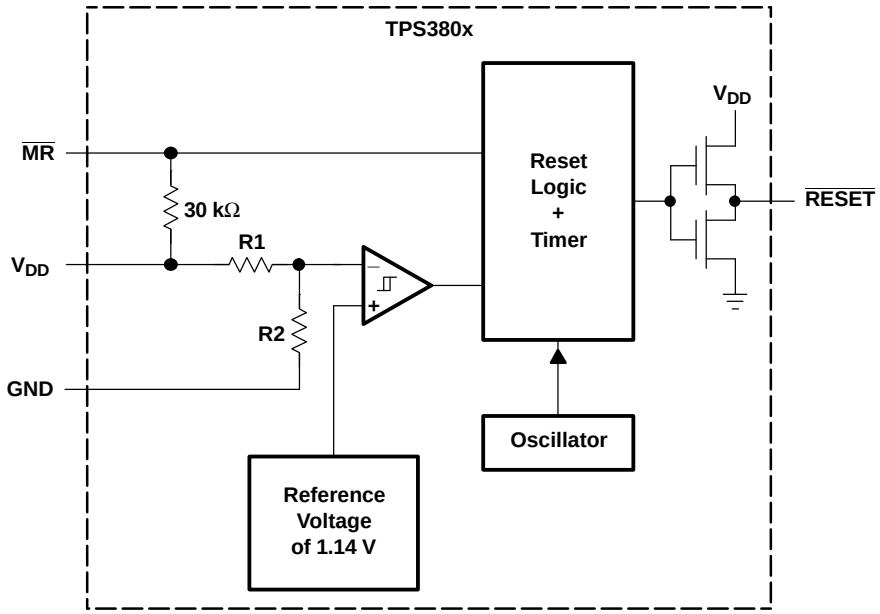


Figure 1. functional block diagram

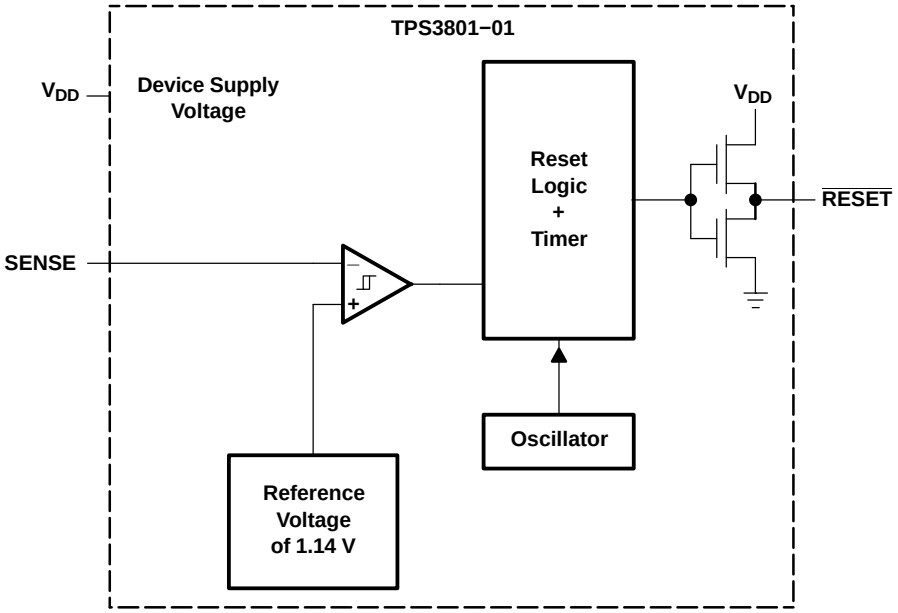
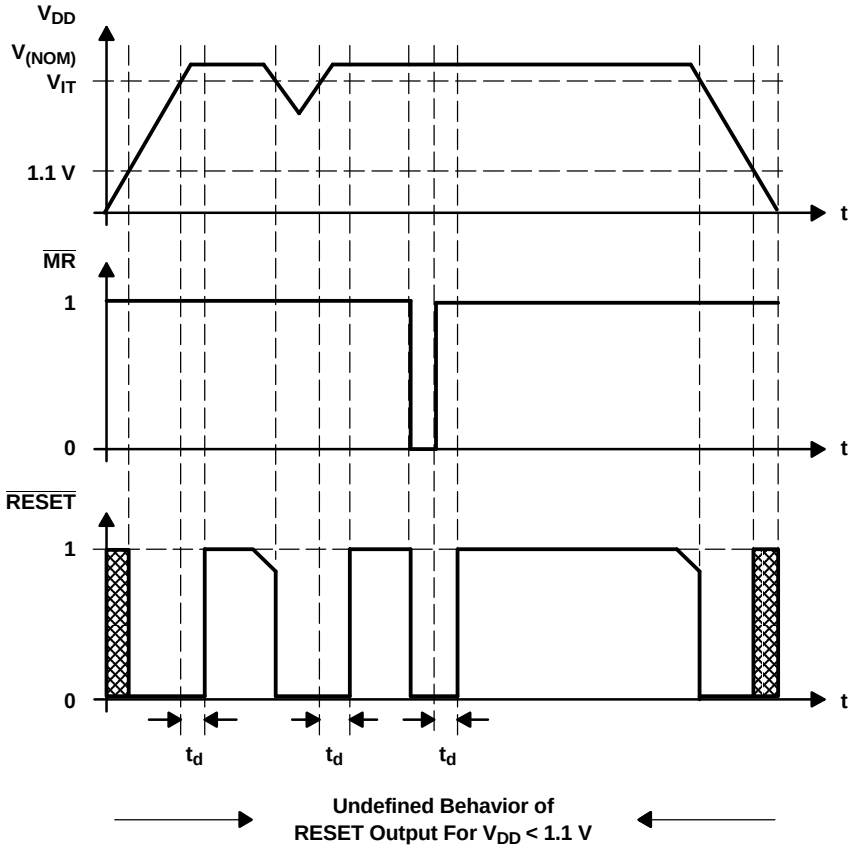


Figure 2. functional block diagram (continued)

TIMING DIAGRAM



NOTE: $\overline{\text{RESET}}$ should not be forced high during the power-up sequence (until V_{DD} > 1.1 V).

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

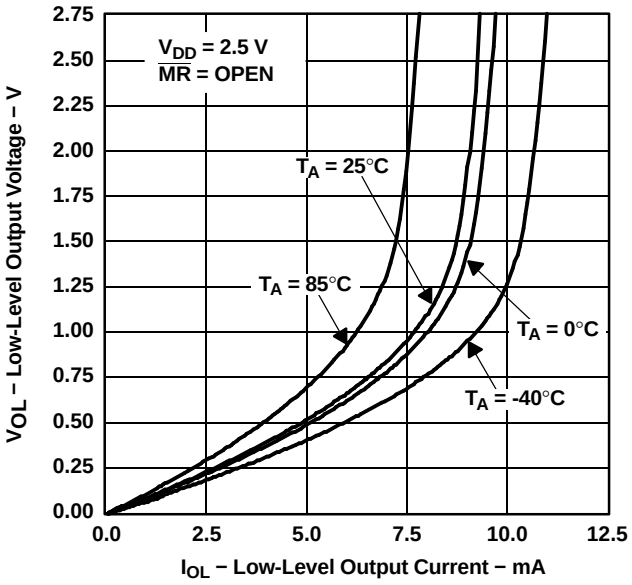


Figure 3.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

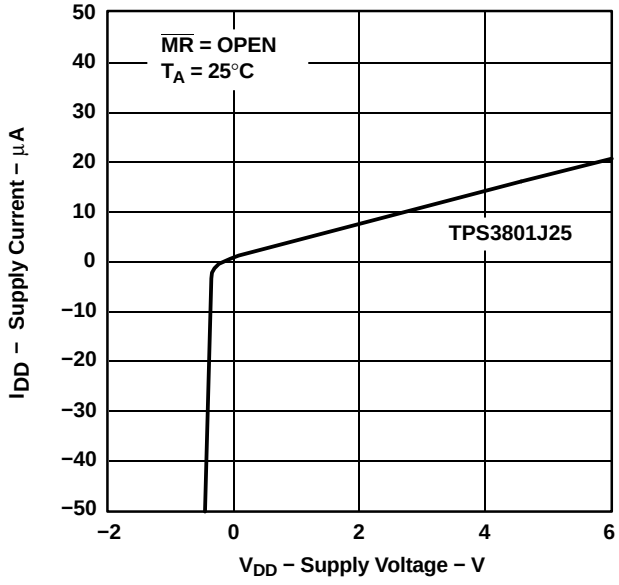


Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

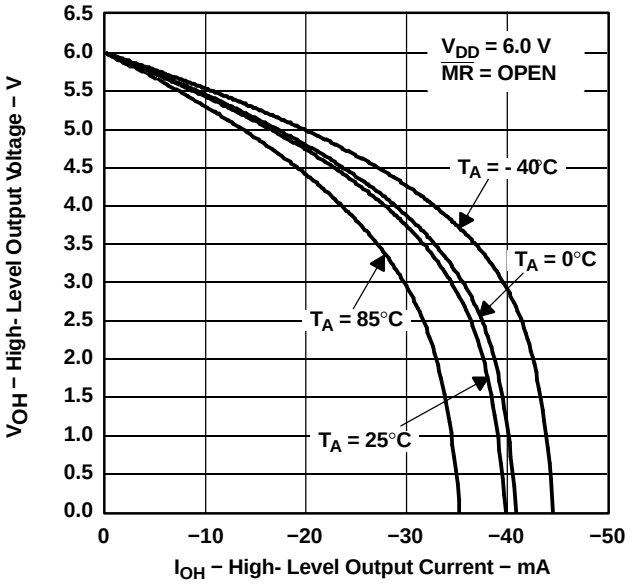


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

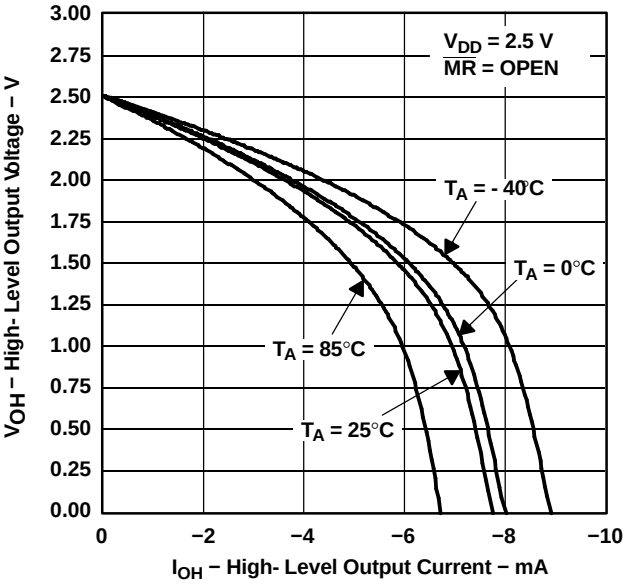


Figure 6.

TYPICAL CHARACTERISTICS (continued)

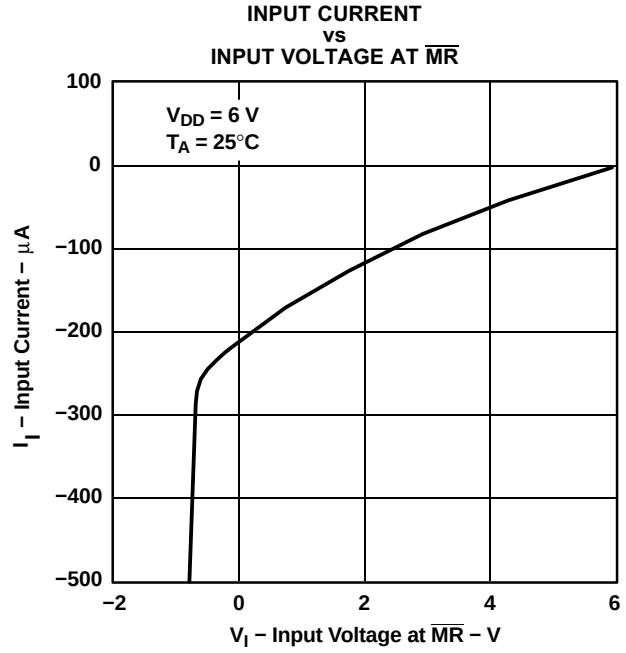


Figure 7.

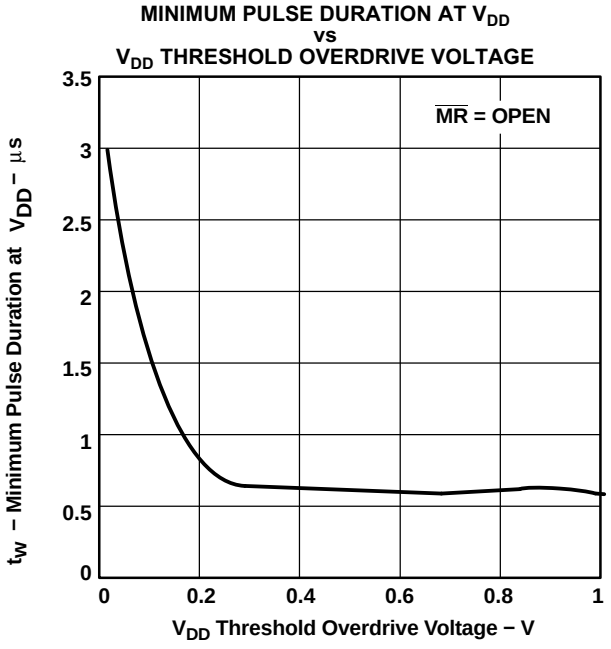


Figure 8.

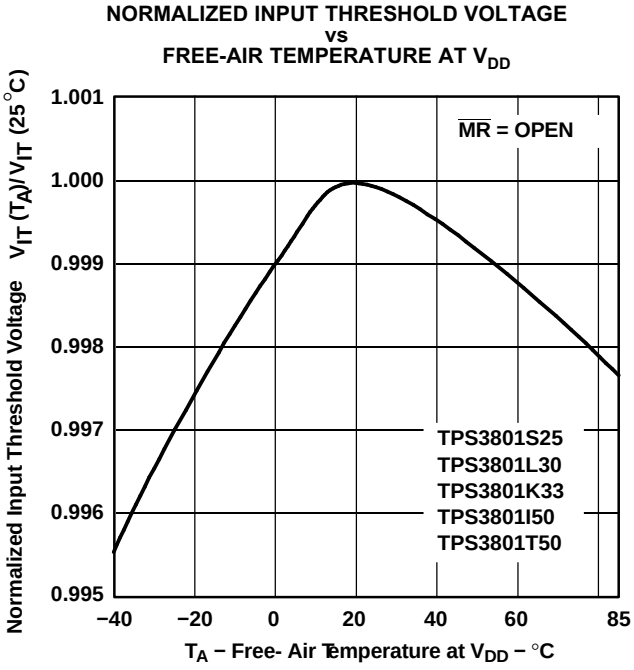


Figure 9.

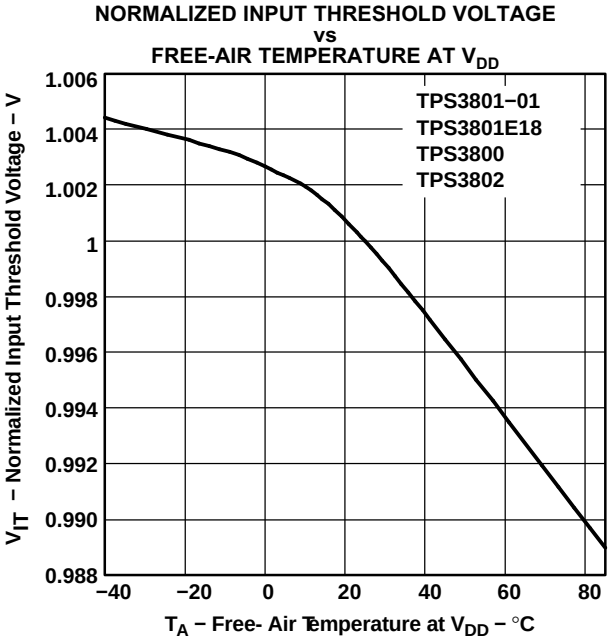


Figure 10.

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