64-Position OTP Digital Potentiometer

AD5273

FEATURES

64 Positions
OTP (One-Time-Programmable)[1] Set-and-Forget Resistance Setting—Low Cost Alternative Over EEMEM Unlimited Adjustments Prior to OTP Activation
1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ End-to-End Terminal Resistance
Compact SOT-23-8 Standard Package
Ultralow Power: I_{DD} = 5 μA Max
Fast Settling Time: t_S = 5 μs Typ in Power-Up
I²C® Compatible Digital Interface
Computer Software[2] Replaces μC in Factory Programming Applications
Wide Temperature Range: –40°C to +105°C
6 V Programming Voltage
Low Operating Voltage: 2.7 V to 5.5 V
OTP Validation Check Function

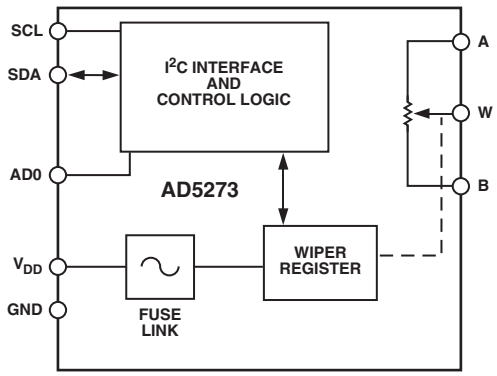
APPLICATIONS

Systems Calibrations
Electronics Level Settings
Mechanical Potentiometers and Trimmers Replacement
Automotive Electronics Adjustments
Transducer Circuits Adjustments
Programmable Filters up to 6 MHz BW[3]

GENERAL DESCRIPTION

The AD5273 is a 64-position, one-time-programmable (OTP) digital potentiometer[4] that employs fuse link technology to achieve the permanent program setting. This device performs the same electronic adjustment function as most mechanical trimmers and variable resistors. It allows unlimited adjustments before permanently setting the resistance values. The AD5273 is programmed using a 2-wire, I²C compatible digital control. During the write mode, a fuse blow command is executed after the final value is determined, thereby freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). When this permanent setting is achieved, the value will not change, regardless of the supply variations or environmental stresses under normal operating conditions. To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in the read mode.

FUNCTIONAL BLOCK DIAGRAM



In addition, for applications that program the AD5273 at the factory, Analog Devices offers device programming software[2] running on Windows NT®, 2000, and XP operating systems. This software application effectively replaces any external I²C controllers, which in turn enhances users' systems' time-to-market.

The AD5273 is available in 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ resistances, in a compact SOT-23 8-lead standard package, and operates from –40°C to +105°C.

Along with its unique OTP feature, the AD5273 lends itself well to general digital potentiometer applications due to its effective resolution, array resistance options, small footprint, and low cost.

An AD5273 evaluation kit and software are available. The kit includes the connector and cable that can be converted for factory programming applications.

For applications that require dynamic adjustment of resistance settings with nonvolatile EEMEM, users should refer to the AD523x and AD525x families of nonvolatile memory digital potentiometers.

NOTES
[1] One-Time-Programmable—unlimited adjustments before permanent setting.
[2] ADI cannot guarantee the software to be 100% compatible in all systems due to the wide variations in computer configurations.
[3] Applies to 1 kΩ parts only.
[4] The terms digital potentiometer, VR, and RDAC are used interchangeably.

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AD5273–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 2.7 V to 5.5 V, $V_A \le V_{DD}$, V_B = 0 V, –40°C < T_A < +105°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resolution	N				6	Bits
Resistor Differential NL[2]	R-DNL					
(10 kΩ, 50 kΩ, 100 kΩ)		R_{WB}, V_A = NC	–0.5	+0.05	+0.5	LSB
(1 kΩ)		R_{WB}, V_A = NC	–1	+0.25	+1	LSB
Resistor Nonlinearity[2]	R-INL					LSB
(10 kΩ, 50 kΩ, 100 kΩ)		R_{WB}, V_A = NC	–0.5	+0.10	+0.5	LSB
(1 kΩ)		R_{WB}, V_A = NC	–5	+2	+5	LSB
Nominal Resistance Tolerance[3]	$\Delta R_{AB}/R_{AB}$	T_A = 25°C				
(10 kΩ, 50 kΩ, 100 kΩ)			–30		+30	%
Nominal Resistance (1 kΩ)	R_{AB}		0.8	1.2	1.6	kΩ
Rheostat Mode Temperature Coefficient[4]	$(\Delta R_{AB}/R_{AB})/\Delta T$	Wiper = No Connect		300		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 3 V or 5 V		60	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[5]	DNL		–0.5	+0.1	+0.5	LSB
Integral Nonlinearity[5]	INL		–0.5		+0.5	LSB
Voltage Divider[4]						
Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x20		10		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x3F	–1		0	LSB
(10 kΩ, 50 kΩ, 100 kΩ)			–1		0	LSB
(1 kΩ)			–6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	–6		0	LSB
(10 kΩ, 50 kΩ, 100 kΩ)			0		1	LSB
(1 kΩ)			0		5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance[7] A, B	C_A, C_B	f = 5 MHz, Measured to GND, Code = 0x20		25		pF
Capacitance[7] W	C_W	f = 1 MHz, Measured to GND, Code = 0x20		55		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High (SDA and SCL)	V_{IH}		0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)	V_{IL}		–0.5		0.3 V_{DD}	V
Input Logic High (ADO)	V_{IH}		3.0		V_{DD}	V
Input Logic Low (ADO)	V_{IL}		0		0.4	V
Input Logic Current	I_{IL}	V_{IN} = 0 V or 5 V		0.01	1	µA
Input Capacitance[7]	C_{IL}			3		pF
Output Logic Low (SDA)	V_{OL}				0.4	V
Three-State Leakage Current	I_{OZ}				±1	µA
Output Capacitance[7]	C_{OZ}			3		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply[8]	V_{DD_OTP}	T_A = 25°C	6		6.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		0.1	5	µA
OTP Supply Current[9]	I_{DD_OTP}	T_A = 25°C, V_{DD} = 6 V	100			mA
Power Dissipation[10]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.2	0.03	mW
Power Supply Sensitivity	PSRR	R_{AB} = 1 kΩ	–0.3		+0.3	%/%
	PSRR	R_{AB} = 10 kΩ, 50 kΩ, 100 kΩ	–0.05		+0.05	%/%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS[7, 11, 12]						
Bandwidth –3 dB	BW_1 kΩ	R_{AB} = 1 kΩ, Code = 0x20		6000		kHz
	BW_10 kΩ	R_{AB} = 10 kΩ, Code = 0x20		600		kHz
	BW_50 kΩ	R_{AB} = 50 kΩ, Code = 0x20		110		kHz
	BW_100 kΩ	R_{AB} = 100 kΩ, Code = 0x20		60		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, R_{AB} = 1 kΩ, V_B = 0 V, f = 1 kHz		0.05		%
Adjustment Settling Time	t_{S1}	V_A = 5 V ± 1 LSB Error Band, V_B = 0, Measured at V_W		5		µs
OTP Settling Time[13]	t_{S_OTP}	V_A = 5 V ± 1 LSB Error Band, V_B = 0, Measured at V_W, V_{DD} = 6 V		400		ms
Power-Up Settling Time – Post Fuses Blown	t_{S2}	V_A = 5 V ± 1 LSB Error Band, V_B = 0, Measured at V_W		5		µs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 1 kΩ, f = 1 kHz, Code = 0x20		3		nV/√Hz
		R_{AB} = 20 kΩ, f = 1 kHz, Code = 0x20		13		nV/√Hz
		R_{AB} = 50 kΩ, f = 1 kHz, Code = 0x20		20		nV/√Hz
		R_{AB} = 100 kΩ, f = 1 kHz, Code = 0x20		28		nV/√Hz
INTERFACE TIMING CHARACTERISTICS (applies to all parts[7, 12, 14])						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;\,STA}$ Hold Time (repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;\,STA}$ Setup Time for START Condition	t_5		0.6			µs
$t_{HD;\,DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;\,DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL Signals	t_9				0.3	µs
$t_{SU;\,STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES

[1] Typicals represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

[3] V_{AB} = V_{DD}, Wiper (V_W) = No Connect.

[4] $\Delta R_{WB}/\Delta T = \Delta R_{WA}/\Delta T$. Temperature coefficient is code dependent; see the Typical Performance Characteristics.

[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[6] Resistor terminals A, B, and W have no limitations on polarity with respect to each other.

[7] Guaranteed by design and not subject to production test.

[8] Different from operating power supply, power supply for OTP is used one time only.

[9] Different from operating current, supply current for OTP lasts approximately 400 ms for the one time it is needed.

[10] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[11] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

[12] All dynamic characteristics use V_{DD} = 5 V.

[13] Different from settling time after fuses are blown. The OTP settling time occurs once only.

[14] See Figure 1 for location of measured values.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V, +6.5 V
V_A, V_B, V_W to GND . . . . . GND, V_{DD}
Maximum Current
  I_{WB}, I_{WA} Pulsed . . . . . ±20 mA
  I_{WB} Continuous ($R_{WB} \leq 1$ kΩ, A Open)[2] . . . . . ±4 mA
  I_{WA} Continuous ($R_{WA} \leq 1$ kΩ, B Open)[2] . . . . . ±4 mA
Digital Input and Output Voltage to GND . . . . . 0 V, V_{DD}
Operating Temperature Range . . . . . –40°C to +105°C
Maximum Junction Temperature ($T_{J\ MAX}$) . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . 220°C
Thermal Resistance[3] θ_{JA}, SOT-23 . . . . . 230°C/W

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[3] Package Power Dissipation = $(T_{J\ MAX} - T_A)/\theta_{JA}$.

ORDERING GUIDE

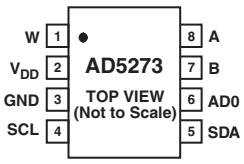
Model	Resistance R_{AB} (kΩ)	Package Option	Package Description	Number of Pieces on a REEL	Branding
AD5273BRJ1-R2	1	RJ-8	SOT-23	250	DYA
AD5273BRJ1-REEL7	1	RJ-8	SOT-23	3,000	DYA
AD5273BRJ10-R2	10	RJ-8	SOT-23	250	DYB
AD5273BRJ10-REEL7	10	RJ-8	SOT-23	3,000	DYB
AD5273BRJ50-R2	50	RJ-8	SOT-23	250	DYC
AD5273BRJ50-REEL7	50	RJ-8	SOT-23	3,000	DYC
AD5273BRJ100-R2	100	RJ-8	SOT-23	250	DYD
AD5273BRJ100-REEL7	100	RJ-8	SOT-23	3,000	DYD
AD5273EVAL	*	NA	Evaluation Board	*	NA

*Users should order samples additionally as the evaluation kit comes with a socket but does not include the parts.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5273 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

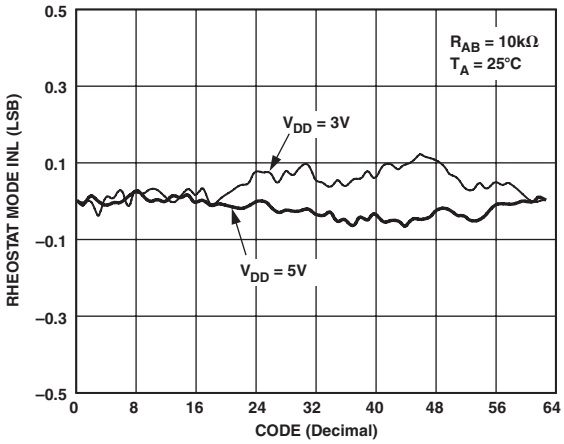
PIN CONFIGURATION



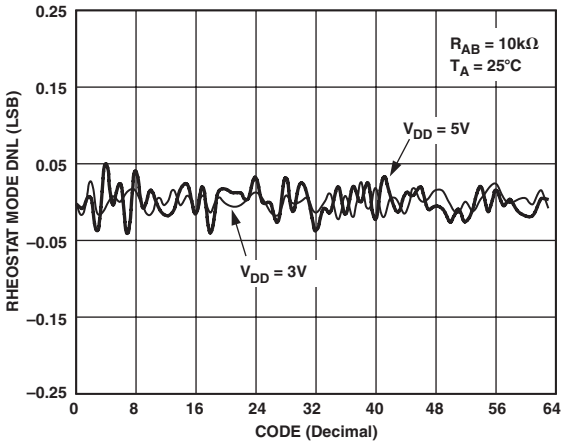
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	W	Wiper Terminal W. GND ≤ V_W ≤ V_{DD}.
2	V_{DD}	Positive Power Supply. Specified for non-OTP operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 6 V and 100 mA driving capability.
3	GND	Common Ground.
4	SCL	Serial Clock Input. Requires pull-up resistor.
5	SDA	Serial Data Input/Output. Requires pull-up resistor.
6	AD0	I^2C Device Address Bit. Allows maximum of two AD5273s to be addressed.
7	B	Resistor Terminal B. GND ≤ V_B ≤ V_{DD}.
8	A	Resistor Terminal A. GND ≤ V_A ≤ V_{DD}.

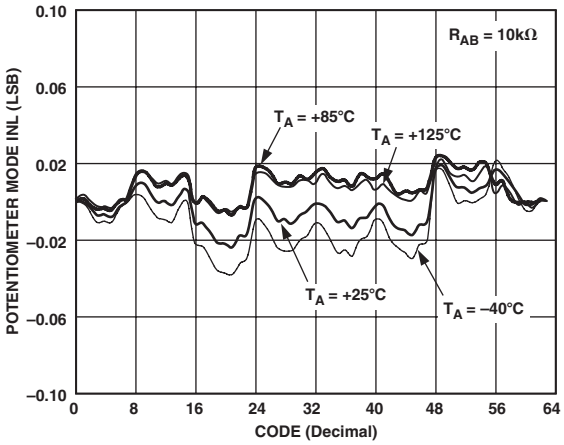
AD5273–Typical Performance Characteristics



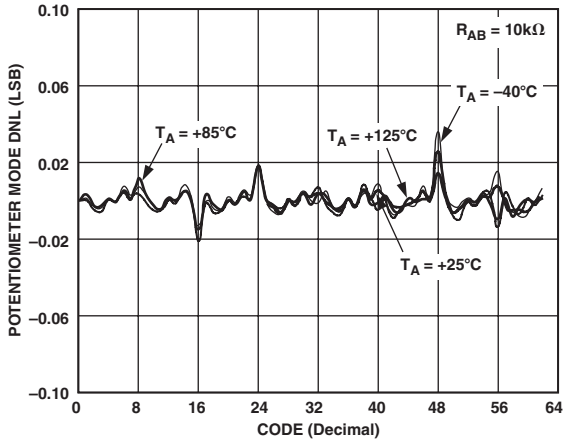
TPC 1. R_{INL} vs. Code vs. Supply Voltages



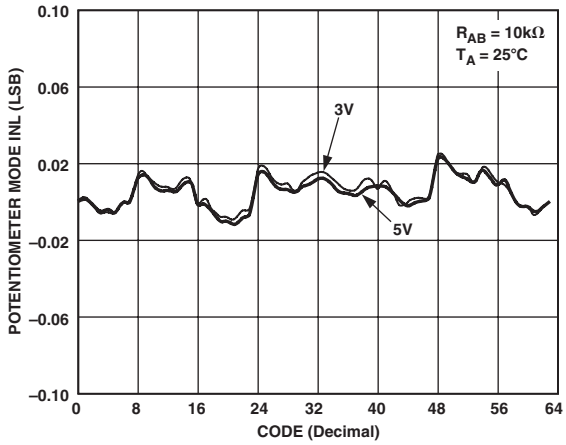
TPC 2. R_{DNL} vs. Code vs. Supply Voltages



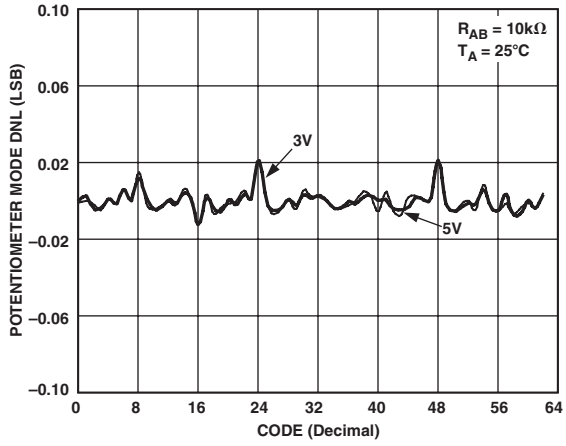
TPC 3. INL vs. Code vs. Temperature



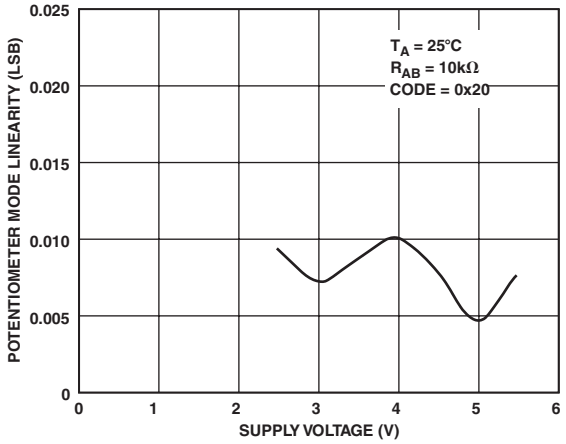
TPC 4. DNL vs. Code vs. Temperature



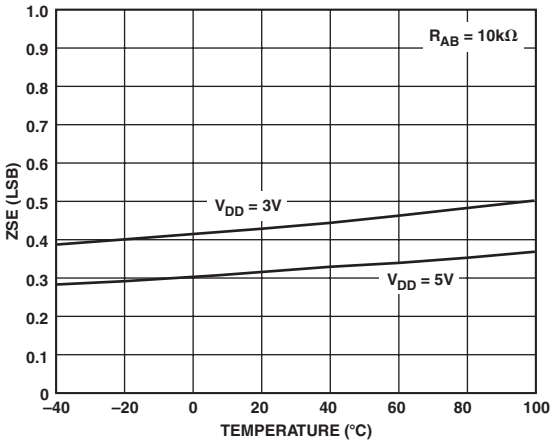
TPC 5. INL vs. Code vs. Supply Voltages



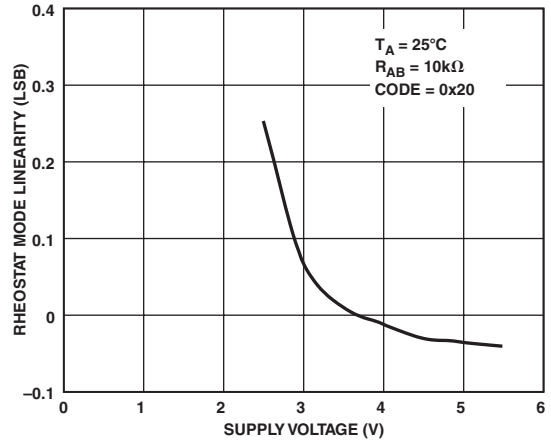
TPC 6. DNL vs. Code vs. Supply Voltages



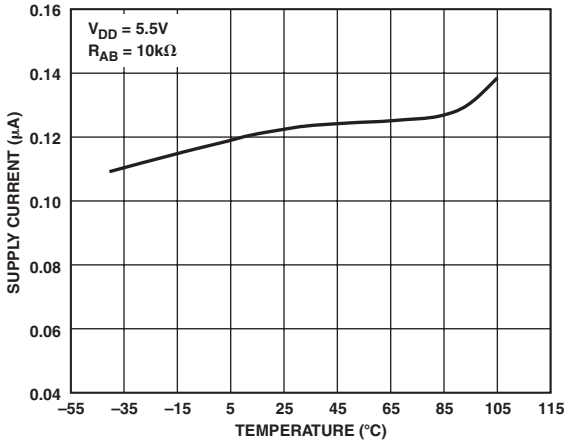
TPC 7. INL vs. Supply Voltage



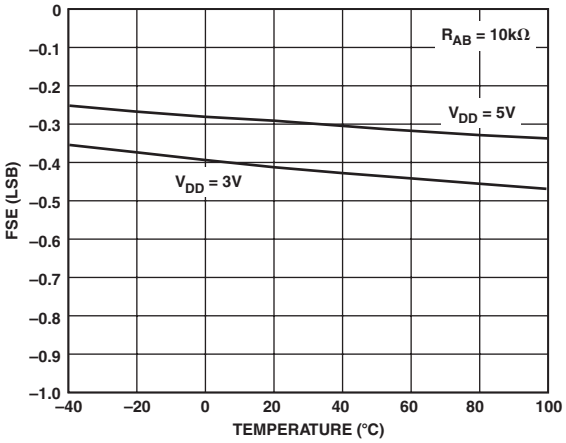
TPC 10. Zero-Scale Error



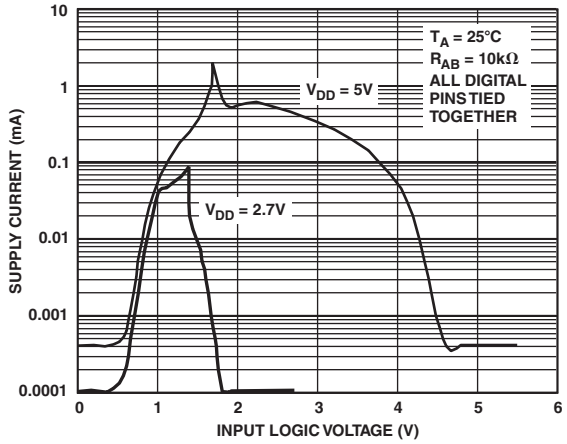
TPC 8. R_{INL} vs. Supply Voltage



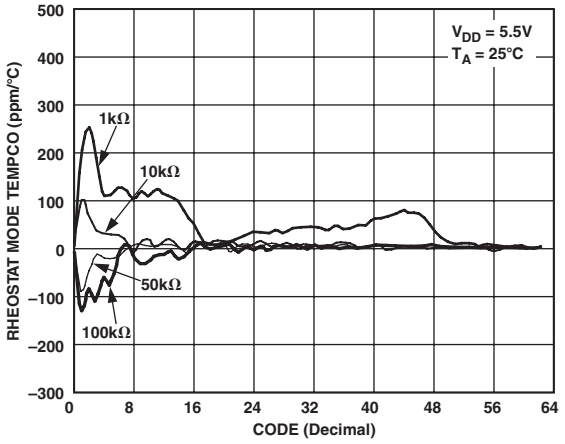
TPC 11. Supply Current vs. Temperature



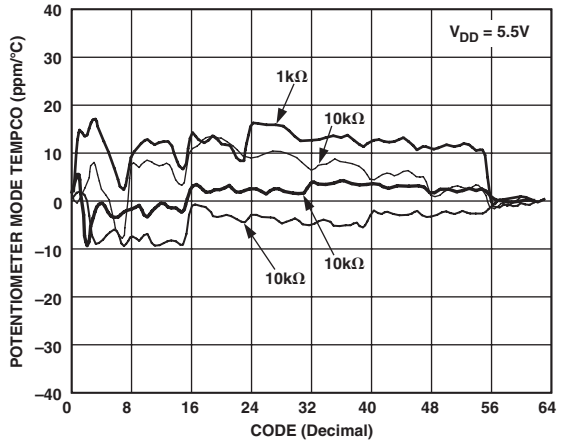
TPC 9. Full-Scale Error



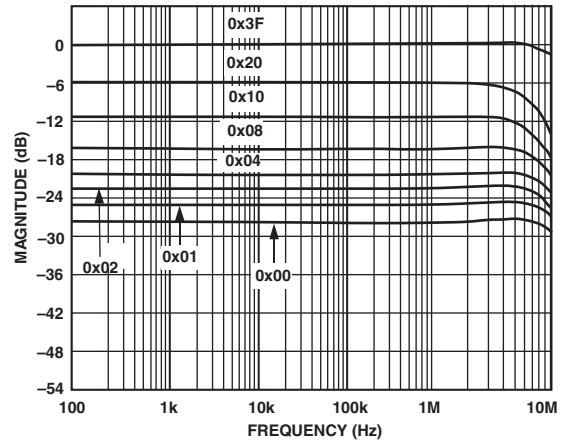
TPC 12. Supply Current vs. Digital Input Voltage



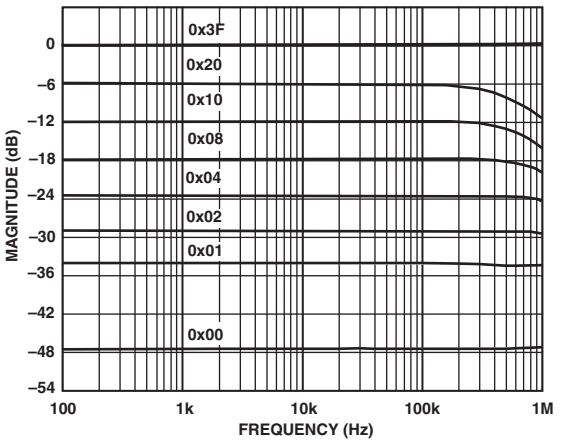
TPC 13. Rheostat Mode Tempco ($\Delta R_{WB}/R_{WB}$)/ΔT vs. Code



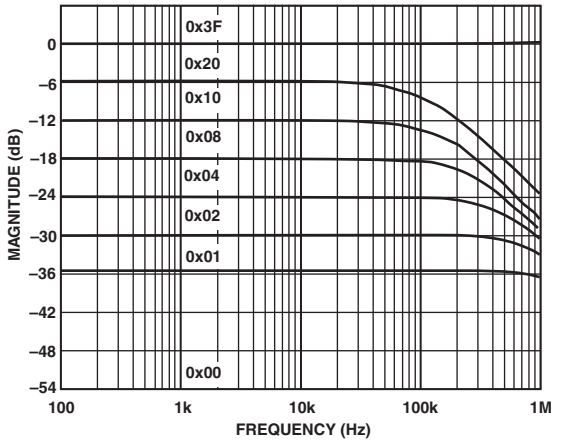
TPC 14. Potentiometer Mode Tempco ($\Delta V_W/V_W$)/ΔT vs. Code



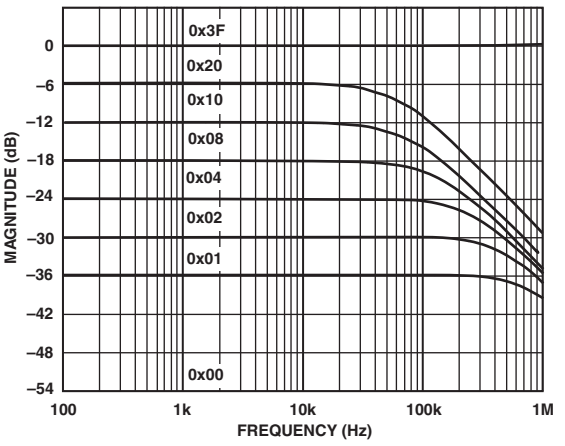
TPC 15. Gain vs. Frequency vs. Code, R_{AB} = 1 kΩ



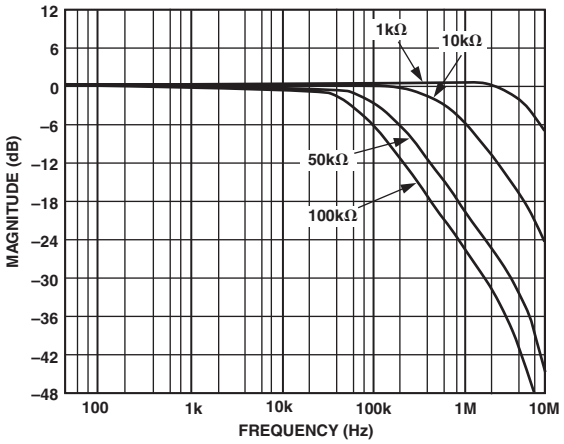
TPC 16. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ



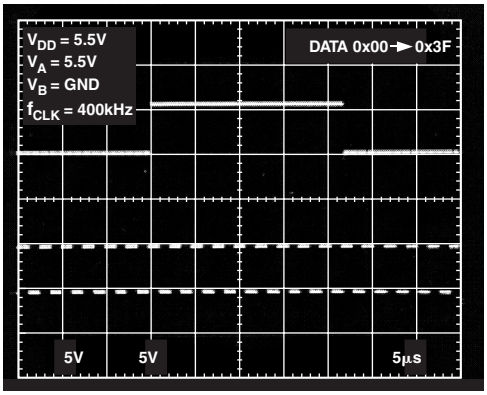
TPC 17. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ



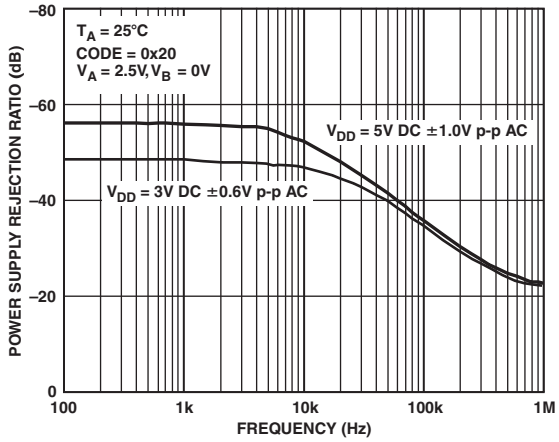
TPC 18. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ



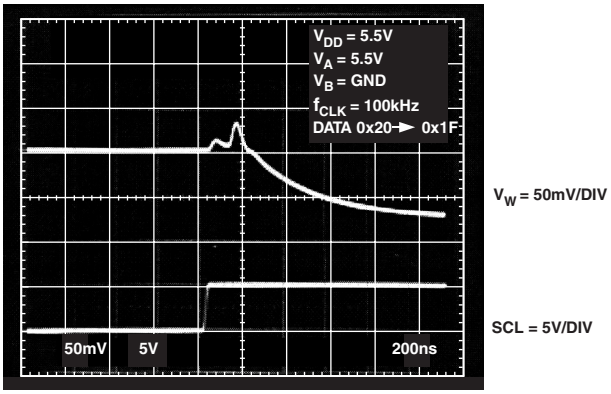
TPC 19. –3 dB Bandwidth



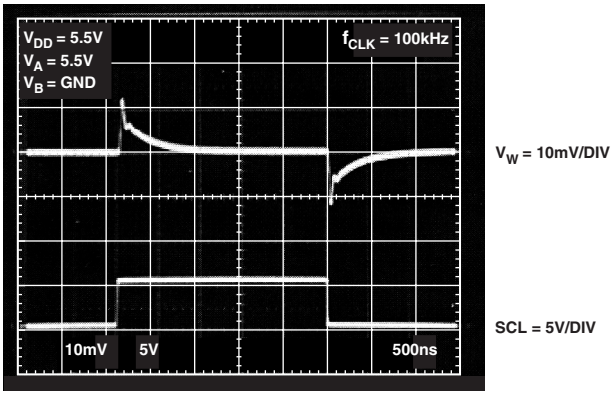
TPC 22. Large Settling Time



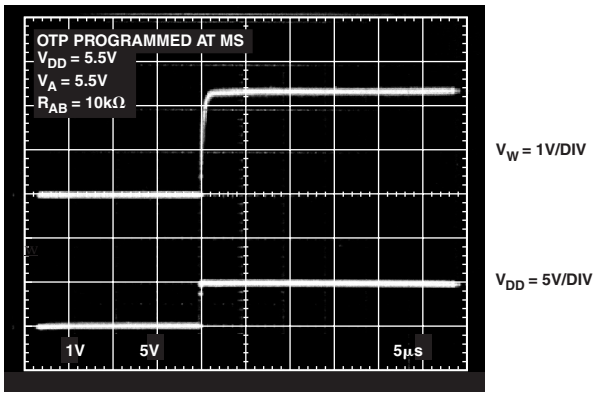
TPC 20. PSRR vs. Frequency



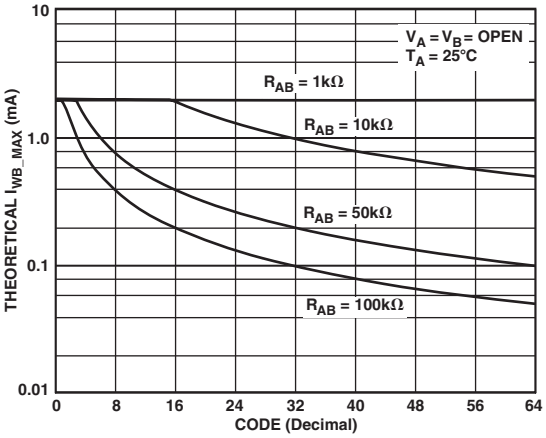
TPC 23. Midscale Glitch Energy



TPC 21. Digital Feedthrough



TPC 24. Power-Up Settling Time after Fuses Blown



TPC 25. I_{WB_MAX} vs. Code

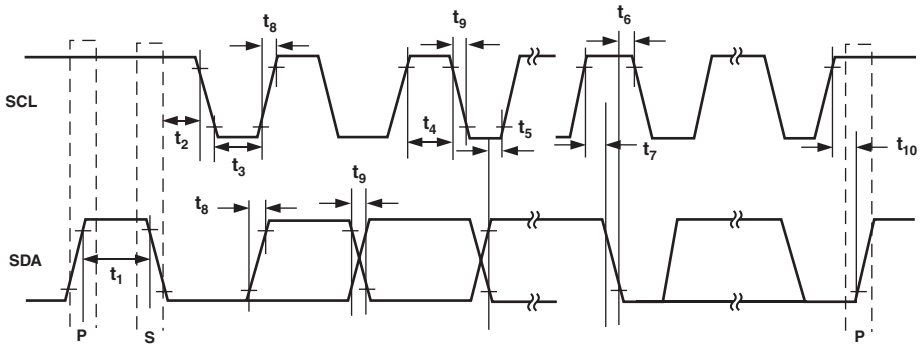


Figure 1. Interface Timing Diagram

Table I. SDA Write Mode Bit Format

S	0	1	0	1	1	0	AD0	0	A	T	X	X	X	X	X	X	X	A	X	X	D5	D4	D3	D2	D1	D0	A	P
	SLAVE ADDRESS BYTE									INSTRUCTION BYTE									DATA BYTE									

Table II. SDA Read Mode Bit Format

S	0	1	0	1	1	0	AD0	1	A	E1	E0	D5	D4	D3	D2	D1	D0	A	P
	SLAVE ADDRESS BYTE									DATA BYTE									

SDA BIT DEFINITIONS AND DESCRIPTIONS

S = Start Condition.

P = Stop Condition.

A = Acknowledge.

X = Don't Care.

T = OTP Programming Bit. Logic 1 programs wiper position permanently.

D5, D4, D3, D2, D1, D0 = Data Bits.

E1, E0 = OTP Validation Bits.

0, 0 = Ready to Program.

0, 1 = Test Fuse Not Blown Successfully. (For factory setup checking purpose only. Users should not see these combinations.)

1, 0 = Fatal Error. Do not retry. Discard the unit.

1, 1 = Programmed Successfully. No further adjustments possible.

AD0 = I^2C Device Address Bit. Allows maximum of two AD5273s to be addressed.

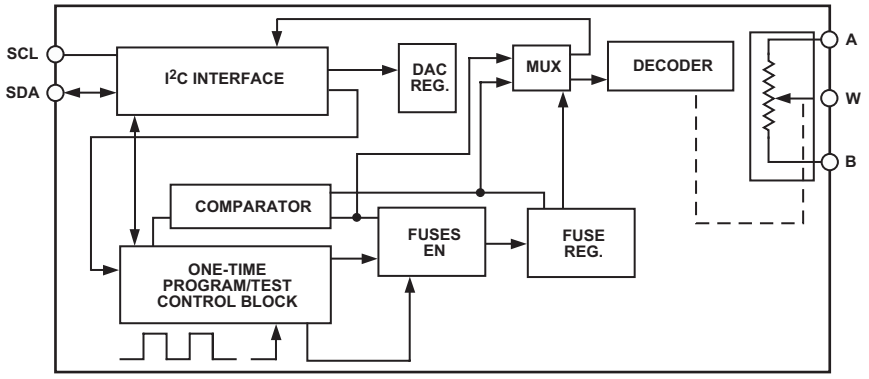


Figure 2. Detailed Functional Block Diagram

THEORY OF OPERATION

The AD5273 is a one-time-programmable (OTP), set-and-forget, 6-bit digital potentiometer. The AD5273 allows unlimited 6-bit adjustments prior to the OTP. OTP technology is a proven cost-effective alternative over EEMEM in one-time memory programming applications. The AD5273 employs fuse link technology to achieve the memory retention of the resistance setting function. It comprises six data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are programmed correctly.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5273 presets to midscale during power on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit to high along with the proper coding (Table I). Note that the fuse link technology requires 6 V to blow the internal fuses to achieve a given setting. The user is allowed only one attempt at blowing the fuses. Once programming is completed, the power supply voltage must be reduced to the normal operating range of 2.7 V to 5.5 V.

The device control circuit has two validation bits, E1 and E0, that can be read back in the read mode for checking the programming status as shown in Table III. Users should always read back the validation bits to ensure that the fuses are properly blown.

Table III. Validation Status

E1	E0	Status
0	0	Ready for Programming
0	1	Test Fuse Not Blown Successfully. (For factory setup checking purpose only. Users should not see these combinations.)
1	0	Fatal Error. Some fuses are not blown. Do not retry. Discard the unit.
1	1	Successful. No further programming is possible.

When the OTP T bit is set, the internal clock is enabled. The program will attempt to blow a test fuse. The operation stops if this fuse is not blown properly. The validation Bits E1 and E0 show 01. This status is intended for factory setup checking purpose only so users should not see such status. If the test fuse is blown successfully, the data fuses will be programmed next. The six data fuses will be programmed in six clock cycles. The output of the fuses is compared with the code stored in the DAC register. If they do not match, E1 and E0 of 10 are issued as a fatal error and the operation stops. Users should never try blowing the fuses for more than one attempt because the fuse structure may have changed that prohibits further programming. As a result, users must discard the unit. This error status can occur if the OTP supply voltage droops below 6 V, the OTP supply current is limited, or both the voltage and current ramp times are slow. If the output and stored code match, the programming lock fuse will be blown so that no further programming is possible. In the meantime, E1 and E0 will issue 11 indicating the lock fuse is blown successfully. All the fuse latches are enabled at power-on and therefore the output corresponds to the stored setting from this point on. Figure 2 shows a detailed functional block diagram.

DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE

Rheostat Mode Operation

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused terminal can be opened or shorted with W. This operation is called rheostat mode (Figure 3).

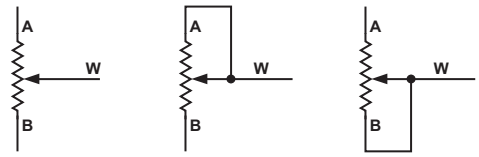


Figure 3. Rheostat Mode Configuration

The nominal resistance (R_{AB}) of the RDAC has 64 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is considered. The 6-bit data in the RDAC latch is decoded to select one of the 64 settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Such connection yields a minimum of 60 Ω resistance between terminals W and B because of the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 219 Ω (R_{WB} = (1) × R_{AB}/63 + R_W) for data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10060 Ω ((63) × R_{AB}/63 + R_W). Figure 4 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining R_{WB} is

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the 6-bit binary code.

R_{AB} is the end-to-end resistance.

R_W is the wiper resistance contributed by the on resistance of the internal switch.

Table IV. R_{WB} vs. Codes; R_{AB} = 10 kΩ and the A Terminal Is Opened

D (Dec)	R_{WB} (Ω)	Output State
63	10060	Full-Scale (R_{AB} + R_W)
32	5139	Midscale
1	219	1 LSB
0	60	Zero-Scale (Wiper Contact Resistance)

Since a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened or shorted to W. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{63 - D}{63} \times R_{AB} + R_W \quad (2)$$

Table V. R_{WA} vs. Codes; R_{AB} =10 kΩ and B Terminal Is Opened

D (Dec)	R_{WA} (Ω)	Output State
63	60	Full-Scale
32	4980	Midscale
1	9901	1 LSB
0	10060	Zero-Scale

The typical distribution of the resistance tolerance from device to device is process lot dependent, and it is possible to have ±30% tolerance.

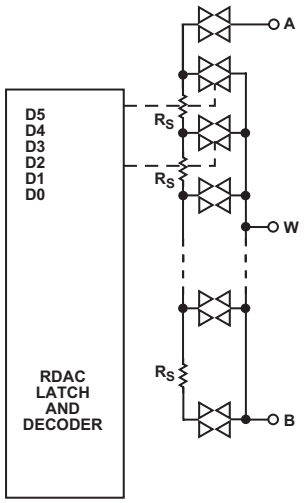


Figure 4. AD5273 Equivalent RDAC Circuit

Potentiometer Mode Operation

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (Figure 5).

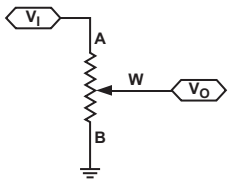


Figure 5. Potentiometer Mode Configuration

Ignoring the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{63} V_A \quad (3)$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{\frac{D}{63} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad (4)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratio-metric function of D/63 with a relatively small error contributed by the R_W terms, and therefore the tolerance effect is almost cancelled. Although the thin film step resistor R_S and CMOS switches resistance R_W have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where R_W dominates.

Potentiometer mode operations include others such as op amp input, feedback resistor networks, and other voltage scaling applications. A, W, and B terminals can in fact be input or output terminals provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed V_{DD} to GND.

ESD PROTECTION

Digital inputs SDA and SCL are protected with a series input resistor and parallel Zener ESD structures (Figure 6).

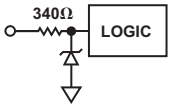


Figure 6. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

There are also ESD protection diodes between V_{DD} and the RDAC terminals. The V_{DD} of AD5273 therefore defines their voltage boundary conditions, see Figure 7. Supply signals present on terminals A, B, and W that exceed V_{DD} will be clamped by the internal forward-biased diodes and should be avoided.

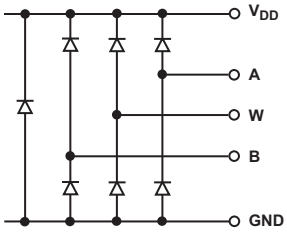


Figure 7. Maximum Terminal Voltages Set by VDD

POWER-UP/POWER-DOWN SEQUENCES

Similarly, because of the ESD protection diodes, it is important to power V_{DD} first before applying any voltages to terminals A, B, and W. Otherwise, the diode will be forward-biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuits. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}. Similarly, V_{DD} should be powered down last.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies are applied to the same V_{DD} terminal of the AD5273. The AD5273 employs fuse link technology that requires 6 V to blow the internal fuses to achieve a given setting. The user is allowed only one attempt at blowing the fuses. Once programming is complete, power supply voltage must be reduced to the normal operating range of 2.7 V to 5.5 V. Such dual voltage requires isolation between supplies. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 6 V and must be able to provide 100 mA transient current for 400 ms in order for successful one-time programming. Once programming is complete, the 6 V supply must be removed to allow normal operation of 2.7 V to 5.5 V at regular microamp current levels. Figure 8 shows the simplest implementation using a jumper. This approach saves one voltage supply but draws additional current and requires manual configuration.

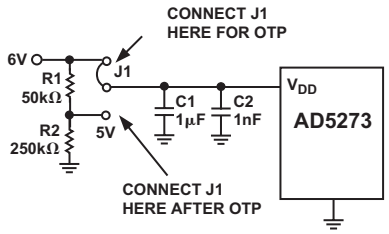


Figure 8. Power Supply Requirement

An alternate approach in 3.5 V to 5.5 V systems adds a signal diode between the system supply and the OTP supply for isolation, as shown in Figure 9.

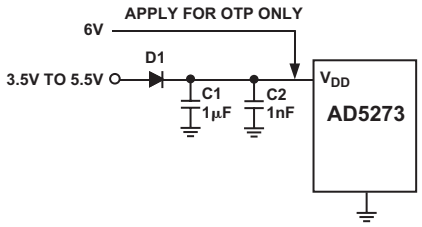


Figure 9. Isolating the 6 V OTP Supply from the 3.5 V to 5.5 V Normal Operating Supply. The 6 V supply must be removed once OTP is complete.

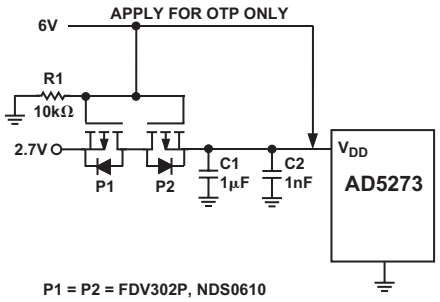


Figure 10. Isolating the 6 V OTP Supply from the 2.7 V Normal Operating Supply. The 6 V supply must be removed once OTP is complete.

For users who operate their systems at 2.7 V, it is recommended to use the bi-directional low threshold P-Ch MOSFETs for the supplies isolation. Figure 10 assumes that the 2.7 V system voltage is first applied. The gates of P1 are P2 are pulled to ground, which turns on P1 and subsequently P2. As a result, V_{DD} of AD5273 approaches 2.7 V. When the AD5273 setting is found, the factory tester applies the 6 V to V_{DD} and also to the gates of P1 and P2 to turn them off. While the OTP command is executing at this time to program AD5273, the 2.7 V source is therefore protected. Once the OTP is complete, the tester withdraws the 6 V, and AD5273 setting is permanently fixed.

The AD5273 achieves the OTP function through blowing internal fuses. Users should always apply the 6 V one-time program voltage requirement at the first program command. Noncompliance of such a requirement may lead to the change of the fuse structures, rendering inoperable programming.

Poor PCB layout introduces parasitic that may also affect the fuse programming. Therefore, it is recommended to add a 1 nF ceramic capacitor in parallel with 1 µF tantalum capacitor as close as possible to the V_{DD} pin. These capacitors provide the extra transient currents that make the PCB layout variations less sensitive to the OTP programming error.

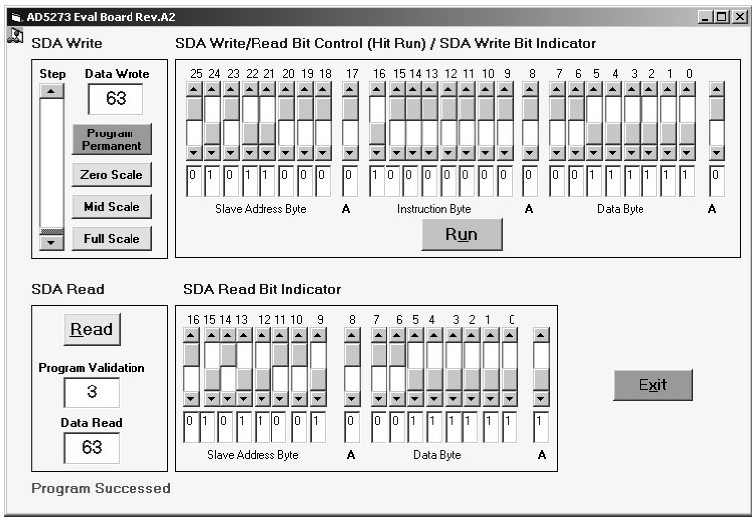


Figure 11. Computer Software

CONTROLLING THE AD5273

There are two ways of controlling the AD5273. Users can either program the device with computer software or with external I²C controllers.

Software Programming

Due to the advantage of the one-time programmable feature, most systems using the AD5273 will program the devices in the factory before shipping them to the end users. As a result, ADI offers device programming software that can be implemented in the factory on computers running Windows NT, 2000, and XP platforms. The software, which can be downloaded from the AD5273 product folder at www.analog.com is an executable file that does not require any programming languages or user programming skills. Figure 11 shows the software interface.

Write

The AD5273 starts at midscale after power-up prior to any OTP programming. To increment or decrement the resistance, the user may simply move the scrollbar on the left. Once the desired setting is found, the user can press the Program Permanent button to lock the setting permanently. To write any specific values, the user should use the bit pattern control in the upper screen and press the Run button. The format of writing data to the device is shown in Table I. Once the desired setting is found, the user can turn the T bit to 1 and press the Run button to program the setting permanently.

Read

To read the validation bits and data out from the device, the user can simply press the Read button. The user can also set the bit pattern in the upper screen and press the Run button. The format of reading data out from the device is shown in Table II.

In both read and write operations, the program generates the I²C digital signals through the parallel port LPT1 Pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively, to control the device (see Figure 12).

To apply the device programming software in the factory, users may lay out the AD5273 SCL and SDA pads on the PCB such that the programming signals can be communicated to and from the parallel port. Figure 13 shows a recommended AD5273 PCB layout into which pogo pins can be inserted for factory programming. To prevent damaging the PC parallel port, 100 Ω resistors should also be put in series to the SCL and SDA pins. Pull-up resistors on SCL and SDA are also required.

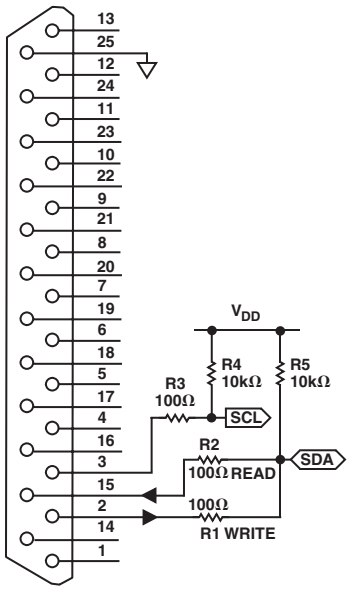


Figure 12. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND.

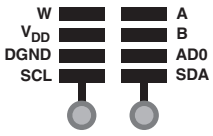


Figure 13. Recommended AD5273 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can communicate through the parallel port for programming. Refer to Figure 8.

I²C Controller Programming

Write Bit Pattern Illustrations

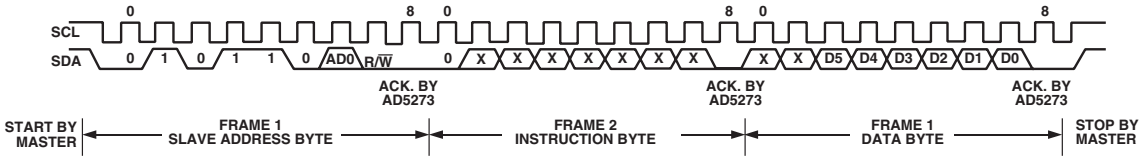


Figure 14a. Writing to the RDAC Register

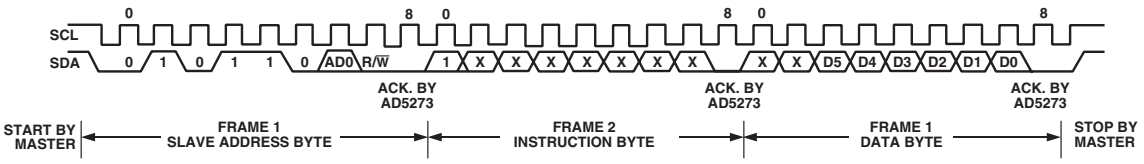


Figure 14b. Activating One-Time Programming

Read Bit Pattern Illustration

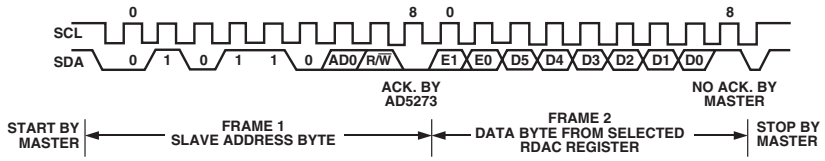


Figure 15. Reading Data from the RDAC Register

For users who do not use the software solution, the AD5273 can be controlled via an I²C compatible serial bus and is connected to this bus as a slave device. Referring to Figures 14a, 14b, and 15, the 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when SDA goes from high to low while SCL is high (Figure 14a). The following byte is the slave address byte, which consists of the six MSBs as slave address defined as 010110. The next bit is AD0; it is an I²C device address bit. Depending on the states of their AD0 bits, two AD5273s can be addressed on the same bus (see Figure 16). The last LSB is the R/$\overline{W}$ bit, which determines whether data will be read from or written to the slave device.

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. A write operation contains one more instruction byte than the read operation. The instruction byte in the write mode follows the slave address byte. The MSB of the instruction byte labeled T is the one-time programming bit. After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 14a).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference with the write mode, there are eight data bits followed by a no acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL as shown in Figure 11.

4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In the write mode, the master will pull the SDA line high during the 10th clock pulse to establish a stop condition (see Figures 14a and 14b). In the read mode, the master will issue a no acknowledge for the ninth clock pulse, i.e., the SDA line remains high. The master will then bring the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 15).

A repeated write function gives the user flexibility to update the RDAC output a number of times, except after permanent programming, after addressing and instructing the part only once. During the write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the write mode has to be started again with a new slave address, instruction, and data bytes. Similarly, a repeated read function of the RDAC is also allowed.

CONTROLLING TWO DEVICES ON ONE BUS

Figure 16 shows two AD5273 devices on the same serial bus. Each has a different slave address since the state of each AD0 pin is different. This allows each device to operate independently. The master device output bus line drivers are open-drain pull-downs in a fully I^2C compatible interface.

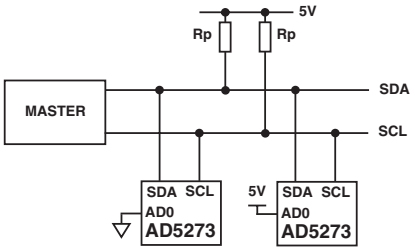


Figure 16. Two AD5273 Devices on One Bus

APPLICATIONS

Programmable Voltage Reference (DAC)

It is common to buffer the output of the digital potentiometer as a DAC unless the load is much larger than R_{WB}. The buffer serves the purpose of impedance conversion as well as delivering high current, which may be needed.

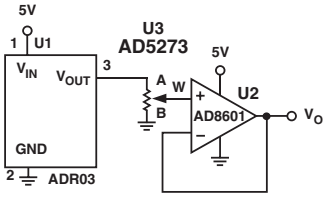


Figure 17. Programmable Voltage Reference (DAC)

Programmable Voltage Source with Boosted Output

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 18).

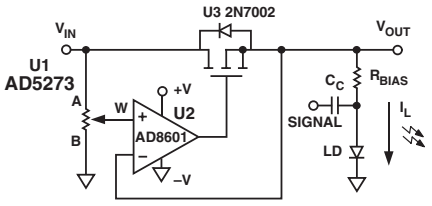


Figure 18. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N_1. N_1 power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference, such as the ADR421, ADR03, or ADR370, can be applied at the A terminal of the digital potentiometer.

Programmable Current Source

A programmable current source can be implemented with the circuit shown in Figure 19. The load current is simply the voltage across terminals B-to-W of the AD5273 divided by R_S. Notice that at zero-scale, the A terminal of the AD5273 will be at –2.048 V, which makes the wiper voltage clamped at ground potential. Dependent on the load, Equation 5 is therefore valid only at certain codes. For example, when the compliance voltage V_L equals half of the V_{REF}, the current can be programmed from midscale to full-scale of the AD5273.

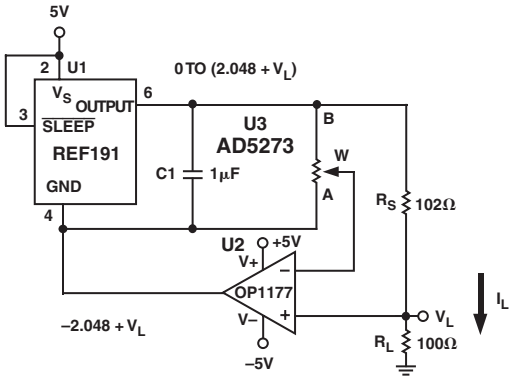


Figure 19. Programmable Current Source

$$I_L = \frac{(V_{REF} \times D)/64}{R_S} \Big| 32 \le D \le 63 \qquad (5)$$

Gain Control Compensation

As shown in Figure 20, the digital potentiometers are commonly used in gain controls or sensor transimpedance amplifier signal conditioning applications.

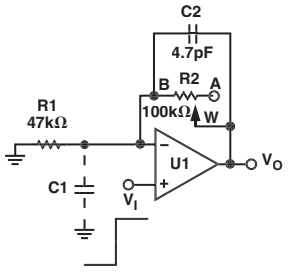


Figure 20. Typical Noninverting Gain Amplifier

In both applications, one of the digital potentiometer terminals is connected to the op amp inverting node with finite terminal capacitance C1. It introduces a zero for the 1 β_o term with 20 dB/dec, whereas a typical op amp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring, or in the worst case, oscillate when the input is a step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input. To reduce the effect of C1, users should also configure B or A rather than W terminal at the inverting node.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, one may use the relationship above and scale C2 as if R2 were at its maximum value. Doing so may overcompensate by slowing down the settling time when R2 is set at low values. As a result, C2 should be found empirically for a given application. In general, C2 in the range of a few picofarads to no more than a few tenths of a picofarad is adequate for the compensation.

There is also a W terminal capacitance connected to the output (not shown); its effect on stability is less significant so that the compensation may not be necessary unless the op amp is driving a large capacitive load.

Programmable Low-Pass Filter

In A/D conversion applications, it is common to include an anti-aliasing filter to band-limit the sampling signal. To minimize various system redesigns, users can use two 1 kΩ AD5273s to construct a generic second-order Sallen Key low-pass filter. Since the AD5273 is a single-supply device, the input must be dc offset when an ac signal is applied to avoid clipping at ground. This is illustrated in Figure 21. The design equations are

$$\frac{V_O}{V_I} = \frac{\omega_O{}^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O{}^2} \tag{6}$$

$$\omega_o = \sqrt{\frac{1}{R1R2C1C2}} \tag{7}$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \tag{8}$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where $Q = 0.707$, let $C1$ be twice the size of $C2$ and let $R1 = R2$. As a result, $R1$ and $R2$ can be adjusted to the same setting to achieve the desirable bandwidth.

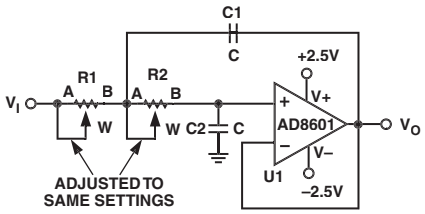


Figure 21. Sallen Key Low-Pass Filter

Level Shift for Different Voltages Operation

When users need to interface a 2.5 V controller with the AD5273, a proper voltage level shift must be employed so that the digital potentiometer can be read from or written to the controller; Figure 22 shows one of the implementations. M1 and M2 should be low threshold N-Ch power MOSFETs, such as the FDV301N.

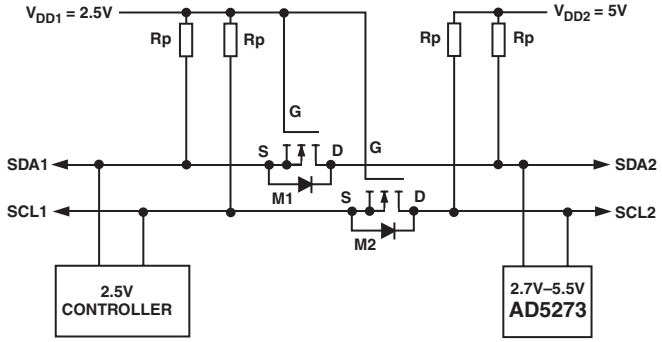


Figure 22. Level Shift for Different Voltage Operation

Resistance Scaling

The AD5273 offers 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ nominal resistances. For users who need to optimize the resolution with an arbitrary full-range resistance, the following techniques can be the solutions. Applicable only to the voltage divider mode, by paralleling a discrete resistor as shown in Figure 23, a proportionately lower voltage appears at terminal A–B. This translates into a finer degree of precision because the step size at terminal W will be smaller. The voltage can be found as

$$V_W(D) = \frac{(R_{AB} \,||\, R2)}{R3 + R_{AB} \,||\, R2} \times \frac{D}{63} \times V_{DD} \tag{9}$$

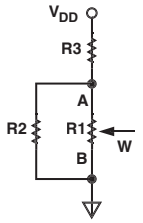


Figure 23. Lowering the Nominal Resistance

Figure 23 shows that the digital potentiometer changes steps linearly. On the other hand, log taper adjustment is usually preferred in applications like volume control. Figure 24 shows another way of resistance scaling. In this circuit, the smaller the R2 with respect to R_{AB}, the more it behaves like the pseudo log taper characteristic. The wiper voltage is simply

$$V_W(D) = \frac{(R_{WB}(D) \,||\, R2)}{R_{WA}(D) + R_{WB}(D) \,||\, R2} \times V_I \tag{10}$$

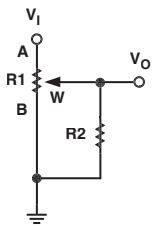


Figure 24. Resistor Scaling with Log Adjustment Characteristics

Resolution Enhancement

Borrowing from ADI's patented RDAC segmentation technique, users can configure three AD5273s to double the resolution (see Figure 25). First, U3 must be paralleled with a discrete resistor R_P that is chosen to be equal to a step resistance ($R_P = R_{AB}/64$). Adjusting U1 and U2 together forms the coarse 6-bit adjustment and adjusting U3 alone forms the finer 6-bit adjustment. As a result, the effective resolution becomes 12-bit.

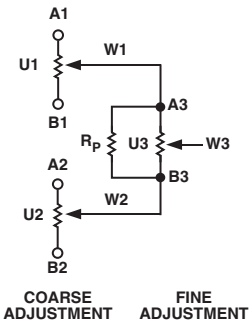


Figure 25. Double the Resolution in Rheostat Mode Operation

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentiometers. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5273 (1 kΩ resistor) measures 6 MHz at half scale. TPCs 15 to 18 provide the large signal BODE plot characteristics of the four available resistor versions 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. Figure 26 shows a parasitic simulation model. The code following Figure 26 provides a macro model net list for the 1 kΩ device.

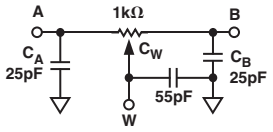


Figure 26. Circuit Simulation Model for RDAC = 1 kΩ

Macro Model Net List for RDAC

```
.PARAM D = 63, RDAC = 1E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A      0      25E-12
RWA     A      W      {(1-D/63)*RDAC+60}
CW      W      0      55E-12
RWB     W      B      {D/63*RDAC+60}
CB      B      0      25E-12
*
.ENDS DPOT
```

EVALUATION BOARD

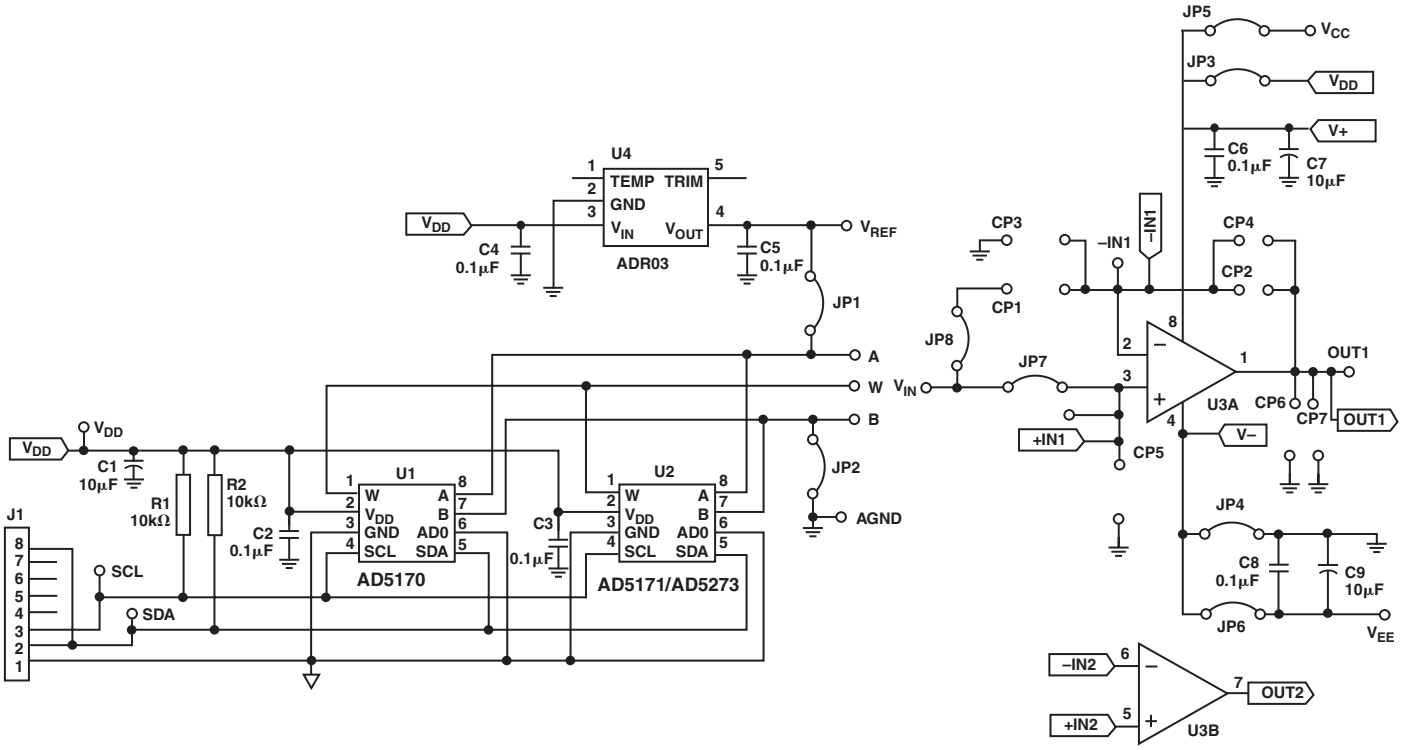


Figure 27. Evaluation Board Schematic

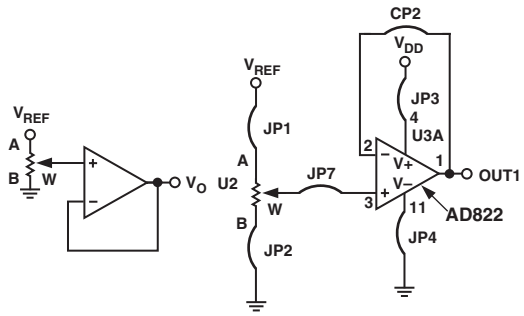


Figure 28. One of the Possible Configurations: Programmable Voltage Reference

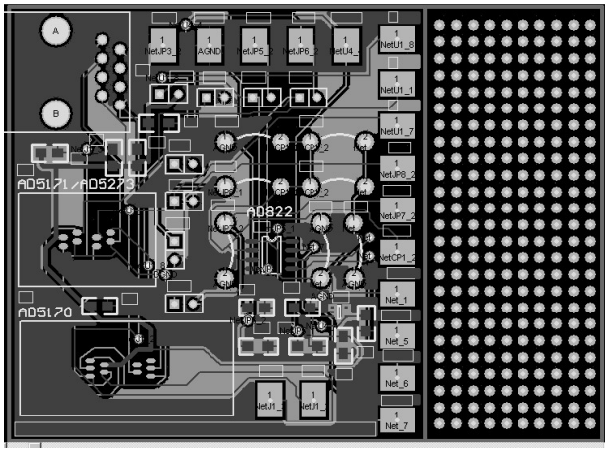
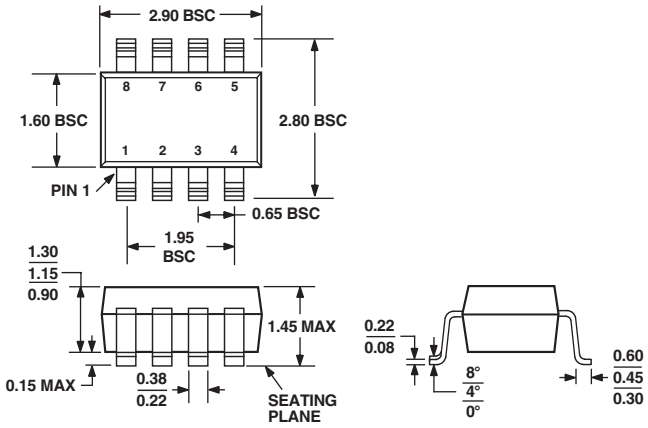


Figure 29. Evaluation Board

OUTLINE DIMENSIONS

8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178BA

Revision History

Location	Page
11/03—Data Sheet changed from REV. B to REV. C.	
Changes to SDA BIT DEFINITIONS AND DESCRIPTIONS	10
Changes to ONE-TIME PROGRAMMING (OTP) section	11
Changes to Table III	11
Changes to POWER SUPPLY CONSIDERATIONS	13
Changes to Figures 8, 9, and 10	13
10/03—Data Sheet changed from REV. A to REV. B	
Changes to FEATURES	1
Changes to APPLICATIONS	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to PIN FUNCTION DESCRIPTIONS	5
Changes to TPCs 7, 8, 13, and 14 captions	7
Deleted TPC 20; renumbered successive TPCs	9
Change to TPC 21 caption	9
Change to the SDA BIT DEFINITIONS AND DESCRIPTIONS	10
Replaced THEORY OF OPERATION section	11
Replaced DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE section	11
Replaced ESD PROTECTION section	12
Replaced TERMINAL VOLTAGE OPERATING RANGE section	12
Replaced POWER-UP SEQUENCE section	12
Replaced POWER SUPPLY CONSIDERATIONS section	13
Changes to APPLICATIONS section	16
Change to Equation 9	17
Deleted Digital Potentiometer Family Selection Guide	19
6/03—Data Sheet changed from REV. 0 to REV. A.	
Change to SPECIFICATIONS	2
Change to POWER SUPPLY CONSIDERATIONS section	12
Updated OUTLINE DIMENSIONS	20