

**FEATURES**

**0.4  $\Omega$  maximum on resistance @ 125°C**  
**0.08  $\Omega$  maximum on resistance flatness @ 125°C**  
**1.8 V to 5.5 V single supply**  
**Automotive temperature range from -40°C to +125°C**  
**400 mA current-carrying capability**  
**Tiny 6-lead SOT-23, 8-lead MSOP, and 6-ball WLCSP packages**  
**35 ns switching times**  
**Low power consumption**  
**TTL-/CMOS-compatible inputs**  
**Pin compatible with ADG701/ADG702**

**APPLICATIONS**

**Power routing**  
**Cellular phones**  
**Modems**  
**PCMCIA cards**  
**Hard drives**  
**Data acquisition systems**  
**Communications systems**  
**Relay replacement**  
**Battery-powered systems**

**GENERAL DESCRIPTION**

The ADG801 and ADG802 are monolithic CMOS, single-pole, single throw (SPST) switches with on resistance of less than 0.4  $\Omega$ . These switches are designed using an advanced submicron process that provides extremely low on resistance, high switching speed, and low leakage currents.

The low on resistance of <0.4  $\Omega$  makes these parts ideal for applications where low on resistance switching is critical.

The ADG801 switch is normally open (NO), while the ADG802 is normally closed (NC). Each switch conducts equally well in both directions when on.

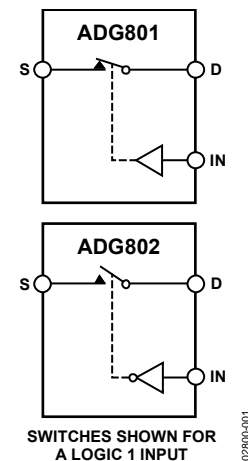
**FUNCTIONAL BLOCK DIAGRAM**

Figure 1.

**PRODUCT HIGHLIGHTS**

1. Low on resistance (0.25  $\Omega$  typical).
2. 1.8 V to 5.5 V single-supply operation.
3. Tiny 6-lead SOT-23, 8-lead MSOP, and 6-ball WLCSP packages.
4. 400 mA current-carrying capability.
5. Automotive temperature range from -40°C to +125°C.
6. Pin compatible with ADG701 (ADG801) and ADG702 (ADG802).

**Rev. A**

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

**TABLE OF CONTENTS**

Features .....	1	ESD Caution.....	5
Applications.....	1	Pin Configuration and Function Descriptions.....	6
Functional Block Diagram .....	1	Terminology .....	7
General Description .....	1	Typical Performance Characteristics .....	8
Product Highlights .....	1	Test Circuits.....	10
Revision History .....	2	Outline Dimensions .....	12
Specifications.....	3	Ordering Guide .....	14
Absolute Maximum Ratings.....	5		

**REVISION HISTORY**

**3/07—Rev. 0 to Rev. A**

Updated Format .....	Universal
Added 6-Ball WLCSP Package (Text and Figures) .....	Universal
Replaced Typical Performance Characteristics Section .....	8
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	14

**5/02—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted. The automotive temperature range is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C <sup>1</sup>	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analogue Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.25			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$ ; Test Circuit 1
	0.3	0.35	0.4	$\Omega$ max	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$ ; Test Circuit 1
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.05			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$
		0.07	0.08	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 30$	nA max	$V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
Drain Off Leakage, $I_D$ (Off)	$\pm 0.01$			nA typ	$V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 30$	nA max	$V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.01$			nA typ	$V_S = V_D = 1\text{ V}$ , or $4.5\text{ V}$ ; Test Circuit 3
	$\pm 0.25$	$\pm 3$	$\pm 30$	nA max	$V_S = V_D = 1\text{ V}$ , or $4.5\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	35			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	45	50	55	ns max	$V_S = 3\text{ V}$ ; Test Circuit 4
$t_{OFF}$	9			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	15	18	21	ns max	$V_S = 3\text{ V}$ ; Test Circuit 4
Charge Injection	50			pC typ	$V_S = 2.5\text{ V}$ , $R_S = 0\ \Omega$ ; $C_L = 1\text{ nF}$ ; Test Circuit 5
Off Isolation	-61			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; $f = 100\text{ kHz}$ ; Test Circuit 6
Bandwidth -3 dB	12			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 7
$C_S$ (Off)	180			pF typ	$f = 1\text{ MHz}$
$C_D$ (Off)	180			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	420			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V
		1.0	2.0	$\mu\text{A}$ max	

<sup>1</sup> On resistance parameters tested with  $I_S = 10\text{ mA}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG801/ADG802

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. The automotive temperature range is  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ .

**Table 2.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C <sup>1</sup>	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.4			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$ ; Test Circuit 1
	0.6	0.65	0.7	$\Omega$ max	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$ ; Test Circuit 1
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.1	0.1	0.1	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 3.3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3.3\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 30$	nA max	$V_S = 3.3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3.3\text{ V}$ ; Test Circuit 2
Drain Off Leakage, $I_D$ (Off)	$\pm 0.01$			nA typ	$V_S = 3.3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3.3\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 30$	nA max	$V_S = 3.3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3.3\text{ V}$ ; Test Circuit 2
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.01$			nA typ	$V_S = V_D = 1\text{ V}$ , or $3.3\text{ V}$ ; Test Circuit 3
	$\pm 0.25$	$\pm 3$	$\pm 30$	nA max	$V_S = V_D = 1\text{ V}$ , or $3.3\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	40			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	55	60	65	ns max	$V_S = 1.5\text{ V}$ ; Test Circuit 4
$t_{OFF}$	9			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	15	18	21	ns max	$V_S = 1.5\text{ V}$ ; Test Circuit 4
Charge Injection	10			pC typ	$V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 5
Off Isolation	-61			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; Test Circuit 6
Bandwidth -3 dB	12			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 7
$C_S$ (Off)	180			pF typ	$f = 1\text{ MHz}$
$C_D$ (Off)	180			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	420			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V
		1.0	2.0	$\mu\text{A}$ max	

<sup>1</sup> On resistance parameters tested with  $I_S = 10\text{ mA}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
Analog Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, Pin S or Pin D	400 mA
Peak Current, Pin S or Pin D	800 mA, pulsed at 1 ms, 10% duty cycle max
Operating Temperature Range Automotive	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ( $T_{JMAX}$ )	150°C
Package Power Dissipation MSOP	$(T_{JMAX} - T_A)/\theta_{JA}$
$\theta_{JA}$ Thermal Impedance	206°C/W
$\theta_{JC}$ Thermal Impedance SOT-23 (4-Layer Board)	44°C/W
$\theta_{JA}$ Thermal Impedance	119°C/W
$\theta_{JC}$ Thermal Impedance WLCSP (4-Layer Board)	91.99°C/W
$\theta_{JA}$ Thermal Impedance	120°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

<sup>1</sup> Overvoltages at Pin IN, Pin S, or Pin D are clamped by internal diodes. Current should be limited to the maximum ratings provided.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3. Truth Table**

ADG801 (Pin IN)	ADG802 (Pin IN)	Switch Condition
0	1	Off
1	0	On

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

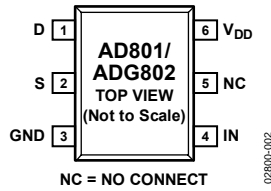


Figure 2. 6-Lead SOT-23 (RJ-6)

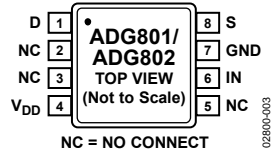


Figure 3. 8-Lead MSOP (RM-8)

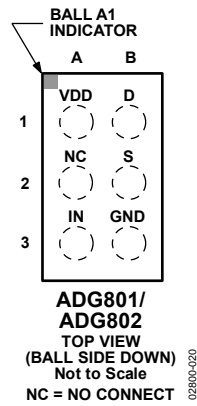


Figure 4. 6-Ball 2 × 3 WLCSP (CB-6-1)

Table 4. Pin Function Descriptions

SOT-23	Pin Number		Mnemonic	Description
	MSOP	WLCSP		
1	1	B1	D	Drain Terminal. Can be an input or an output.
2	8	B2	S	Source Terminal. Can be an input or an output.
3	7	B3	GND	Ground (0 V) Reference.
4	6	A3	IN	Logic Control Input.
5	2, 3, 5	A2	NC	Most Positive Power Supply Potential.
6	4	A1	V <sub>DD</sub>	Most Positive Power Supply Potential.

## TERMINOLOGY

### $V_{DD}$

The most positive power supply potential.

### $I_{DD}$

Positive supply current.

### GND

Ground (0 V) reference.

### S

The source terminal can be an input or an output.

### D

The drain terminal can be an input or an output.

### IN

Logic control input.

### $V_D$ ( $V_S$ )

Analog voltage on Terminal D and Terminal S.

### $R_{ON}$

Ohmic resistance between Terminal D and Terminal S.

### $R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

### $I_S$ (Off)

Source leakage current with the switch off.

### $I_D$ (Off)

Drain leakage current with the switch off.

### $I_D, I_S$ (On)

Channel leakage current with the switch on.

### $V_{INL}$

Maximum input voltage for Logic 0.

### $V_{INH}$

Minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

Input current of the digital input.

### $C_S$ (Off)

The off switch source capacitance is measured with reference to ground.

### $C_D$ (Off)

The off switch drain capacitance is measured with reference to ground.

### $C_D, C_S$ (On)

The on switch capacitance is measured with reference to ground.

### $C_{IN}$

Digital input capacitance.

### $t_{ON}$

The delay between applying the digital control input and when the output switches on. See Figure 17.

### $t_{OFF}$

The delay between applying the digital control input and when the output switches off.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

### Insertion Loss

The loss due to the on resistance of the switch.

## TYPICAL PERFORMANCE CHARACTERISTICS

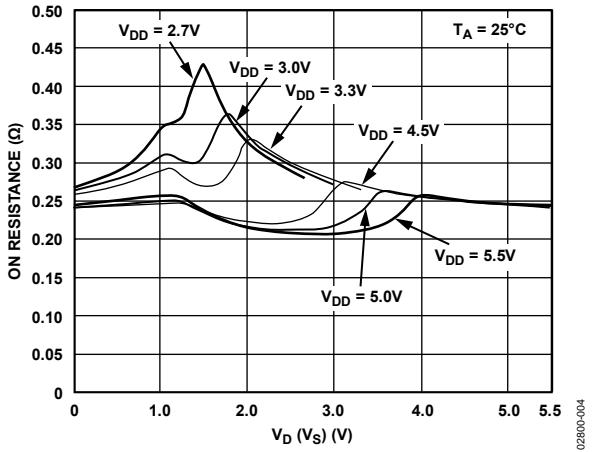


Figure 5. On Resistance vs. V<sub>D</sub> (V<sub>S</sub>)

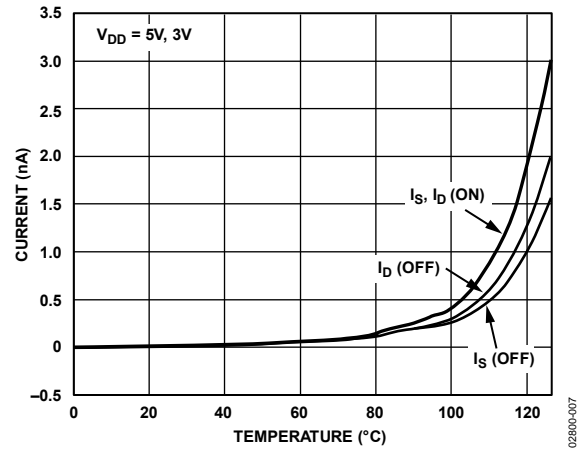


Figure 8. Leakage Current vs. Temperature

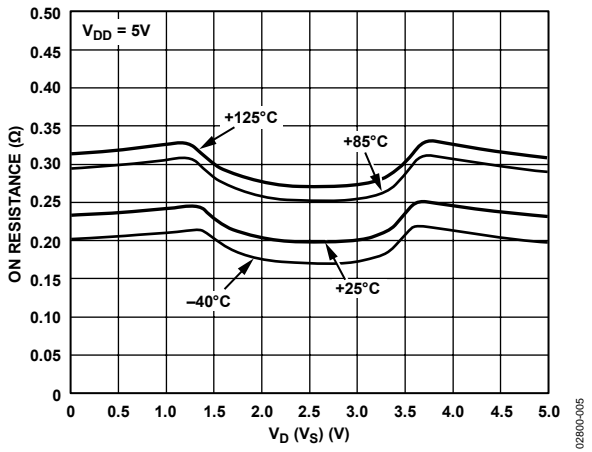


Figure 6. On Resistance vs. V<sub>D</sub> (V<sub>S</sub>) for Different Temperatures

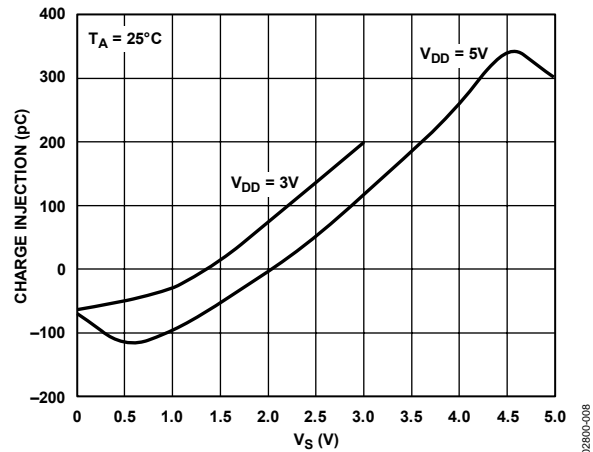


Figure 9. Charge Injection vs. Source Voltage

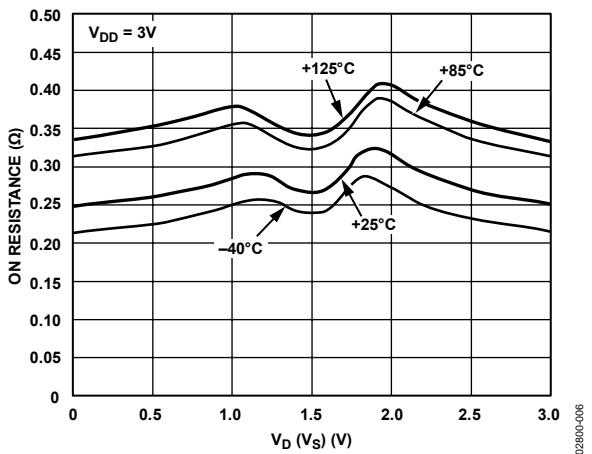


Figure 7. On Resistance vs. V<sub>D</sub> (V<sub>S</sub>) for Different Temperatures

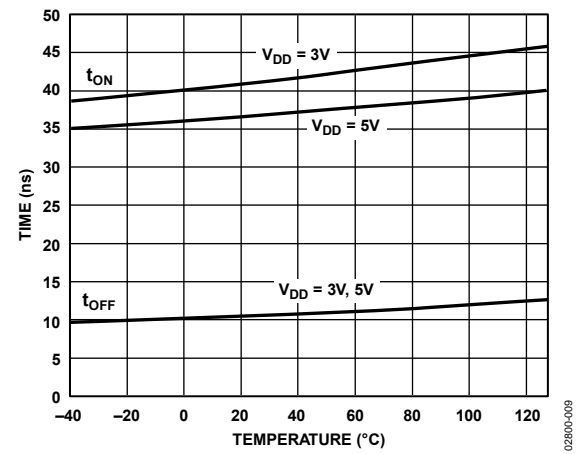


Figure 10. t<sub>ON</sub>/t<sub>OFF</sub> Times vs. Temperature



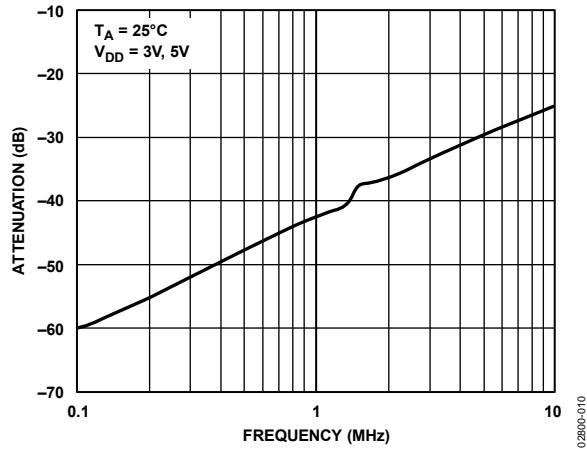


Figure 11. Off Isolation vs. Frequency

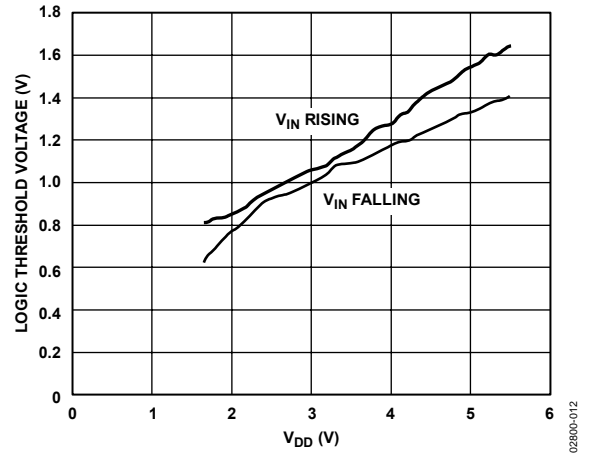


Figure 13. Logic Threshold Voltage vs. Supply Voltage

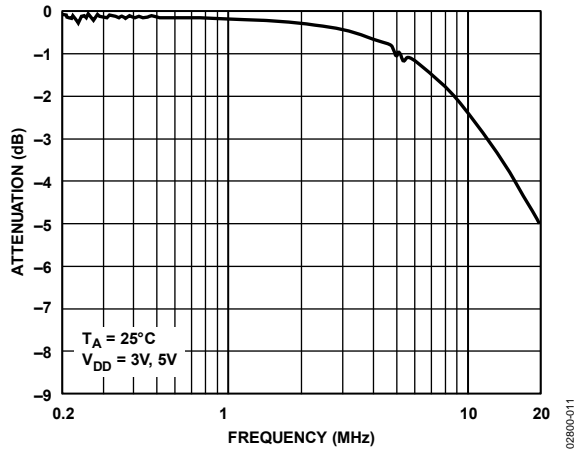


Figure 12. On Response vs. Frequency

## TEST CIRCUITS

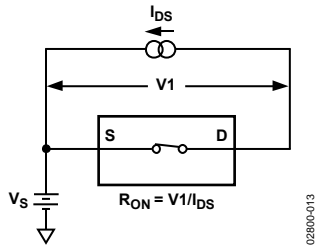


Figure 14. On Resistance

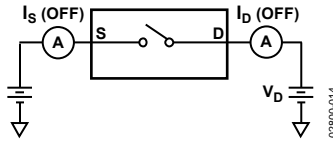


Figure 15. Off Leakage

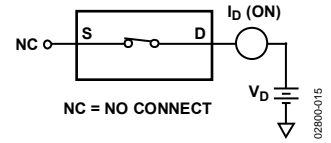


Figure 16. On Leakage

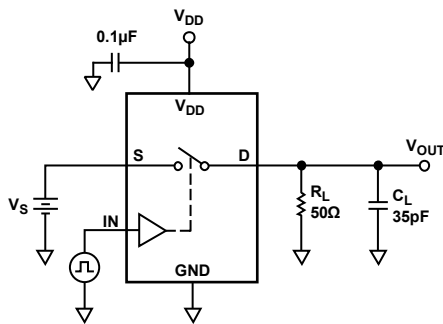


Figure 17. Switching Times

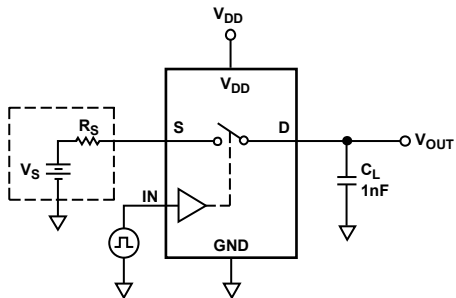
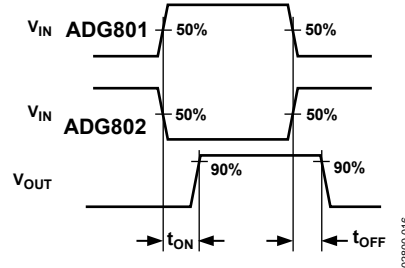
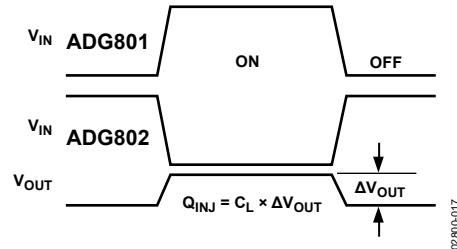


Figure 18. Charge Injection



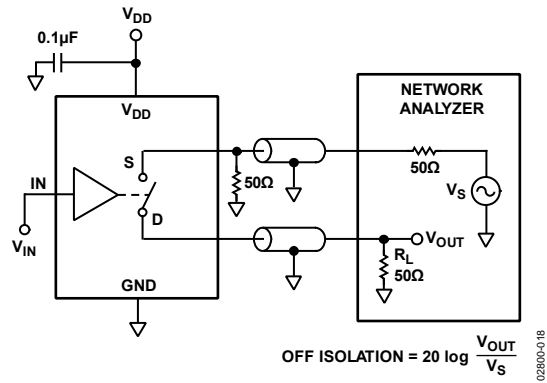


Figure 19. Off Isolation

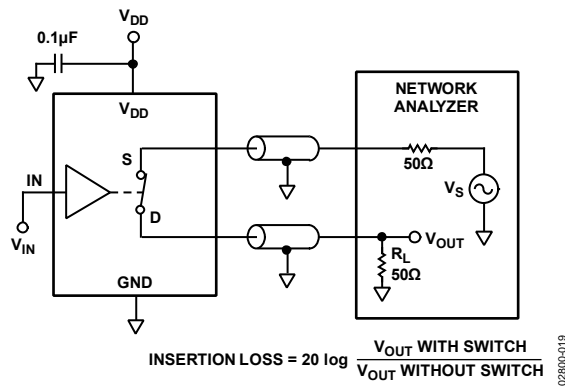
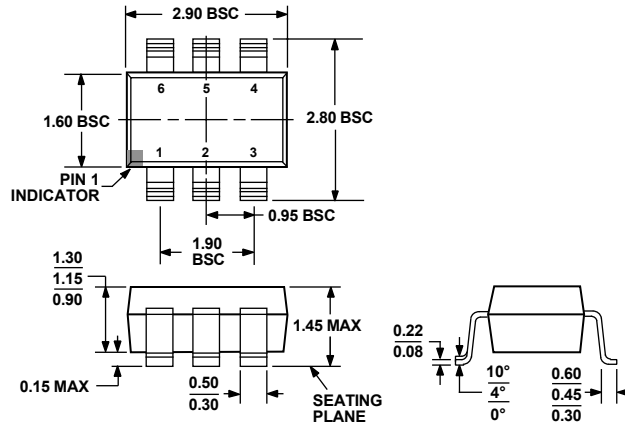


Figure 20. Bandwidth

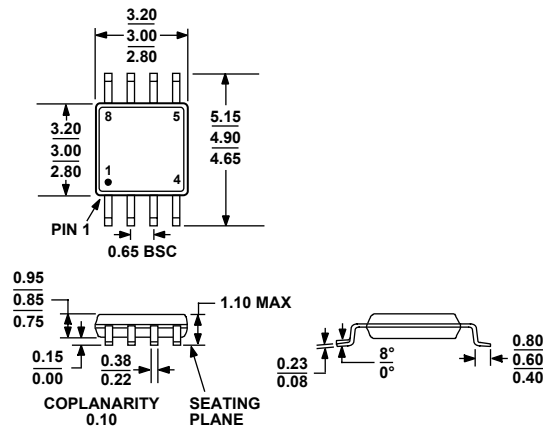
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 21. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)

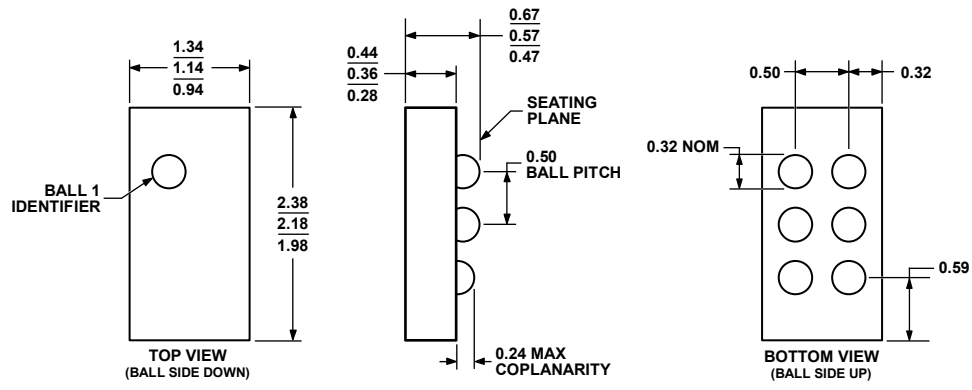
Dimensions shown in inches and (millimetres)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 22. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



062206-A

Figure 23. 6-Ball Wafer Level Chip Scale Package [WLCSP]  
(CB-6-1)  
Dimensions shown in millimeters

# ADG801/ADG802

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding <sup>1</sup>
ADG801BCB-REEL7	-40°C to +125°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-1	SLB
ADG801BCBZ-REEL7 <sup>2</sup>	-40°C to +125°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-1	S06
ADG801BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SLB
ADG801BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SLB
ADG801BRM-REEL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SLB
ADG801BRMZ <sup>2</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S06
ADG801BRMZ-REEL <sup>2</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S06
ADG801BRMZ-REEL7 <sup>2</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S06
ADG801BRT-R2	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SLB
ADG801BRT-500RL7	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SLB
ADG801BRT-REEL	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SLB
ADG801BRT-REEL7	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SLB
ADG801BRTZ-500RL7 <sup>2</sup>	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S06
ADG801BRTZ-REEL <sup>2</sup>	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S06
ADG801BRTZ-REEL7 <sup>2</sup>	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S06
ADG802BCB-REEL7	-40°C to +125°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-1	SMB
ADG802BCBZ-REEL7 <sup>2</sup>	-40°C to +125°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-1	S0F
ADG802BRM-R2	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRM-REEL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SMB
ADG802BRMZ <sup>2</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S0F
ADG802BRMZ-REEL <sup>2</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S0F
ADG802BRMZ-REEL7 <sup>2</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S0F
ADG802BRT-500RL7	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SMB
ADG802BRT-REEL	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SMB
ADG802BRT-REEL7	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SMB
ADG802BRTZ-500RL7 <sup>2</sup>	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S0F
ADG802BRTZ-REEL <sup>2</sup>	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S0F
ADG802BRTZ-REEL7 <sup>2</sup>	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S0F

<sup>1</sup> Branding on SOT-23 and MSOP packages is limited to three characters due to space constraints.

<sup>2</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**